DDR Termination Regulator

General Description

The RTQ2536-QA is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RTQ2536-QA possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 10μF (effective value) ceramic output capacitor. The RTQ2536-QA supports remote sensing functions and all features required to power the DDRI / DDRII / DDRIII / DDRIII-L / DDRIV and DDRIV-L VTT bus termination according to the JEDEC specification.

The RTQ2536-QA is available in the thermal efficient package, WDFN-10SL 3x3.

Ordering Information

RTQ2536□□-QA

- Grade
  QA: AEC-Q100 Qualified and Screened by High Temperature
- Package Type
  QW: WDFN-10SL 3x3 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note :

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

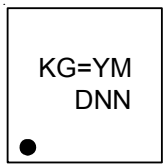
Features

- **AEC-Q100 Grade 1 Qualified**
- **VIN Input Voltage Range : 1V to 3.5V**
- **VCNTL Input Voltage Range : 2.9V to 5.5V**
- **Support Ceramic Capacitors**
- **10mA Source/Sink Reference Output**
- **Meets DDRI, DDRII JEDEC Spec**
- **Supports DDRIII, DDRIII-L, DDRIV and DDRIV-L Applications**
- **Soft-Start Function**
- **UVLO and OCP Protection**
- **Thermal Shutdown**

Applications

- Automotive and Industrial Supplies
- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

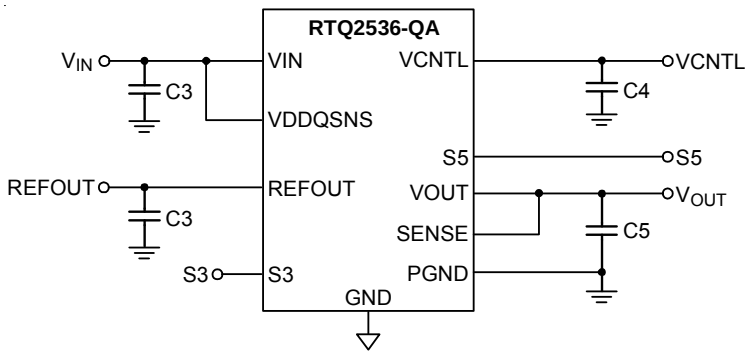
Marking Information



KG= : Product Code

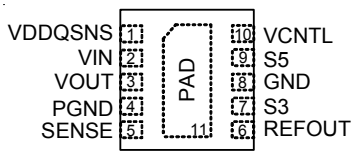
YMDNN : Date Code

Simplified Application Circuit



Pin Configuration

(TOP VIEW)

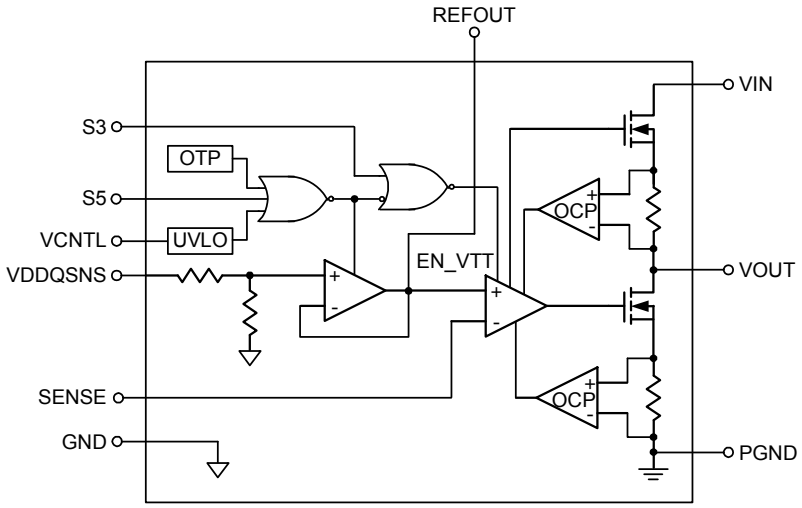


WDFN-10SL 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDDQSNS	Reference input.
2	VIN	Power input of the regulator.
3	VOUT	Power output of the regulator.
4	PGND	Power ground of the regulator.
5	SENSE	Voltage sense input for the regulator. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	Reference output. Connect to GND through a 0.1μF ceramic capacitor.
7	S3	S3 signal input.
9	S5	S5 signal input.
10	VCNTL	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A ceramic decoupling capacitor with a value 4.7μF is required.
8	GND	Analog ground. Connect to negative terminal of the output capacitor.
11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

Functional Block Diagram



Operation

The RTQ2536-QA is a linear sink/source DDR termination regulator with current capability up to 2A. The RTQ2536-QA builds in a high-side N-MOSFET which provides current sourcing and a low-side N-MOSFET which provides current sinking. All the control circuits are supplied by the power VCNTL. In normal operation, the error amplifier OP adjusts the gate driving voltage of the power MOSFET to achieve SENSE voltage well tracking the VDDQSNS/2 voltage.

Both the source and sink currents are detected by the internal sensing resistor, and the OCP function will work to limit the current to a designed value when overload happens. Furthermore, the current will be folded back to be one half if VOUT is out of the power good window.

Buffer

This function provides REFOUT output equal to VDDQSNS/2 with 10mA source/sink current capability.

Control Logic

This block includes VCNTL UVLO, VDDQSNS UVLO and Enable/Disable functions, and provides logic control to the whole chip.

Thermal Protection

Both the high-side and low-side power MOSFETs will be turned off when the junction temperature is higher than typically 160°C, and be released to normal operation when junction temperature falls below 135°C typically.

Power State Control

The input pins S3 and S5 of the RTQ2536-QA, provide simple control of the power state. Table 1 describes S3/S5 terminal logic state and corresponding state of REFOUT/VOUT outputs. VOUT is turn-off and discharged to GND in state S3. When both S5 and S3 pins are LOW, the power state is set to S4/S5. In S4/S5 state, all the outputs are turn-off and discharged to GND.

Table 1. S3 and S5 Control Table

STATE	S3	S5	REFOUT	VOUT
S0	HI	HI	ON	ON
S3	LO	HI	ON	OFF (Discharge)
S4/S5	LO	LO	OFF (Discharge)	OFF (Discharge)

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN, VCNTL ---------- –0.3V to 6V
- Input Voltage, S3, VDDQSNS, SENSE, S5 ---------- –0.3V to 6V
- Output Voltage, VOUT, REFOUT ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10SL 3x3 ---------- 4.09W
- Package Thermal Resistance (Note 2)
  WDFN-10SL 3x3, θ_{JA} ---------- 30.5°C/W
  WDFN-10SL 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Thermal Shutdown Temperature ---------- 160°C
- Thermal Shutdown Hysteresis ---------- 15°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Control Input Voltage, VCNTL ---------- 2.9V to 5.5V
- Supply Input Voltage, VIN ---------- 1V to 3.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = $V_{VDDQSNS}$ = 1.5V, V_{CNTL} = 3.3V, V_{SENSE} = 0.75V, C_{OUT} = 10µF x 1, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCNTL Supply Current	I_{VCNTL}	V_{S3} = VCNTL, V_{S5} = VCNTL, no load	--	0.5	0.75	mA
VCNTL Shutdown Current	I_{SHDN_VCNTL}	V_{S3} = 0V, V_{S5} = 0V, no load	--	65	80	µA
		V_{S3} = 0V, V_{S5} = VCNTL, no load	--	200	350	µA
VIN Supply Current	I_{VIN}	V_{S3} = VCNTL, V_{S5} = VCNTL, no load	--	1	35	µA
VIN Shutdown Current	I_{SHDN_VIN}	V_{S3} = 0V, V_{S5} = 0V, no load	--	0.1	10	µA
Output						
VOUT Output Voltage	V_{OUT}	V_{IN} = 1.5V, $V_{VDDQSNS}$ = 1.5V, I_{OUT} = 0A	--	0.75	--	V
		V_{IN} = 1.35V, $V_{VDDQSNS}$ = 1.35V, I_{OUT} = 0A	--	0.675	--	
		V_{IN} = 1.2V, $V_{VDDQSNS}$ = 1.2V, I_{OUT} = 0A	--	0.6	--	
		V_{IN} = 1.05V, $V_{VDDQSNS}$ = 1.05V, I_{OUT} = 0A (Note 5)	--	0.525	--	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Output Voltage Offset		V_{OUT_OS}	I_{OUT} = ±2A, V_{IN} = 1.5V, V_{REFOUT} = 0.75V	–30	--	30	mV
			I_{OUT} = ±2A, V_{IN} = 1.35V, V_{REFOUT} = 0.675V	–30	--	30	
			I_{OUT} = ±2A, V_{IN} = 1.2V, V_{REFOUT} = 0.6V	–30	--	30	
			I_{OUT} = ±2A, V_{IN} = 1.05V, V_{REFOUT} = 0.525V (Note 5)	–30	--	30	
VOUT Source Current Limit		$I_{LIM\_VOUT\_SR}$	VOUT in PGOOD window	2	--	--	A
VOUT Sink Current Limit		$I_{LIM\_VOUT\_SK}$	VOUT in PGOOD window	2	--	--	A
VOUT Discharge Resistance		$R_{DISCHARGE}$	$V_{VDDQSNS}$ = 0V, V_{OUT} = 0.3V, V_{S3} = 0V	--	18	25	Ω
VDDQSNS and REFOUT							
VDDQSNS Input Current		$I_{VDDQSNS}$	$V_{VDDQSNS}$ = 1.8V	20	30	40	μA
VDDQSNS Voltage Range		$V_{VDDQSNS}$		0.5	--	1.8	V
REFOUT Voltage Tolerance to $V_{VDDQSNS}$		V_{TOL_REFOUT}	–10mA < I_{REFOUT} < 10mA, $V_{VDDQSNS}$ = 1.5V	–15	--	15	mV
			–10mA < I_{REFOUT} < 10mA, $V_{VDDQSNS}$ = 1.35V	–13.5	--	13.5	
			–10mA < I_{REFOUT} < 10mA, $V_{VDDQSNS}$ = 1.2V	–12	--	12	
			–10mA < I_{REFOUT} < 10mA, $V_{VDDQSNS}$ = 1.05V (Note 5)	–10.5	--	10.5	
REFOUT Source Current Limit		$I_{LIM\_REFOUT\_SR}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit		$I_{LIM\_REFOUT\_SK}$	V_{REFOUT} = VDDQSNS / 2 + 1V	10	40	--	mA
UVLO/S3/S5							
UVLO Threshold		V_{UVLO_VCNTL}	Rising	2.5	2.7	2.85	V
			Hysteresis	--	120	--	mV
S3/S5 Input Voltage	Logic-High	V_{IN_H}		1.7	--	--	V
	Logic-Low	V_{IN_L}		--	--	0.3	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

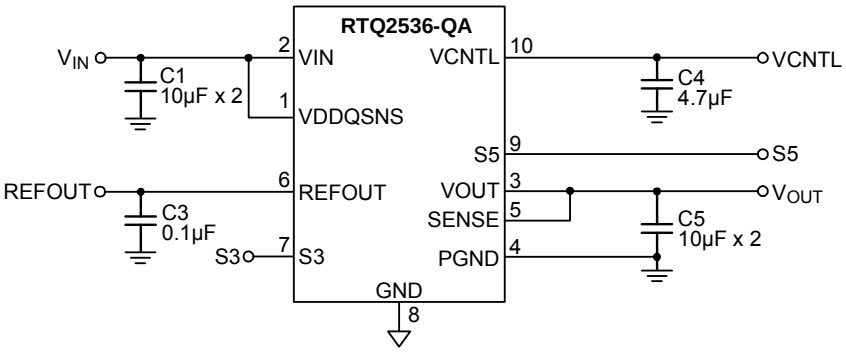
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

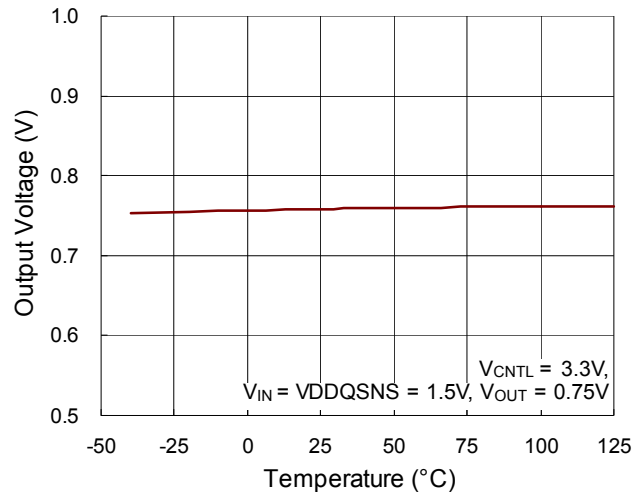
Note 5. Guarantee by design.

Typical Application Circuit

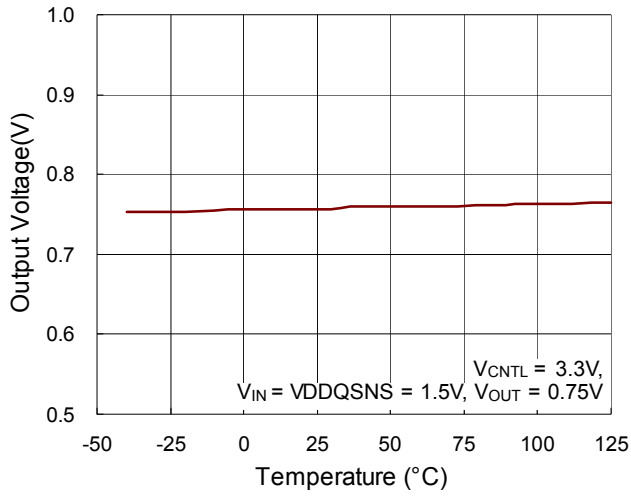


Typical Operating Characteristics

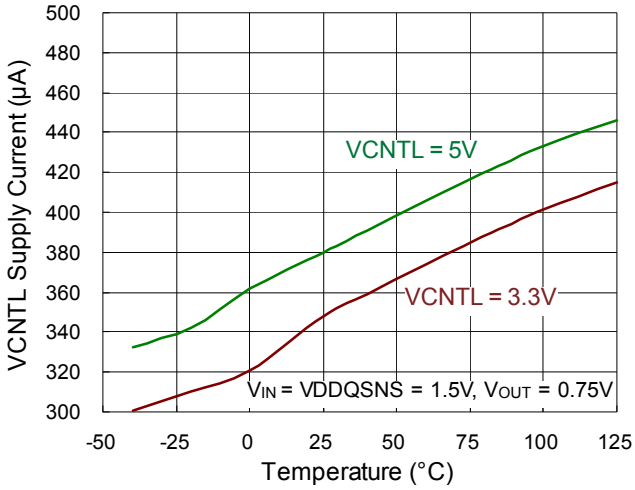
Output Voltage vs. Temperature



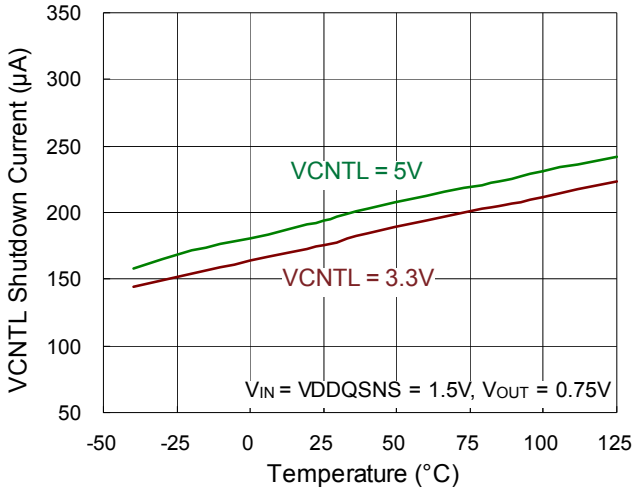
REFOUT Voltage vs. Temperature



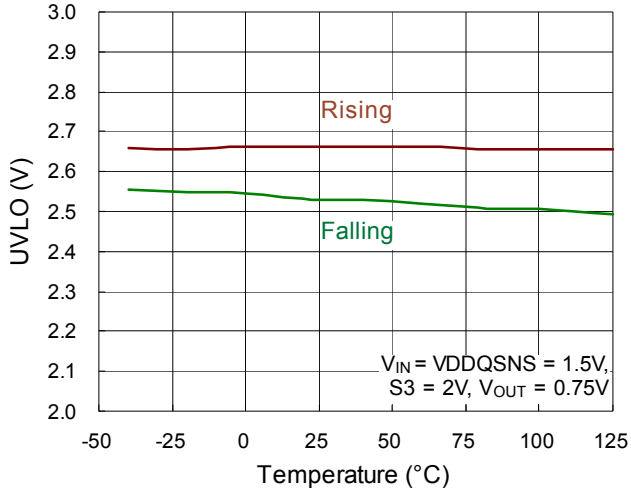
VCNTL Supply Current vs. Temperature



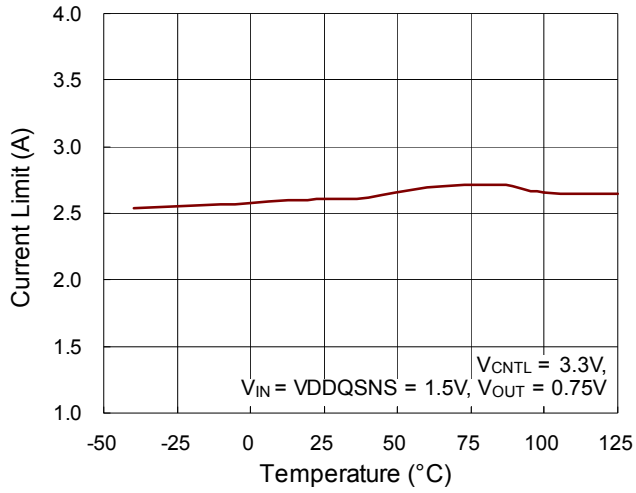
VCNTL Shutdown Current vs. Temperature



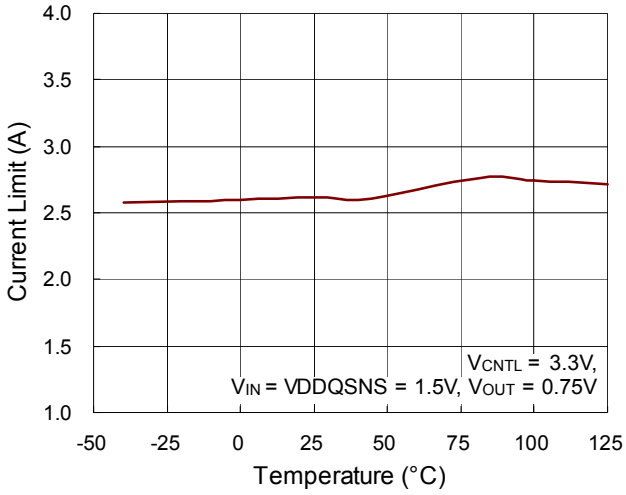
UVLO vs. Temperature



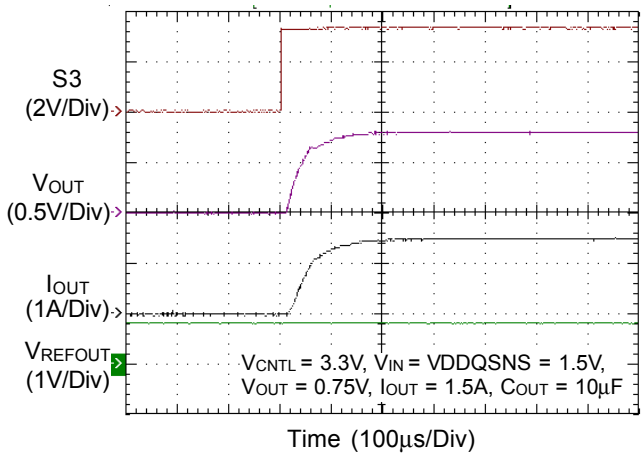
Sourcing Current Limit vs. Temperature



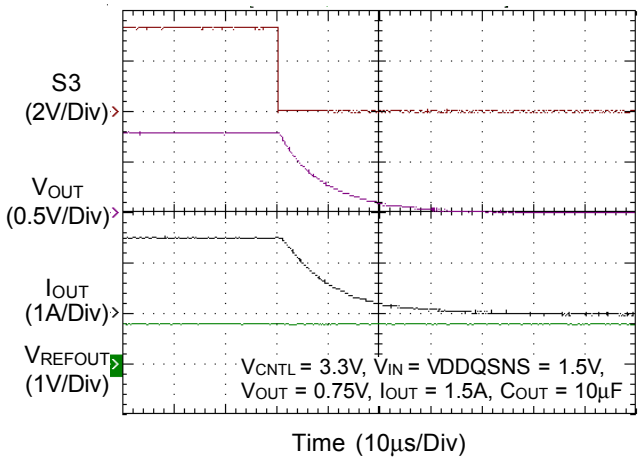
Sinking Current Limit vs. Temperature



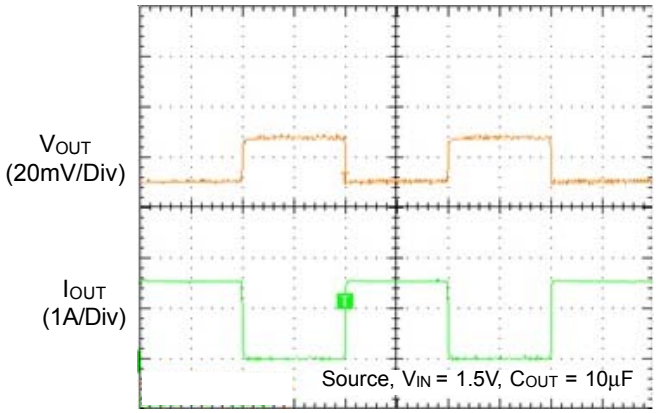
Power On from S3



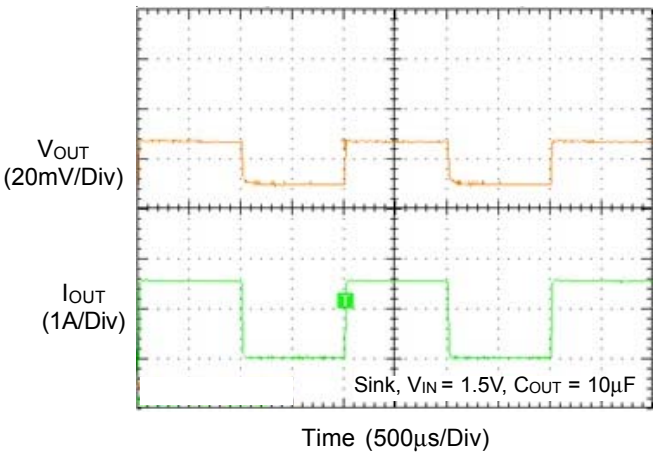
Power Off from S3



0.75V_{OUT} @ 1.5A Transient Response



0.75V_{OUT} @ 1.5A Transient Response



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RTQ2536-QA is a 2A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count system such as notebook PC applications. The RTQ2536-QA possesses a high speed operating amplifier that provides fast load transient response and only requires two 10µF ceramic input capacitor and a 10µF ceramic output capacitors.

Capacitor Selection

Good bypassing is recommended from VIN to GND to help improve AC performance. A 10µF or greater input capacitor located as close as possible to the IC is recommended. The input capacitor must be located at a distance of less than 0.5 inches from the VIN pin of the IC.

For stable operation, the total capacitance of the ceramic capacitor at the VTT output terminal must be larger than 10µF (effective value). The RTQ2536-QA is designed specifically to work with low ESR ceramic output capacitor in space saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. The output capacitor should be located near the VTT output terminal pin as close as possible.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10SL 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 4.09W for a WDFN-10SL 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

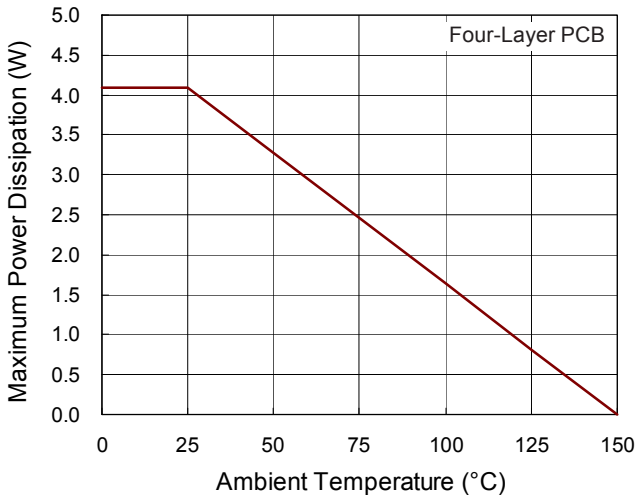
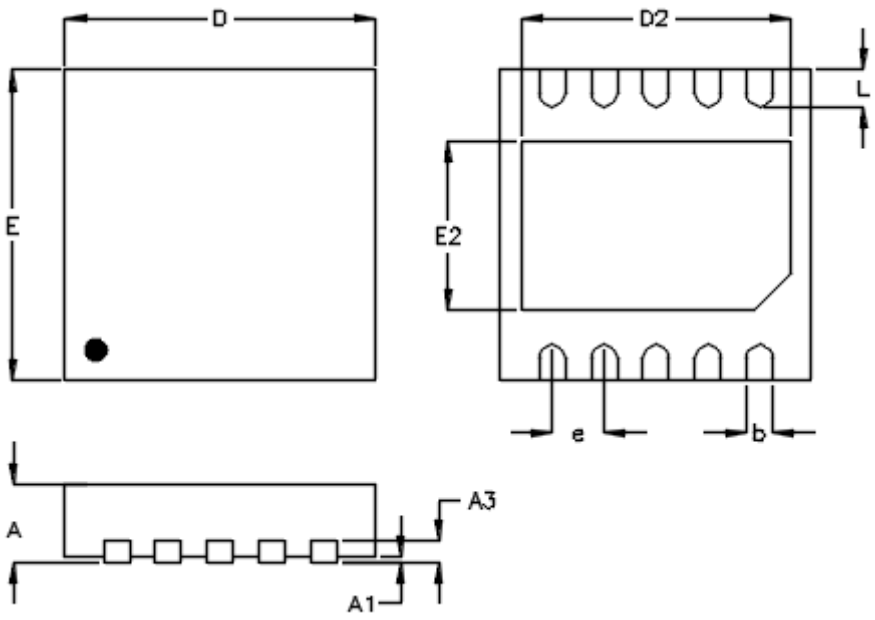
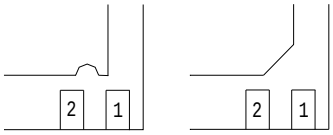


Figure 1. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

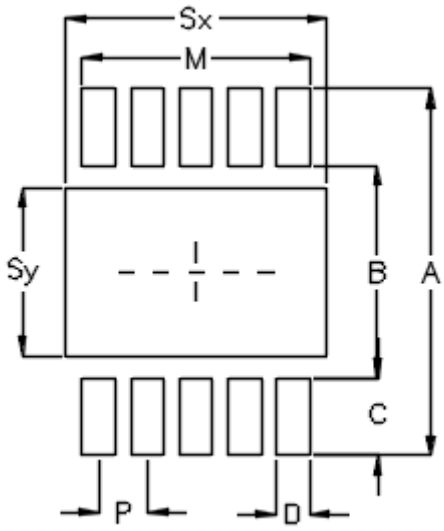
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.900	3.100	0.114	0.122
D2	2.550	2.650	0.100	0.104
E	2.900	3.100	0.114	0.122
E2	1.590	1.690	0.063	0.067
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 10SL DFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-10S	10	0.50	3.80	2.20	0.80	0.35	2.70	1.74	2.35	±0.05

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Datasheet Revision History

Version	Date	Description	Item
02	2023/10/27	Modify	Ordering Information on P1 Add Footprint Information on P12