6A, 18V, Synchronous Step-Down Converter

General Description

The RTQ2816 is a high efficiency, monolithic synchronous step-down DC-DC converter that can deliver up to 6A output current from a 4.5V to 18V input supply. The RTQ2816 current-mode architecture with external compensation allows the transient response to be optimized over a wide range of loads and output capacitors. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. Fault condition protections include output under-voltage protection, output over-voltage protection, and over-temperature protection. The low current shutdown mode provides output disconnection, enabling easy power management in battery-powered systems.

Features

- **Low $R_{DS(ON)}$ Power MOSFET Switches 26mΩ/19mΩ**
- **Input Voltage Range : 4.5V to 18V**
- **Adjustable Switching Frequency : 200kHz to 1.6MHz**
- **Current-Mode Control**
- **Synchronous to External Clock : 200kHz to 1.6MHz**
- **Accurate Voltage Reference 0.8V ± 1%, Over –40°C to 85°C**
- **Monotonic Start-Up into Pre-biased Outputs**
- **Adjustable Soft-Start**
- **Power Good Indicator**
- **Under-Voltage and Over-Voltage Protection**
- **Input Under-Voltage Lockout**
- **RoHS Compliant and Halogen Free**

Ordering Information

RTQ2816□□

- Package Type
  QW : WQFN-14AL 3.5x3.5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

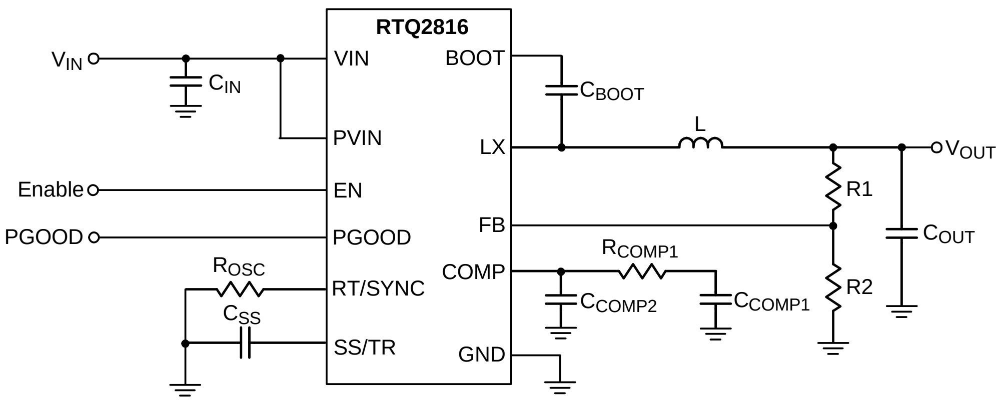
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

- High Performance Point of Load Regulation
- Notebook Computers
- High Density and Distributed Power Systems

Simplified Application Circuit



Marking Information

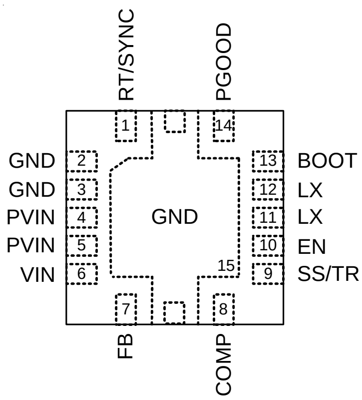
1T=YM DNN

1T= : Product Code

YMDNN : Date Code

Pin Configuration

(TOP VIEW)

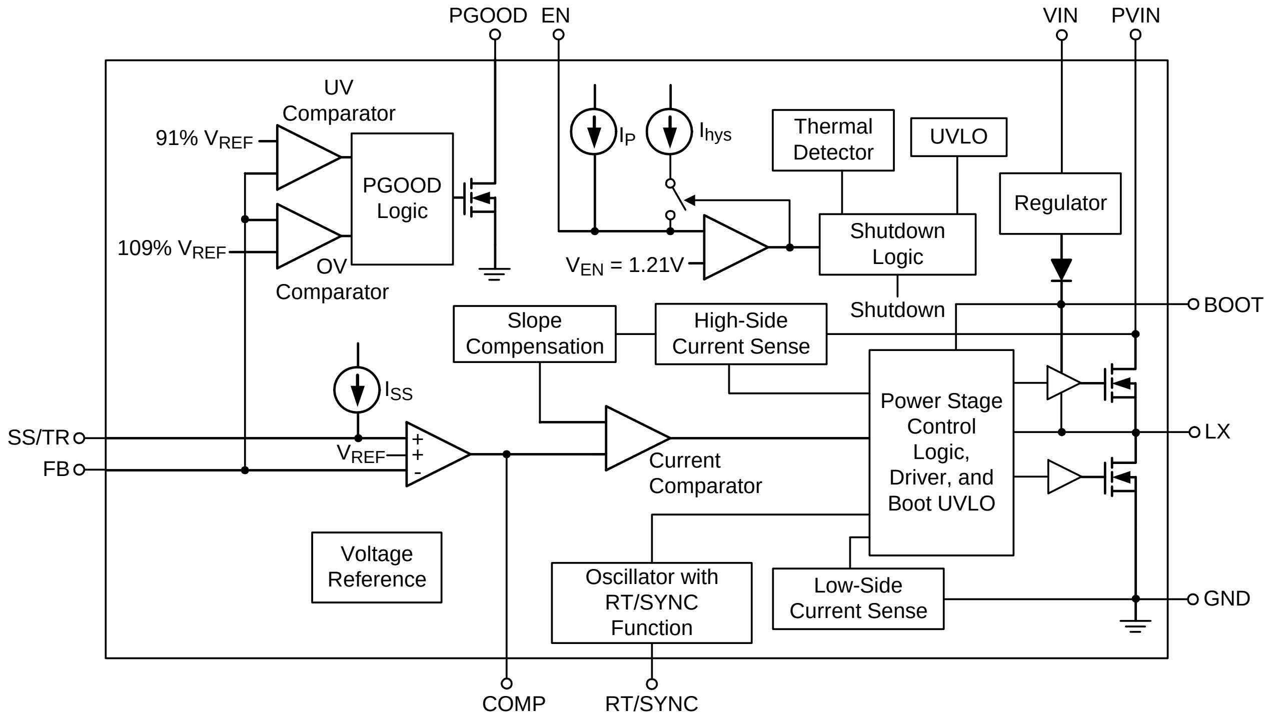


WQFN-14AL 3.5x3.5

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	RT/SYNC	Oscillator resistor and external frequency synchronization input. Connecting a resistor from this pin to GND sets the switching frequency or connecting an external clock to this pin changes the switching frequency.
2, 3, 15 (Exposed Pad)	GND	System ground. Provide the ground return path for the control circuitry and low-side power MOSFET. The exposed pad must be soldered to a large PCB and connected to GND for minimum power dissipation.
4, 5	PVIN	Power input. Supplies the power switches of the device.
6	VIN	Supply voltage input. Supplies the control circuitry and internal reference of the device.
7	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.8V typically.
8	COMP	Compensation node. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop.
9	SS/TR	Soft-start and tracking control input. Connect a capacitor from SS to GND to set the soft-start period. The soft-start period can be used to track and sequence when the external voltage on this pin overrides the internal reference.
10	EN	Enable control input. Floating this pin or connecting this pin to logic high can enable the device and connecting this pin to GND can disable the device.
11, 12	LX	Switch node. LX is the switching node that supplies power to the output and connect the output LC filter from LX to the output load.
13	BOOT	Bootstrap supply for high-side gate driver. Connect a 100nF or greater capacitor from LX to BOOT to power the high-side switch.
14	PGOOD	Power good indicator output. This pin is an open-drain logic output that is pulled to ground when the output voltage is lower or higher than its specified threshold under the conditions of OVP, OTP, dropout, EN shutdown, or during slow start.

Functional Block Diagram



Operation

UV Comparator

If the feedback voltage (V_{FB}) is lower than threshold voltage (91% of V_{REF}), the UV Comparator's output goes high and the logic control circuit is allowed to turn on the MOSFET to pull PGOOD pin to low.

OV Comparator

If the feedback voltage (V_{FB}) is higher than threshold voltage (109% of V_{REF}), the OV Comparator's output goes high and the logic control circuit is allowed to turn on the MOSFET to pull PGOOD pin to low.

Voltage Reference

The converter produces a precise ±1% voltage reference over-temperature by scaling the output of a temperature stable bandgap circuit.

Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the FB pin voltage with the SS/TR pin voltage and the internal reference voltage which is 0.8V. The transconductance of the error amplifier is 1300 μA/V during normal operation. The compensation network should be connected between the COMP pin and ground.

Oscillator with RT/SYNC Function

The switching frequency is adjustable by an external resistor connected between the RT/SYNC pin and GND. The available frequency range is from 200kHz to 1.6MHz. An internal synchronized circuit has been implemented to switch from RT mode to SYNC mode. To implement the synchronization function, connect a square wave clock signal to the RT/SYNC pin with a duty cycle between 10% to 90%. The switching cycle is synchronized to the falling edge of the external clock at RT/SYNC pin.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN, PVIN ---------- –0.3V to 20V
- Switch Node Voltage, LX ---------- –1V to 20.3V
  LX (t ≤ 10ns) ---------- –5V to (V_{IN} + 6.3V)
- BOOT Pin Voltage ---------- –0.3V to (V_{IN} + 7V)
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-14AL 3.5x3.5 ---------- 2.083W
- Package Thermal Resistance (Note 2)
  WQFN-14AL 3.5x3.5, θ_{JA} ---------- 48°C/W
  WQFN-14AL 3.5x3.5, θ_{JC} ---------- 3.8°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Power Input Voltage, PVIN ---------- 1.6V to 18V
- Supply Input Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 4.5V to 18V, V_{PVIN} = 1.6V to 18V, T_A = –40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
PVIN Power Input Operating Voltage	PVIN		1.6	--	18	V
VIN Supply Input Operating Voltage	V_{IN}		4.5	--	18	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	--	4	4.5	V
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	150	--	mV
VIN Shutdown Current		V_{EN} = 0V	--	3	9	μA
VIN Quiescent Current		V_{FB} = 0.83V, not switching	--	600	1000	μA
Enable Voltage						
EN Threshold Voltage	V_{IH}	V_{EN} rising	--	1.21	1.26	V
	V_{IL}	V_{EN} falling	1.1	1.17	--	V
Pull-Up Current		V_{EN} = 1.1V	--	1	--	μA
Hysteresis Current		V_{EN} = 1.3V	--	3	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage						
Reference Voltage	V_{REF}	$0A \le I_{LOAD} \le 6A$	0.792	0.8	0.808	V
Timing Resistor and External Clock						
Switching Frequency	f_{OSC}	R_{OSC} = 27kΩ	1440	1600	1760	kHz
		R_{OSC} = 110kΩ	400	480	560	
		R_{OSC} = 270kΩ	160	200	240	
Switching Frequency Range		Include Sync mode and RT mode set point	200	--	1600	
Minimum Sync Pulse Width			--	20	--	ns
SYNC Threshold Voltage		High-Level	--	--	2	V
		Low-Level	0.8	--	--	
SYNC Falling Edge to LX Rising Edge Delay		Measure at 500kHz with R_{OSC} resistor in series	--	66	--	ns
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$	$V_{BOOT} - V_{LX}$ = 5.5V	--	26	40	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$	V_{IN} = 12V	--	19	30	
LX and BOOT						
Minimum On-Time	t_{ON_MIN}	Measured at 90% to 90% of V_{LX}, I_{LX} = 2A, 25°C	--	--	135	ns
Minimum Off-Time	t_{OFF_MIN}	$V_{BOOT} - V_{LX} \ge 3V$	--	0	--	
BOOT–LX UVLO	$V_{BL\text{-}UVLO}$		--	--	3	V
Soft-Start and Tracking						
Internal Charge Current			--	2	--	μA
SS to Feedback Offset		V_{SS} = 0.4V	--	20	60	mV
Current Limit						
High-Side Switch Current Limit			8	11	--	A
Low-Side Switch Sourcing Current Limit			7	10	--	
Low-Side Switch Sinking Current Limit			--	2.3	--	
Error Amplifier						
Error Amplifier Trans-conductance	gm	$-2\mu A < I_{COMP} < 2\mu A$, V_{COMP} = 1V	--	1300	--	μA/V
Error Amplifier DC Gain		V_{FB} = 0.8V	1000	3100	--	V/V
Error Amplifier Sink/Source Current		V_{COMP} = 1V, 100mV input overdrive	--	±110	--	μA
COMP to I_{switch} gm			--	16	--	A/V
Power Good						
Power Good Rising Threshold		V_{FB} rising (Good)	--	94	--	$\%V_{REF}$
		V_{FB} rising (Fault)	--	109	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Falling Threshold		V_{FB} falling (Fault)	--	91	--	$\%V_{REF}$
		V_{FB} falling (Good)	--	106	-	
Power Good Sink Current Capability		PGOOD signal fault, I_{PGOOD} sinks 2mA	--	--	0.3	V
Power Good Leakage Current		PGOOD signal good, V_{PGOOD} = 5.5V	--	30	100	nA
Minimum VIN for Indicating PGOOD		V_{PGOOD} $<$ 0.5V, I_{PGOOD} sinks 100μA	--	0.6	1	V
Minimum SS/TR Voltage for Indicating PGOOD			--	--	2.6	
Over-Temperature Protection						
Thermal Shutdown	T_{SD}		160	175	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

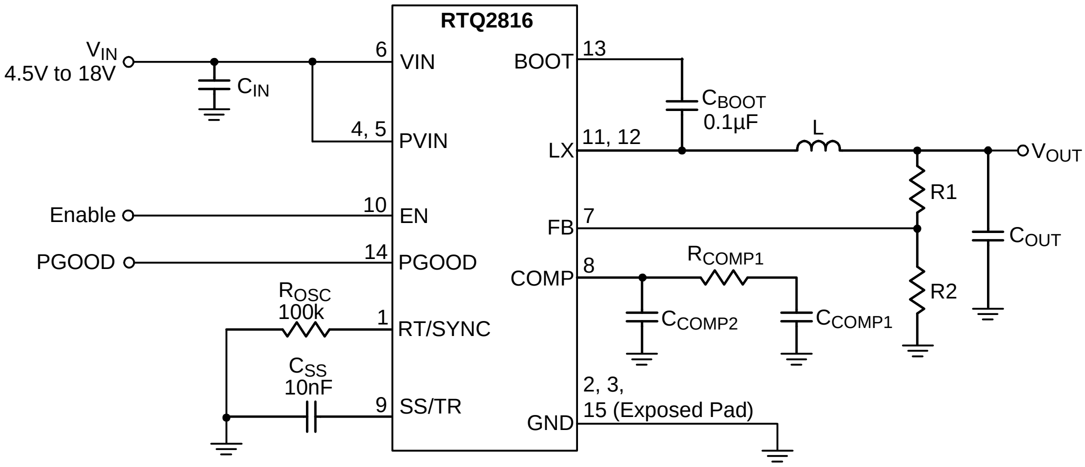
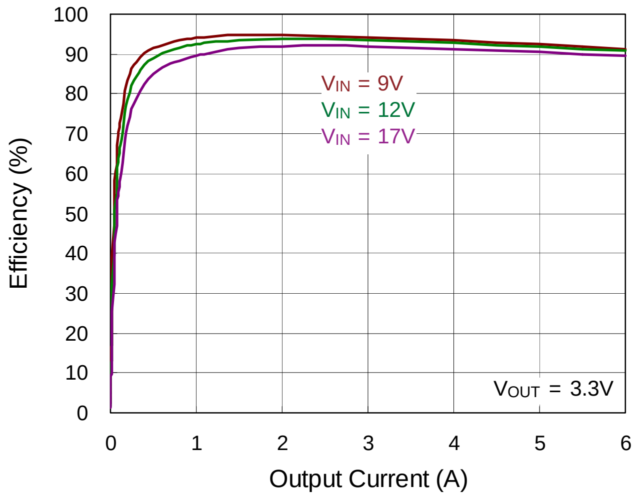


Table 1. Suggested Component Values

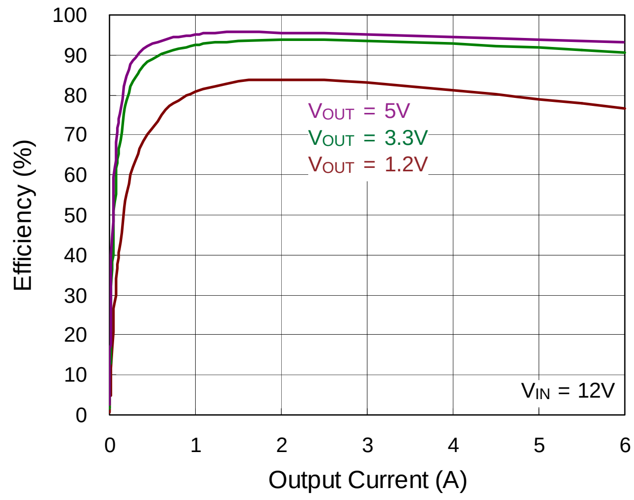
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_{COMP1} (kΩ)	C_{COMP1} (nF)	C_{COMP2} (pF)	C_{OUT} (μF)	L (μH)
5.0	126	24	4.3	8.2	180	22 x 2	4.7
3.3	75	24	2.4	8.2	180	22 x 2	3.7
2.5	51	24	1.8	8.2	180	22 x 2	3.7
1.8	30	24	1.5	8.2	180	22 x 2	2.2
1.5	21	24	1.0	8.2	180	22 x 2	2.2
1.2	12	24	0.82	8.2	180	22 x 2	2.2
1.0	6	24	0.68	8.2	180	22 x 2	1.5

Typical Operating Characteristics

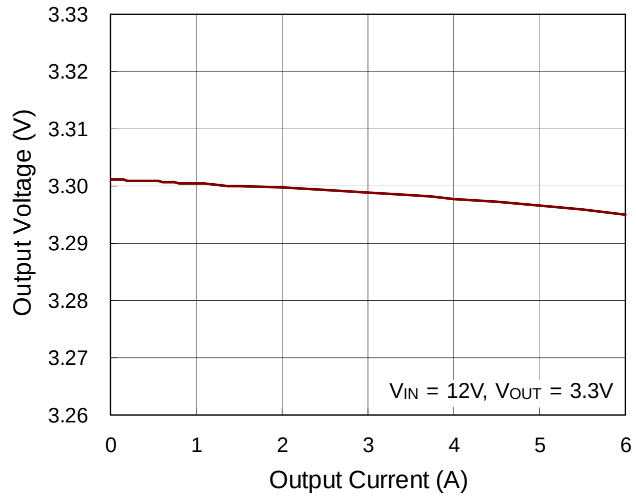
Efficiency vs. Output Current



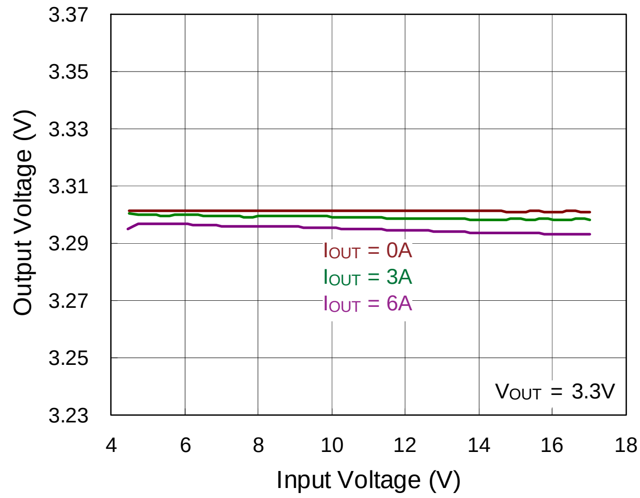
Efficiency vs. Output Current



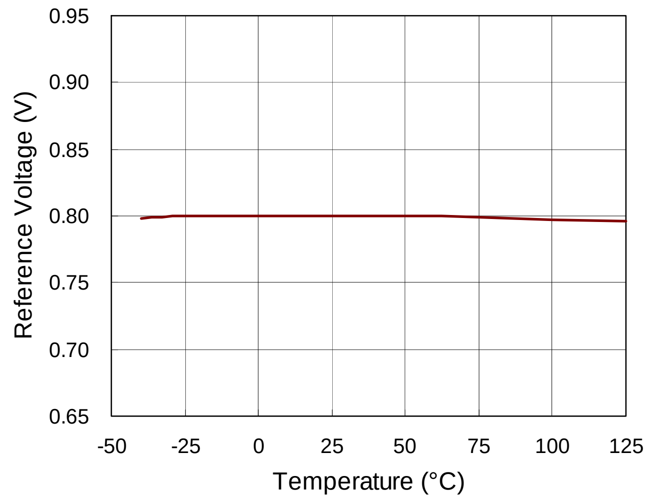
Output Voltage vs. Output Current



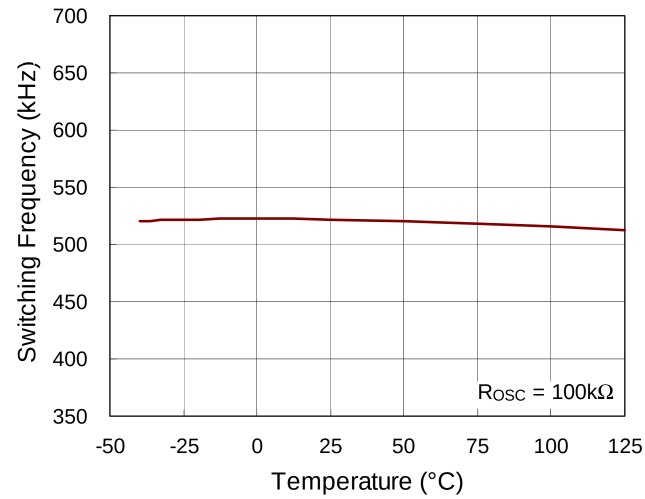
Output Voltage vs. Input Voltage



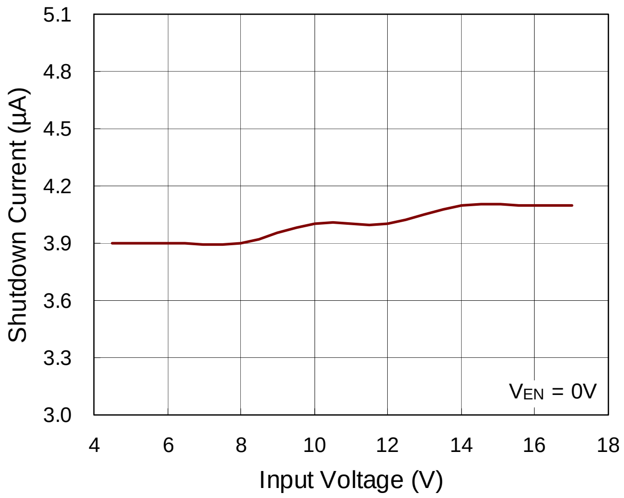
Reference Voltage vs. Temperature



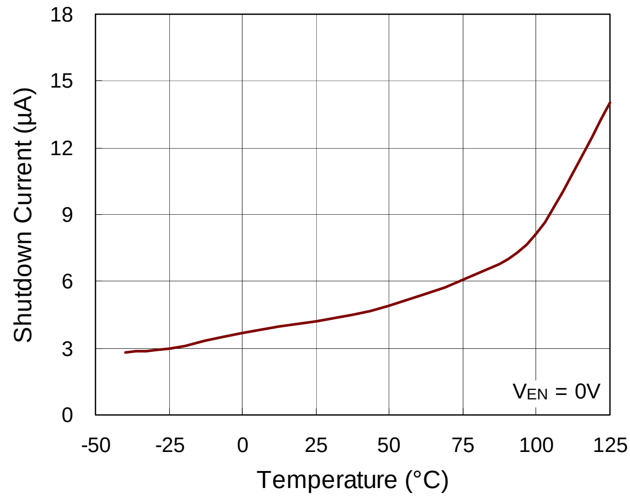
Switching Frequency vs. Temperature



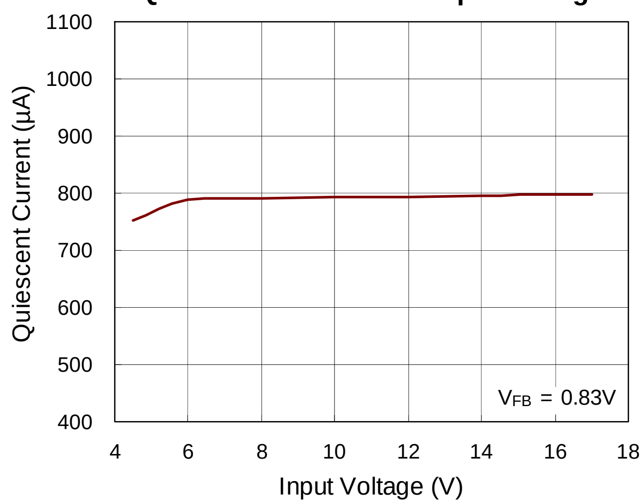
Shutdown Current vs. Input Voltage



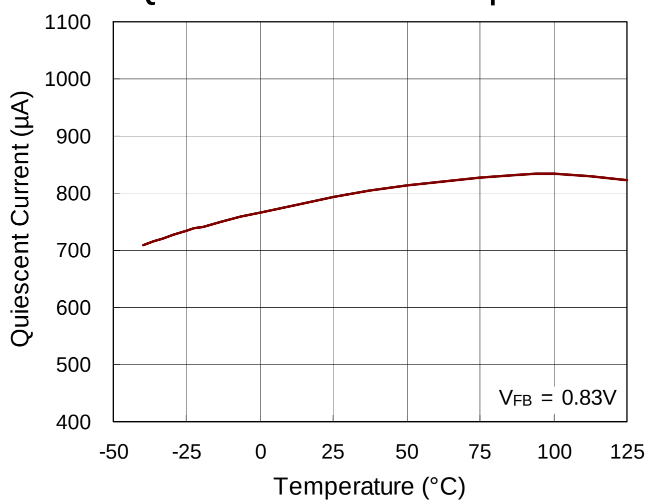
Shutdown Current vs. Temperature



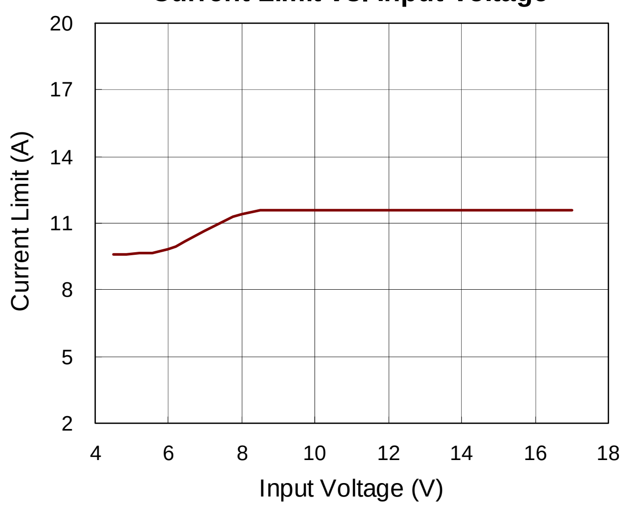
Quiescent Current vs. Input Voltage



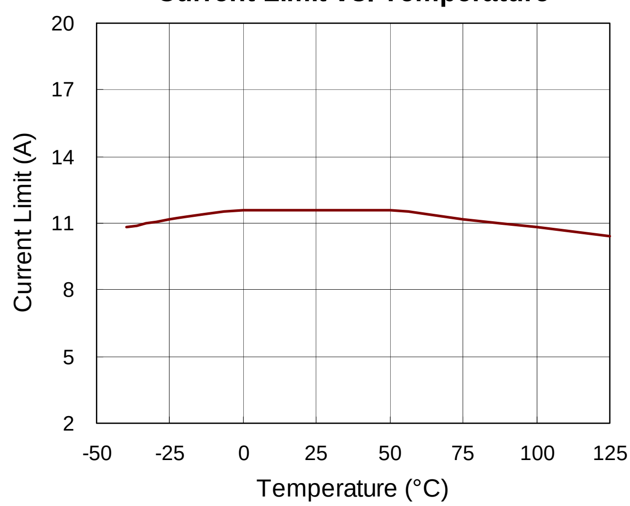
Quiescent Current vs. Temperature



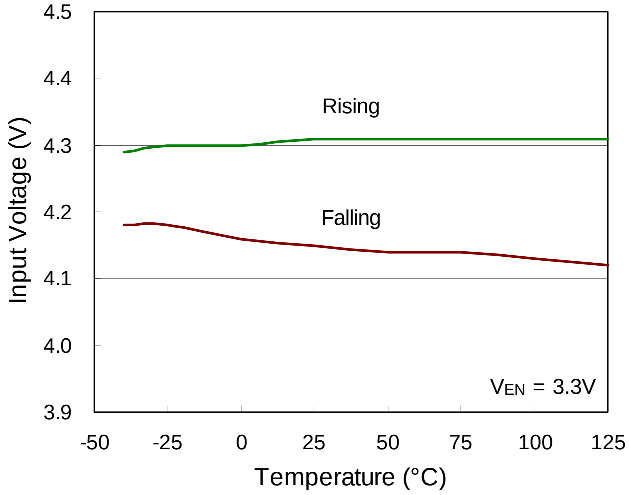
Current Limit vs. Input Voltage



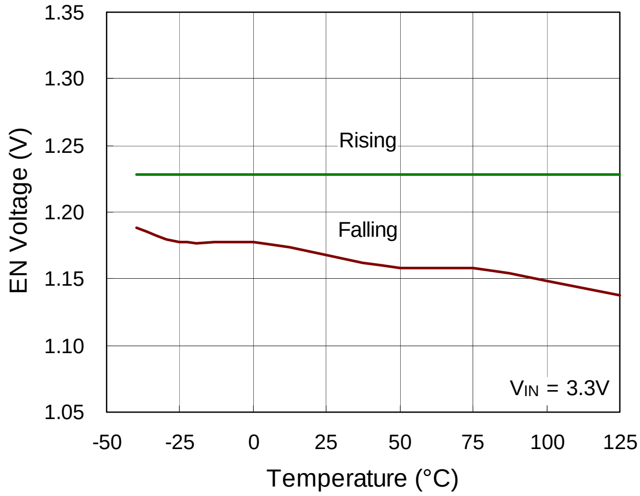
Current Limit vs. Temperature



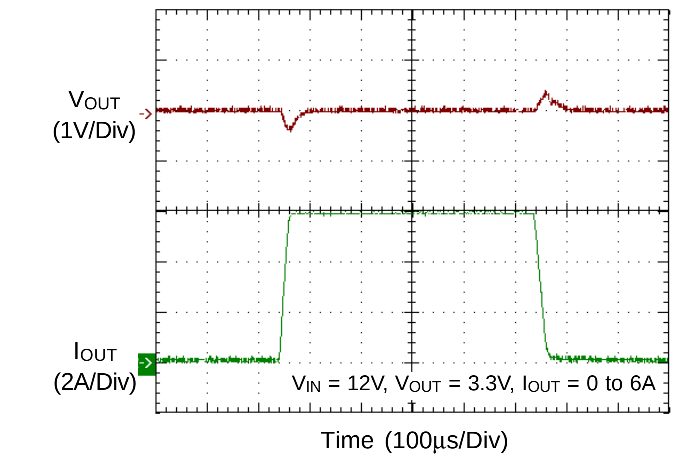
Input Voltage vs. Temperature



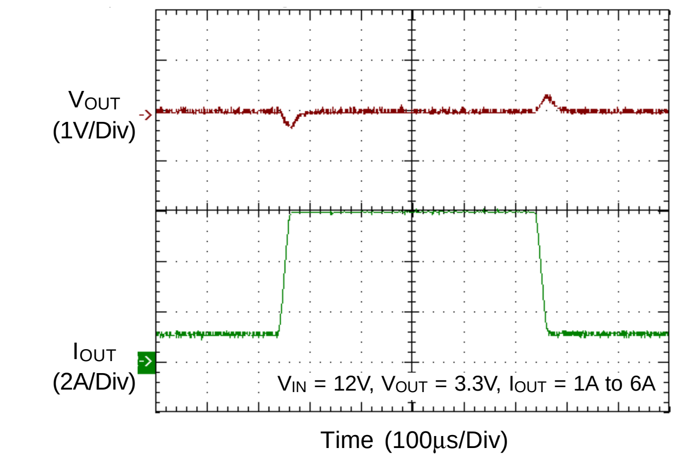
EN Voltage vs. Temperature



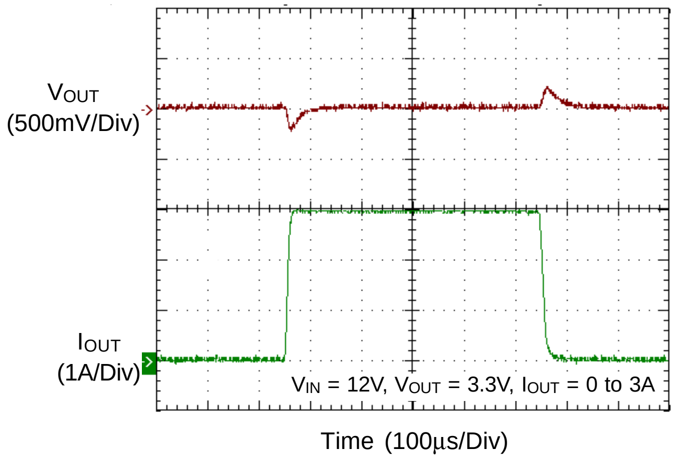
Load Transient Response



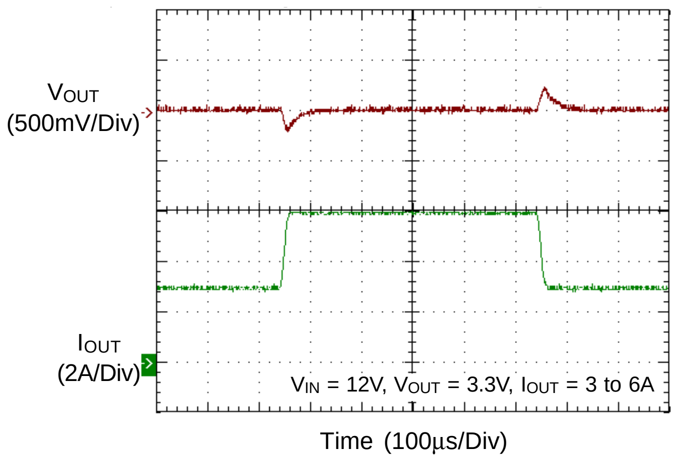
Load Transient Response



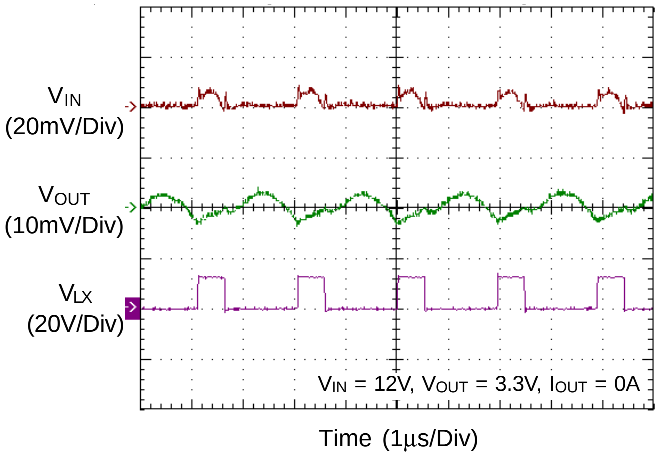
Load Transient Response



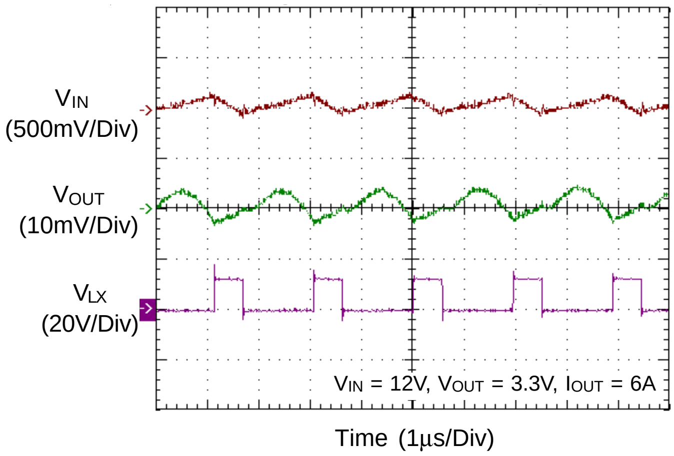
Load Transient Response



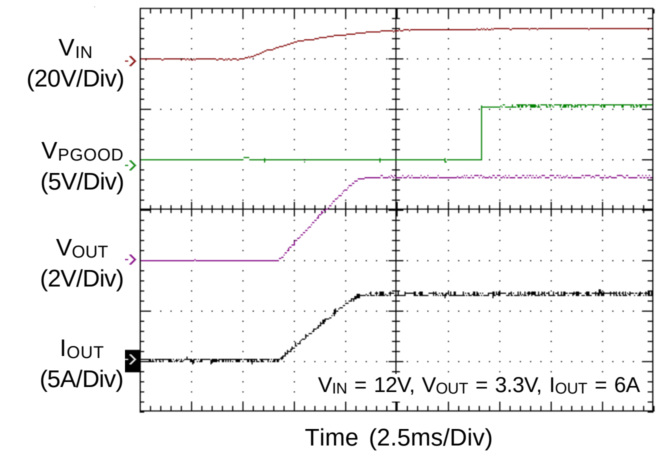
Voltage Ripple



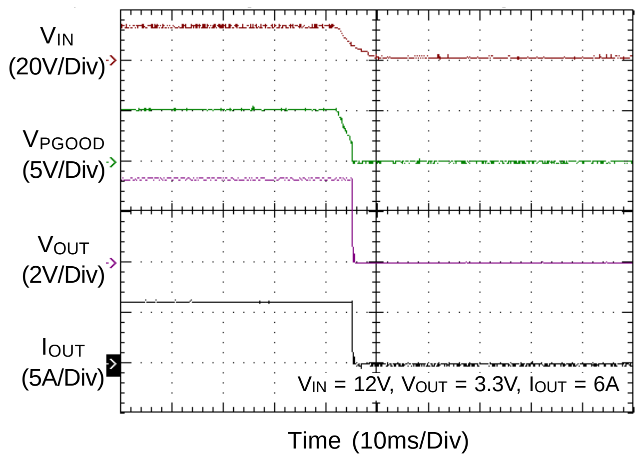
Voltage Ripple



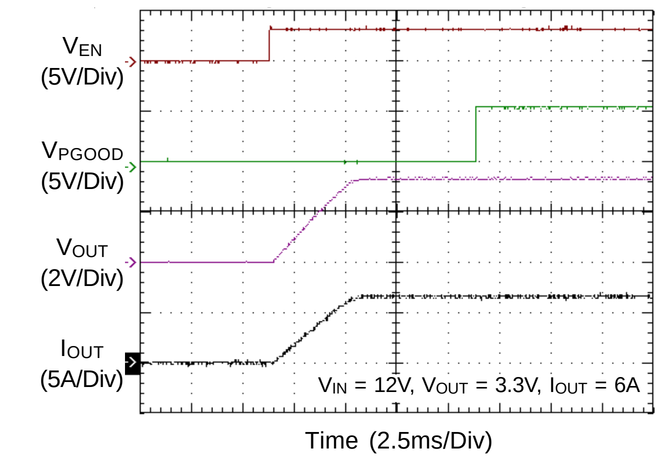
Power On from VIN



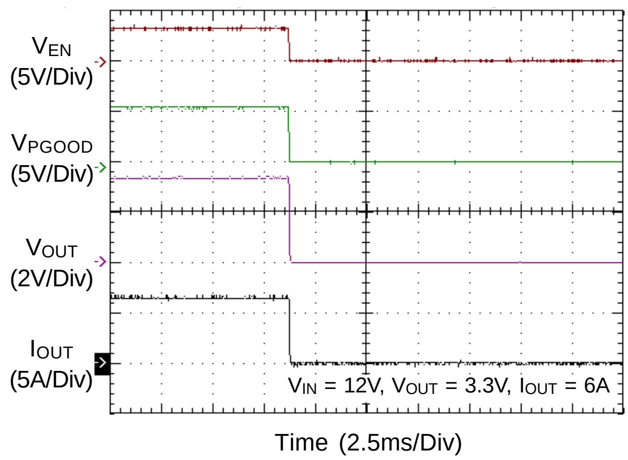
Power Off from VIN



Power On from EN



Power Off from EN



Application Information

This IC is a single phase Buck PWM converter with two integrated N-MOSFETs. It provides good performance during load and line transients by implementing a single feedback loop, current-mode control, and external compensation. The integrated synchronous power switches can increase efficiency and it is suitable for lower duty cycle applications. The switching frequency can be externally set from 200kHz to 1.6MHz which allows for high efficiency and optimal size selection of output filter components. In additional, there is a synchronization mode control in this device which can be synchronized to the external clock frequency, and easily switched from internal switching mode to synchronization mode.

The device contains a power good protection and an external soft-start function that is able to monitor the system output voltage for normal regulation and provides a programmable power up sequence for avoiding inrush currents efficiently. Furthermore, the device incorporates a lot of protections such as OVP, OCP, OTP and etc.

Main Control Loop

The device implements an adjustable fixed frequency with peak current-mode control which offers an excellent performance over various line and loading. During normal operation, the internal high-side power switch is turned on by the internal oscillator initiating. Current in the inductor increases until the high-side switch current reaches the current reference converted by the output voltage V_{COMP} of the error amplifier. The error amplifier adjusts its output voltage by comparing the feedback signal from a resistive voltage divider on the FB pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier increases its current reference until the average inductor current matches the new load current. When the high-side power MOSFET turns off, the low-side synchronous power switch (N-MOSFET) turns on until the beginning of the next clock cycle.

VIN and PVIN Pins

The VIN and PVIN pins can be used together or separately for a variety of applications. In this device, the VIN pin is an input for supplying internal reference and control circuitry and the PVIN pin is an input for providing main power to device system and internal high-side power MOSFET. When the VIN and PVIN pins are tied together, both pins can operate from 4.5V to 18V. When the VIN and PVIN pins are used separately, VIN pin must be ranged from 4.5V to 18V, and the PVIN pin can be applied down to as low as 1.6V to 18V.

The device incorporates an internal under-voltage lockout (UVLO) circuitry on the VIN pin. If the VIN pin voltage exceeds the UVLO rising threshold voltage 4V, the converter resets and prepares the PWM for operation. If the VIN pin voltage falls below the falling threshold voltage 3.85V during normal operation, the device is disabled. Such wide internal UVLO hysteresis of 150mV can efficiently prevent noise caused reset. There is also an external UVLO circuitry which can be achieved by configuring a resistive voltage divider on EN pin for both input VIN and PVIN pins and it is able to provide either input pins an adjustable UVLO function to ensure a proper power up behavior. More discussions are located in the section of Enable Operation.

Output Voltage Setting

The resistive voltage divider allows the FB pin to sense the output voltage as shown in Figure 1.

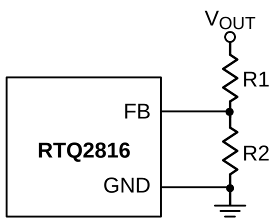


Figure 1. Setting the Output Voltage

For high efficiency, the divider resistance must adopt larger values, but too large values may induce noises and voltage errors by the coupled FB pin input current. It is recommended to use the values between 10kΩ and 100kΩ. The output voltage is set by an external resistive voltage divider according to the following Equation (1) :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right) \quad (1)$$

where V_{REF} is the feedback reference voltage (0.8V typ.).

Soft-Start

The device contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing is programmed by the external capacitor between SS/TR pin and GND. The device provides an internal 2μA charge current for the external capacitor. If a 10nF capacitor is used to set the soft-start, the period can be 4ms. The calculations for external charge capacitor C_{SS} and soft-start time T_{SS} are shown in Equation (2) :

$$T_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (2)$$

where C_{SS} is the external soft-start capacitor, I_{SS} is the soft-start charge current (2μA), V_{REF} is the feedback reference voltage (0.8V).

Once the input voltage falls below UVLO threshold, the EN pin is pulled low, or the OTP is triggered, the device stops switching and the SS/TR pin starts to discharge. It is held such shutdown condition until the event is cleared and the SS/TR pin has already discharged to ground ensuring proper soft-start behavior.

During the pre-biased start-up sequence, the output of device is not discharged by low-side power switch because the device is designed to prevent low-side MOSFET sinking. It is allowed to sink when the SS/TR pin exceeds 2.1V.

Slope Compensation

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the peak inductor current is remained constant under the whole duty cycle range when slope compensation is added. For the device, separated inductor current signal is used to monitor over-current condition, so the maximum output current stays relatively constant regardless of duty cycle. More discussions about over-current protection are described in a later section.

Enable Operation

The EN pin is an device enable input. Pulling the EN pin to logic low that is typically less than the set threshold voltage 1.17V, the device shuts down and enters to low quiescent current state about 2μA. The regulator starts switching again once the EN pin voltage exceeds the threshold voltage 1.21V. In additional, the EN pin is implemented with an internal pull-up current source which allows to enable the device when the EN pin is floating. For general external timing control, the EN pin can be externally pulled high by adding a capacitor and a resistor from the VIN pin as Figure 2.

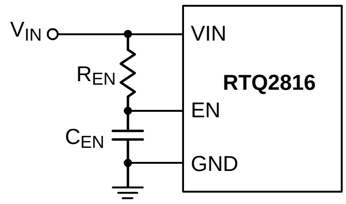


Figure 2. Enable Timing Control

An external MOSFET can be added to implement digital control from the EN pin to ground, as shown in Figure 3. In this case, there is no need to connect a pull-up resistor between the VIN and EN pins since the EN pin is pulled up by the internal current source. The device can simply achieve the digital control only through an external MOSFET on EN pin.

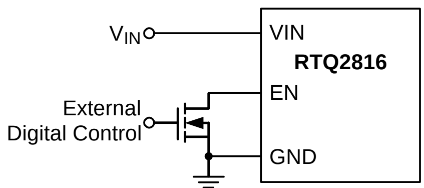


Figure 3. Digital Enable Control

The EN pin can also be applied to adjust its under-voltage lockout (UVLO) threshold with two external resistors divider from the both input VIN and PVIN pins used together or separately, and the application structures can refer to Figure 4, Figure 5, and Figure 6.

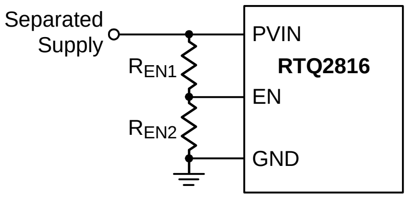


Figure 4. Resistor Divider for PVIN UVLO Setting

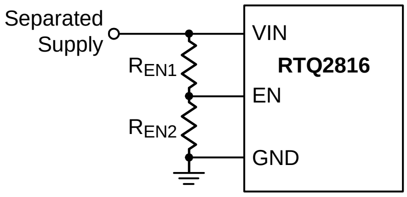


Figure 5. Resistor Divider for VIN UVLO Setting, VIN ≥ 4.5V

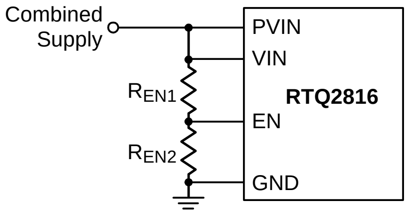


Figure 6. Resistor Divider for PVIN and VIN UVLO Setting

Under above application structures, the adjustable UVLO function of EN pin allows to achieve a secondary UVLO on PVIN pin, a higher UVLO on VIN pin or even a common UVLO on both VIN and PVIN pins. For example, if the EN pin is configured as Figure 5 and the output voltage is set to a higher value 10V. The device may shut down after soft-start sequence is over, and the reason for the result is that the V_{OUT} is still lower than its set target during the V_{IN} rising period even though V_{IN} has already risen to its internal UVLO threshold 4V. To prevent this situation, an adjustable UVLO threshold from EN pin is useful to avoid such high output transfer condition. The exact UVLO thresholds can be calculated by Equation (3). The setting V_{OUT} is 10V and V_{IN} is from 0V to 18V. When V_{IN} is higher than 12V, the device is triggered to enable the converter. Assume R_{EN1} = 56kΩ. Then,

$$R_{EN2} = \frac{R_{EN1} \times V_{IH}}{V_{IN\_S} - V_{IH}} \qquad (3)$$

where V_{IH} is the typical threshold of enable rising (1.21V) and V_{IN_S} is the target turn on input voltage (12V in this example). According to the equation, the suggested resistor R_{EN2} is 6.28kΩ.

Adjustable Operating Frequency-RT Mode

Selection of the operating frequency is a tradeoff between efficiency and component size. Higher operating frequency allows the use of smaller inductor and capacitor values but it may press the minimum controllable on-time to affect devices stability. Lower operating frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and capacitance to maintain low output ripple voltage.

The operating frequency of the device is determined by an external resistor R_{OSC}, that is connected between the RT/SYNC pin and ground. The value of the resistor sets the ramp current which is used to charge and discharge an internal timing capacitor within the oscillator. The practical switching frequency ranges from 200kHz to 1.6MHz. Determine the R_{OSC} resistor value by examining the curve in Figure 7.

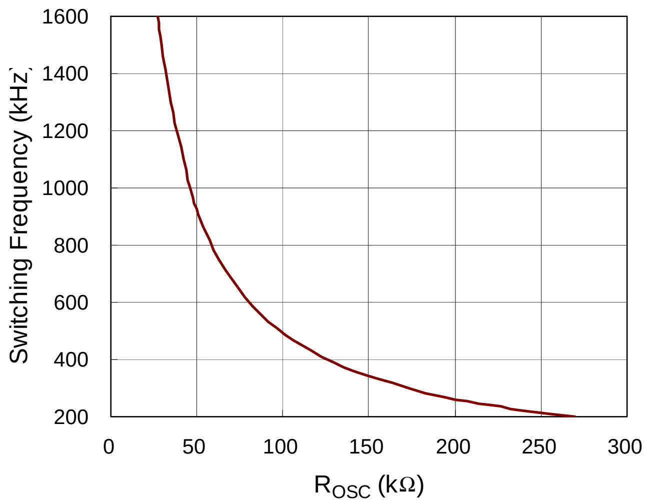


Figure 7. Switching Frequency vs. R_{OSC} Resistor

Synchronization-SYNC Mode

The device is allowed to synchronize with an external square wave clock ranging from 200kHz to 1.6MHz applied to the RT/SYNC pin. The range of sync duty cycle must be from 20% to 80%, and the amplitude of sync signal must be higher than 2V and lower than 0.8V. During the SYNC mode operation, the switching cycle of LX pin is synchronized to the falling edge of the external sync signal.

Before the external sync signal is provided to the RT/SYNC pin, the device operates at the original switching frequency set by resistor R_{OSC}. When the sync signal is provided, the SYNC mode overrides the RT mode to force the device synchronizing to external frequency. This IC can easily switch between RT mode and SYNC mode, and the application structure can be configured as Figure 8.

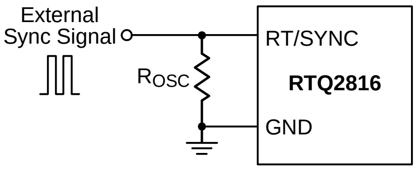


Figure 8. External Sync Signal Control

Power Good Output

The power good output is an open-drain output and needs to connect a voltage source below 5.5V with a pull-up resistor for avoiding the PGOOD floating. When the output voltage is 9% above or 9% below its set voltage, PGOOD is pulled low. It is held low until the output voltage returns within the allowed tolerances ±6% once more. During soft-start, PGOOD is actively held low when V_{IN} is greater than 1V and is only allowed to be high when soft-start period is over that means the SS/TR pin exceeds 2.1V typically and the output voltage reaches 94% of its set voltage. Besides, the PGOOD pin is also pulled low when the input UVLO or OVP are triggered, EN pin is pulled below 1.21V or the OTP is occurred.

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the gate driver voltage for the high-side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RTQ2816. Note that the external boot voltage must be lower than 5.5V.

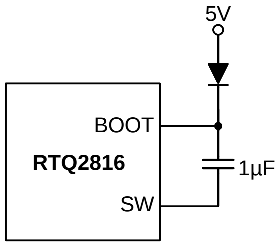


Figure 9. External Bootstrap Diode

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \quad (4)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. Highest efficiency operation is achieved by reducing ripple current at low frequency, but it requires a large inductor to attain this goal.

For the ripple current selection, the value of ΔI_L = 0.24 (I_{MAX}) is a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right] \quad (5)$$

In this device, 3.7µH is recommended for initial design. The current rating of the inductor (caused a 40°C temperature rising from 25°C ambient) must be greater than the maximum load current and ensure that the peak current does not saturate the inductor during short-circuit condition. Referring the Table 1 for the inductor selection reference.

Table 1. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4
WE	744325	10.2 x 10.2 x 4.7
WE	744355	12.8 x 12.8 x 6.2

Input and Output Capacitors Selection

The input capacitance C_{IN} is needed to filter the trapezoidal current at the Source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by Equation (6) :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \quad (6)$$

The formula above has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, Two 10µF and one 4.7µF low ESR ceramic capacitors are recommended for bypassing the PVIN pin and VIN pin respectively and an additional 0.1µF is recommended to place as close as possible to the IC input side for high frequency filtering. All the recommended input and output capacitors can refer to Table 2 for more detail.

Table 2. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (µF)	Case Size
C_{IN}	MURATA	GRM32ER71C226M	22	1210
C_{IN}	TDK	C3225X5R1C226M	22	1210
C_{OUT}	MURATA	GRM31CR60J476M	47	1206
C_{OUT}	TDK	C3225X5R0J476M	47	1210
C_{OUT}	MURATA	GRM32ER71C226M	22	1210
C_{OUT}	TDK	C3225X5R1C226M	22	1210

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple ΔV_{OUT} is determined by Equation (7) :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right] \quad (7)$$

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Level Frequency Shift

While the FB pin drops, switching frequency is proportional to the feedback voltage, this is a level frequency reduced function which is implemented in the device. For the same short-circuit example, when the output voltage drops during over-current condition, the switching frequency is reduced in direct proportion to the output voltage, so the low-side MOSFET is turned off long enough to reduce the inductor current to prevent a current runaway issue. With function of level frequency reducing, the switching frequency can reduce from 100%, 50%, then 25% as the voltage decreases from 0.8V to 0V on FB pin. The principle of level frequency reducing is also allowed to cover the soft-start sequence to increase the switching frequency as feedback voltage increases from 0V to 0.8V.

Output Over-Voltage Protection

The device provides an output over-voltage protection (OVP) once the output voltage exceeds 109% of V_{OUT}, the OVP function turns off the high-side power MOSFET to stop current flowing to the output which can only be released when the output voltage drops below 106% of V_{OUT}. There is a 5μs delay also built into the over-voltage protection circuit to prevent false transition. Using this OVP feature can easily minimize the output overshoot.

High-Side MOSFET Over-Current Protection

The over-current protection (OCP) of high-side MOSFET is implemented in this device, it adopts monitoring inductor current during the on-state to control the COMP pin voltage for turning off the high-side MOSFET. Each cycle the separated inductor current signal is compared through sensing the external inductor current to the COMP pin voltage from an error amplifier output. If the separated inductor current peak value exceeds the set current limit threshold, the high-side power switch is turned off.

Low-Side MOSFET Over-Current Protection

The device not only implements the high-side over-current protection but also provides the over sourcing current protection and over sinking current protection for low-side MOSFET. With these three current protections, the IC can easily control inductor current at both side power switches and avoid current runaway for short-circuit condition.

For the sourcing current protection, there is a specific comparator in internal circuitry to compare the low-side MOSFET sourcing current to the internal set current limit at the end of every clock cycle. When the low-side sourcing current is higher than the set sourcing limit, the high-side power switch is not turned on and low-side power switch is kept on until the following clock cycle for releasing the above sourcing current to the load. It is allowed to turn on the high-side MOSFET again when the low-side current is lower than the set sourcing current limit at the beginning of a new cycle.

For the sinking current protection, it is implemented by detecting the voltage across the low-side power switch. If the low-side reverse current exceeds the set sinking limit, both power switches are off immediately, and it is held to stop switching until the beginning of next cycle. By incorporating this additional protection, the device is able to prevent an excessive sinking current from the load during the condition of pre-biased output and the SS/TR pin is asserted high that is 2.1V or above.

Over-Temperature Protection

An over-temperature protection (OTP) is contained in the device. The protection is triggered to force the device shutdown for protecting itself when the junction temperature exceeds 175°C typically. Once the junction temperature drops below the hysteresis 10°C typically, the device is re-enable and automatically reinstates the power up sequence.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-14AL 3.5x3.5 package, the thermal resistance, θ_{JA}, is 48°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (48°C/W) = 2.083W for a WQFN-14AL 3.5x3.5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

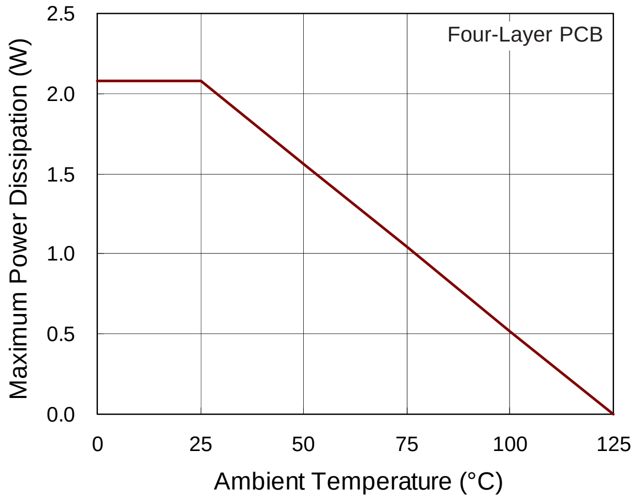


Figure 10. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to VIN and PVIN pins.
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the device.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 11 for reference.

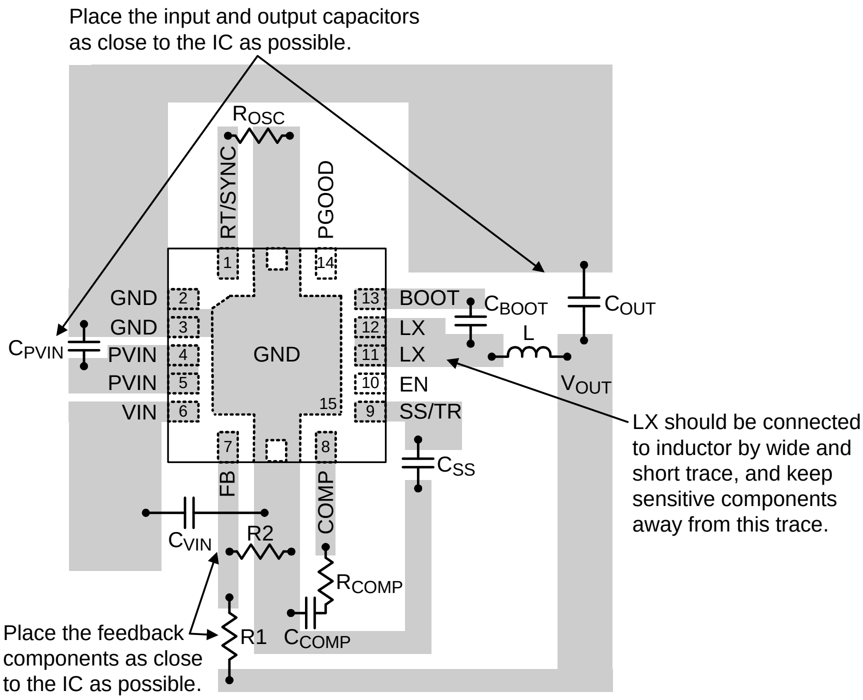
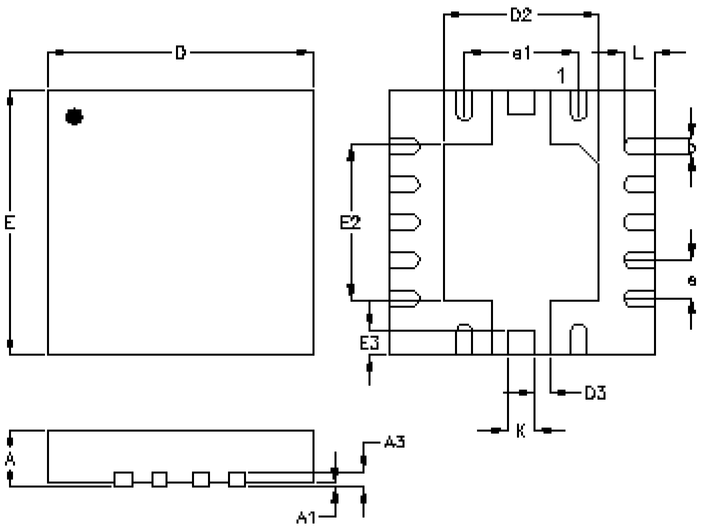
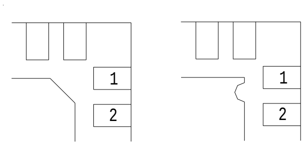


Figure 11. PCB Layout Guide

Outline Dimension





DETAIL A

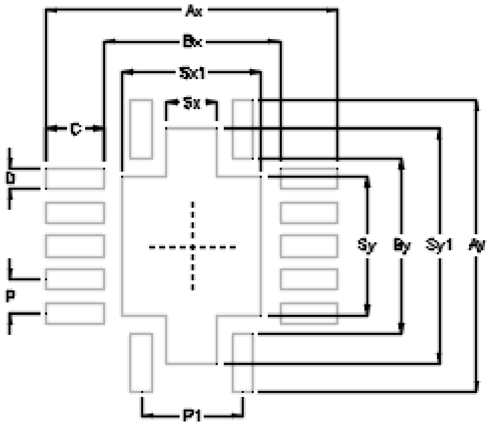
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.000	2.100	0.079	0.083
D3	0.200		0.008	
E	3.400	3.600	0.134	0.142
E2	2.000	2.100	0.079	0.083
E3	0.325		0.013	
e	0.500		0.020	
e1	1.500		0.059	
K	0.350		0.014	
L	0.350	0.450	0.014	0.018

W-Type 14AL QFN 3.5x3.5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)												Tolerance
		P	P1	Ax	Ay	Bx	By	C	D	Sx	Sx1	Sy	Sy1	
V/W/U/XQFN3.5*3.5-14A	14	0.50	1.50	4.30	4.30	2.60	2.60	0.85	0.30	0.75	2.05	2.05	3.50	±0.05

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