Peak 15A, 17V, High Efficiency Synchronous Step-Down Converter

General Description

The RTQ2822T is a high-performance, synchronous step-down converter that can deliver up to 15A output current with an input supply voltage range of 4.5V to 17V. The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate 0.6V reference and an integrated diode for bootstrap circuit to offer a very compact solution.

The RTQ2822T adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultrafast transient response and further reduces the external-component count. In steady state, the ACOT® operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

The device offers a variety of functions for more design flexibility. The selectable switching frequency, current limit level and PWM operation modes makes the RTQ2822T easy-to-use over wide application range. Independent enable control input pin and power good indicator are also provided for easy sequence control. To control the inrush current during the startup, the device provides a programmable soft start-up by an external capacitor connected to the SS pin. Fully protection features are also integrated in the device including the cycle-by-cycle current limit, UVP, input UVLO and OTP.

The RTQ2822T is available in a thermally enhanced VQFN-18L 3.5x3.5 (FC) package.

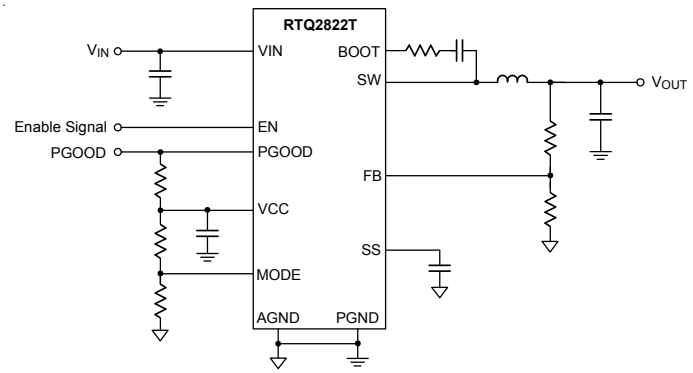
Features

- **4.5V to 17V Input Voltage Range**
- **Integrated 9.8mΩ/4.5mΩ MOSFETs**
- **0.6V ±1% Voltage Reference**
- **Adjustable Output Voltage from 0.6V to 5.5V**
- **Supports Ceramic Output Capacitor**
- **ACOT® Control for Fast Transient Response**
- **Selectable Switching Frequency (400kHz/800kHz/1200kHz)**
- **Selectable Current Limit Level**
- **Power Good Indicator**
- **Programmable Soft-Start Time with a Default 1.2ms**
- **Monotonic Start-Up into Pre-Biased Outputs**
- **18-Lead VQFN (FC) Package**

Applications

- Server, Storage and Network Equipment
- Telecom Infrastructure
- Point of Load (POL) Power Modules
- High Density DC-DC Converters
- High End Digital TV

Simplified Application Circuit



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Ordering Information

RTQ2822T □□

- Package Type
  QVF : VQFN-18L 3.5x3.5 (FC) (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Enable Pin
  T : Internal Pull Low

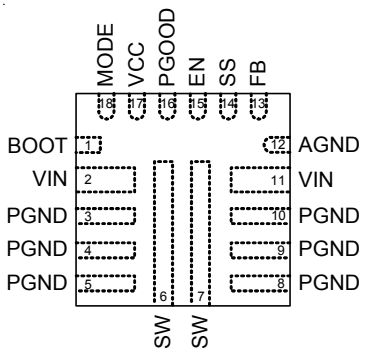
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

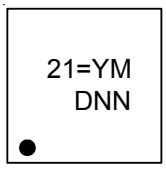
Pin Configuration

(TOP VIEW)



VQFN-18L 3.5x3.5 (FC)

Marking Information



21= : Product Code

YMDNN : Date Code

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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap, supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between the BOOT and SW pins.
2, 11	VIN	Input voltage. Support 4.5V to 17V input voltage. It is suggested to place equal-value input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
3, 4, 5, 8, 9, 10	PGND	System GND. The power GND of the controller circuit and the regulated output voltage. Use wide PCB traces to make the connections. The AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
6, 7	SW	Switch node. Connect to the power inductor.
12	AGND	Analog GND. The AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
13	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. Suggest to place the FB resistor divider as close to FB pin and AGND as possible.
14	SS	Soft-start time control pin. Connect a capacitor between the SS pin and AGND to set the soft-start time. The default internal start-up time is 1.2ms without external capacitor.
15	EN	IC enable.
16	PGOOD	Open-drain, power-good indication output. It is pulled low if the feed-back voltage is out of PGOOD threshold, IC shutdown from OTP and EN goes low, and before the soft-start is finished. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.
17	VCC	4.7V internal LDO output. Connect a 10μF capacitor as close to the VCC pin as possible. It is not recommend to connect VCC to supply others rails.
18	MODE	Switching frequency, current limit selection and light load operation mode selection pin. Connect this pin to a resistor divider from VCC and AGND for different MODE options.

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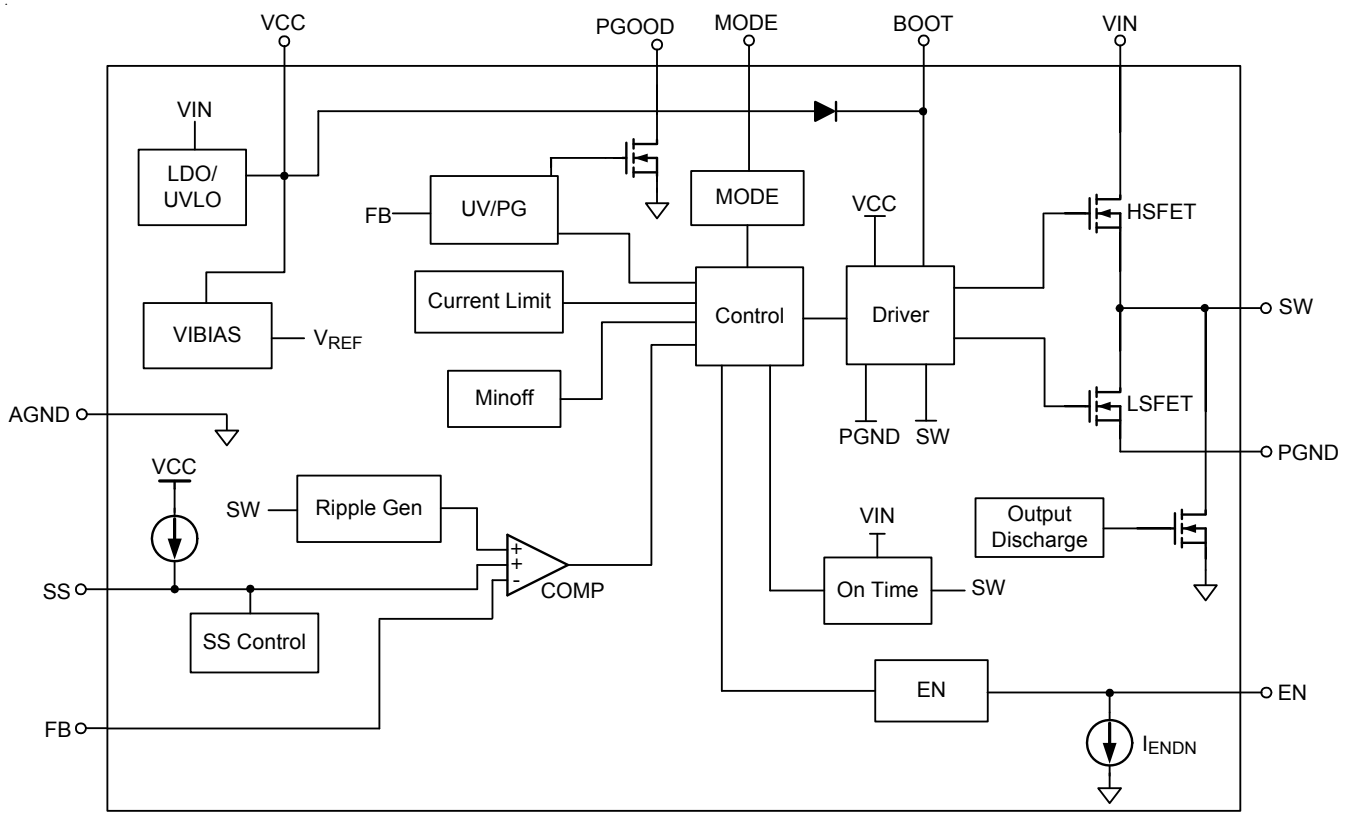
Functional Block Diagram



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Operation

The RTQ2822T is a high efficiency synchronous step-down converter utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture. The ultrafast ACOT® control enables the use of small capacitance to save the PCB size.

During normal operation, the internal high-side power switch (HSFET) turns on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the HSFET turns off, the low-side power switch (LSFET) turns on. Due to the output capacitor ESR, the voltage ripple on the output has similar shape as the inductor current. Via the feedback resistor network, this voltage ripple is compared with the internal reference. When the minimum off-time one-shot (310ns, max.) has timed out and the inductor current is below the current limit threshold, the one-shot is triggered again if the feedback voltage falls below the feedback reference voltage (0.6V, typ.). To achieve stable operation with low-ESR ceramic output capacitors, an internal ramp signal is added to the feedback reference voltage to simulate the output voltage ripple. The ACOT® control architecture features ultrafast transient response. When a load is suddenly increased, the output voltage drops quickly, and almost immediately, a new on-time is triggered and inductor current rises again.

The traditional COT controller implements the on-time to be inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. However, even with defined input and output voltages, a fixed ON time means that frequency has to increase at higher load levels to compensate for the power losses in the MOSFETs and Inductor. The ACOT® control further adds a frequency locked loop system, which slowly adjusts the ON time to compensate the power losses without influencing the fast transient behavior of the COT topology.

Power and Bias Supply

The VIN pins on the RTQ2822T are used to supply voltage to the drain terminal of the internal HSFET. These pins also supply bias voltage for an internal regulator that generates 4.7V at VCC. The voltage on VCC pin is used for internal chip bias and gate drive for the LSFET. The gate drive for the HSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins, which is charged by an internal synchronous diode from VCC. In addition, an internal charge pump maintains the C_{BOOT} voltage is sufficient to turn-on the HSFET.

To improve efficiency and limit power dissipation in the VIN, an external voltage that is above the LDO's internal output voltage can override the internal LDO. When using an external bias on the VCC rail, any power-up and power-down sequencing can be applied. However, it is important to understand that if there is a discharge path on the VCC rail that can pull a current higher than the internal LDO's current limit from the VCC, then the VCC drops below the UVLO falling threshold and thereby shut down the output of the RTQ2822T.

Enable, Start-Up, Shutdown and UVLO

The RTQ2822T implements Under-Voltage Lock Out protection (UVLO) to prevent operation without fully turn-on the internal power MOSFETs. The UVLO monitors the internal VCC regulator voltage. When the VCC voltage is lower than UVLO threshold voltage, the device stops switching. The UVLO is a non-latching protection.

The EN pin is provided to control the device turn-on and turn-off. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching. When the EN pin voltage falls below the turn-off threshold (V_{ENL}), it stops switching. The RTQ2822T internally week pull-down the EN pin.

When appropriate voltages are presented on the VIN, VCC, and EN pins, the RTQ2822T will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp of 1.2ms will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The 6μA current that is sourced from the SS pin will create a smooth voltage ramp on the capacitor. If this external ramp rate is slower than the internal 1.2ms soft-start, the output voltage will be limited by the ramp rate on the SS pin instead. Once both of the external and internal soft-start ramps have exceeded 0.7V,

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the output voltage will be in regulation. The typical external soft-start time can be calculated by the equation below.

$$C_{SS}\,(nF) = \frac{t_{SS}\,(ms) \times I_{SS}\,(\mu A)}{V_{REF}\,(V)}$$

where I_{SS} = 6μA, V_{REF} = 0.6V

When the V_{EN} is lower than V_{ENL}, the SS pin voltage is reset to GND.

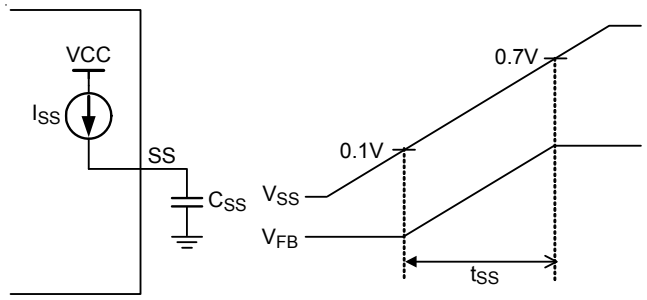

Figure 1. External Soft-Start Time Setting

Figure 2 below shows the typical power-up sequence of the device when the EN pin voltage crosses the EN Input rising threshold. After the voltage on VCC pin crosses the UVLO rising threshold it takes 400μs to read the first MODE setting and approximately 55μs from there to finish the last MODE setting. The output voltage starts ramping after the MODE setting reading is completed.

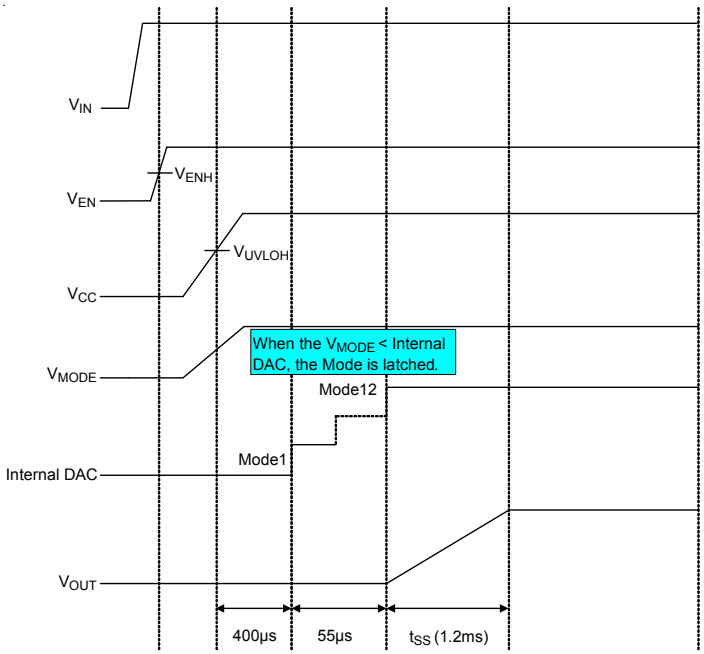

Figure 2. Power Up Sequence

Pre-Bias

If there is a residual voltage on output voltage before start-up, both of the internal HSFET and LSFET are prohibited switching until the soft-start ramp is higher than feedback voltage. When the soft-start ramp is higher than the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated target.

Mode Selection for Light Load Operation, Switching Frequency and Current Limit

The MODE pin offers 12 different states of operation as a combination of Light Load operation, Switching Frequency and Current Limit. As shown in the Figure 3, use a resistor divider from VCC to AGND can set the MODE pin voltage. It is important that the voltage for the MODE pin is derived from the VCC rail only since internally this voltage is referenced to detect the MODE option. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in Table 1. The MODE pin setting can be reset only by a VIN power cycling. The two resistors (R_{M1} and R_{M2}) are suggested to use 1% resistors.

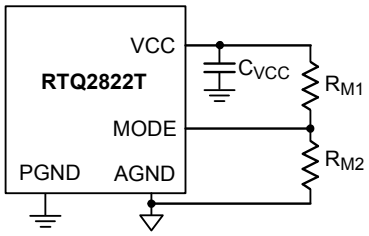

Figure 3. MODE Connection

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Table 1. MODE Setting

Mode	R_{M1} (kΩ)	R_{M2} (kΩ)	Light Load Mode	Current Limit	Switching Frequency (kHz)
1	300	5.1	FCCM	I_{LIM_2}	400
2	200	10	FCCM	I_{LIM_1}	400
3	160	20	FCCM	I_{LIM_2}	800
4	120	20	FCCM	I_{LIM_1}	800
5	200	51	FCCM	I_{LIM_2}	1200
6	180	51	FCCM	I_{LIM_1}	1200
7	150	51	DCM	I_{LIM_2}	400
8	120	51	DCM	I_{LIM_1}	400
9	91	51	DCM	I_{LIM_2}	800
10	82	51	DCM	I_{LIM_1}	800
11	62	51	DCM	I_{LIM_2}	1200
12	51	51	DCM	I_{LIM_1}	1200

Light Load Operation

At low load current, the inductor current can drop to zero and become negative. This is detected by internal zero-current-detect circuitry which utilizes the LSFET $R_{DS(ON)}$ to sense the inductor current. The LSFET is turned off when the inductor current drops to zero, resulting in discontinuous operation (DCM). Both power MOSFETs will remain off with the output capacitor supplying the load current until the feedback voltage falls below the feedback reference voltage. DCM operation maintains high efficiency at light load, while setting MODE to Forced PWM (FCCM) operation helps meet tight voltage regulation accuracy requirements.

Switching Frequency, Minimum On-Time and Minimum Off-Time

The RTQ2822T offers three different switching frequency of 400kHz, 800kHz and 1200kHz by setting the MODE pin voltage. Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

An additional constraint on operating frequency is the minimum controllable on-time and off-time. The minimum on-time is the smallest duration of time in which the high-side power MOSFET (HSFET) can be in its "on" state. This time is typically 54ns. In continuous mode operation, the minimum duty cycle can be estimated by ignoring component losses as follows :

$$D_{MIN} = f_{SW} \times t_{ON_MIN}$$

where t_{ON_MIN} is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RTQ2822T is capable of turning on the low-side power MOSFET (LSFET), tripping the current comparator and turning the power MOSFET back off. This time is 310ns (max.). The minimum off-time limit imposes a maximum duty cycle of t_{ON} /(t_{ON} + t_{OFF_MIN}).

Current Limit and Output Under-Voltage Protection

As shown in Table 1, the RTQ2822T can operate at two different current limits I_{LIM_1} and I_{LIM_2} to support an output peak current of 15A and 13A respectively. The device cycle-by-cycle compares the valley current of the inductor against the current limit threshold. Hence, the output current will be half of the ripple current higher than the valley current.

The inductor current level is monitored by measuring the low-side MOSFET voltage between the SW pin and GND, which is proportional to the switch current, during the on-

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time of LSFET. To improve the current measurement accuracy, temperature compensation is added internally. If the measured drain to source voltage of the LSFET is above the voltage proportional to current limit, the LSFET stays on until the current level becomes lower than the OCL level which reduces the output current availability. When the current is limited, the output voltage tends to drop because the load demand is higher than what the converter can support.

When the output voltage falls below output UVP threshold (V_{UVP}), the UVP comparator detects it and shuts down the device to avoid the excessive heat. If the UVP condition remains for a period of time, a soft-start sequence for auto-recovery will be initiated as shown in Figure 4. When the over-current condition is removed, the output voltage returns to the regulated value.

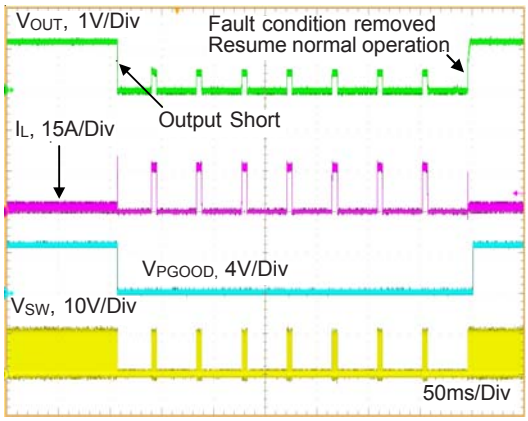

Figure 4. Current Limit and UVP

Similar to the forward over-current, the reverse current protection (NOC) is realized by monitoring the current across the low-side MOSFET. When the LSFET current reaches negative current limit, the low-side MOSFET is turned off.

Note :

(1) In order to prevent the NOC is triggered at light load operation, the inductor valley current should be designed to be higher than I_{LIM_NEG} –5A (max.) when the MODE selection is FCCM.

(2) The current limit threshold of RTQ2822T is designed for "Peak" 15A output current, when the RTQ2822T operates under heavy load, for example, continue > 12A condition, the heat dissipation capacity should be taken into account first. In order to meet the criterion of junction temperature T_J < 150°C, please refer to the section "Thermal consideration" at the beginning of design.

Power-Good Output

The PGOOD pin is an open-drain power-good indication which is connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to become high after soft-start is finished. If V_{FB} rises above a power-good threshold V_{TH_PGLH} (typically 93% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a V_{FB} falling hysteresis ΔV_{TH_PGLH} (typically 9% of the target value) or exceeds V_{FB} rising threshold V_{TH_PGHL} (typically 116% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{FB} falling hysteresis, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis ΔV_{TH_PGHL} (typically 9% of the target value). Once being started-up, if any protection is triggered (UVP and OTP) or EN is from high to low, PGOOD will be pulled to GND. The internal open-drain pull-down device with 250Ω resistance will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic VOUT changes, the RTQ2822T's PGOOD falling edge includes a blanking delay of approximately 1μs.

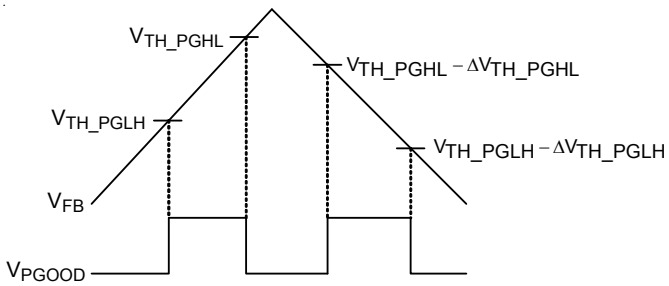

Figure 5. The Logic of PGOOD

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Over-Temperature Protection (OTP)

The RTQ2822T monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SD}, typically 160°C), the RTQ2822T stops switching, SS resets to ground, and an internal discharge switch turns on to quickly discharge the output voltage. During start-up, if the device temperature is higher than 160°C, the device does not start switching. The device re-starts switching when the temperature drops more than 15°C (typ.) but the MODE settings are not re-loaded again. If the temperature continues to rise and above LDO thermal shutdown threshold (T_{SD_LDO}, typically 171°C), the converter shuts down completely.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Output Voltage Discharge

An internal 500Ω discharge switch that discharges the V_{OUT} through SW node during fault events like UVP, OTP , VCC voltage below UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---- –0.3V to 20V
  V_{IN} (t ≤ 20ns) ---- –5V to 30V
- Enable Pin Voltage, V_{EN} ---- –0.3V to 20V
  V_{EN} (t ≤ 20ns) ---- –3V to 30V
- Switch Voltage, V_{SW} ---- –0.3V to 20V
  V_{SW} (t ≤ 100ns) ---- –5V to 25V
  V_{SW} (t ≤ 20ns) ---- –5V to 30V
- BOOT Voltage, V_{BOOT} ---- –0.3V to 26V
  V_{BOOT} (t ≤ 20ns) ---- –5V to 30V
- BOOT to SW (V_{BOOT} – V_{SW}) ---- –0.3V to 6V
  V_{BOOT} – V_{SW} (t ≤ 100ns) ---- –0.3V to 7V
  V_{BOOT} – V_{SW} (t ≤ 20ns) ---- –3V to 9V
- All Other Pins ---- –0.3V to 6V
  All Other Pins (t ≤ 20ns) ---- –3V to 8.5V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-18L 3.5x3.5 (FC) ---- 3.57W
- Junction Temperature ---- 150°C
- Lead Temperature (Soldering, 10 sec.) ---- 260°C
- Storage Temperature Range ---- –65°C to 150°C

ESD Ratings (Note 2)

- ESD Susceptibility
  HBM (Human Body Model) ---- 2kV

Recommended Operating Conditions (Note 3)

- Supply Voltage, VIN ---- 4.5V to 17V
- Junction Temperature Range ---- –40°C to 150°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		VQFN-18L 3.5x3.5 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	33.9	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	18	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	8.4	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	28	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7	°C/W

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Electrical Characteristics

(V_{IN} = 12V, T_J = –40°C to 150°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current							
Supply Current (Shutdown)	I_{SHDN}	T_J = 25°C, V_{EN} = 0V		2	7	20	μA
Supply Current (Quiescent)	I_Q	T_J = 25°C, V_{EN} = 5V, non-switching		400	600	700	μA
Logic Threshold							
EN Input Rising Threshold	V_{ENH}			1.175	1.225	1.3	V
EN Input Falling Threshold	V_{ENL}			1.025	1.104	1.15	V
EN Hysteresis	ΔV_{EN}			--	0.121	--	V
EN Pull-Down Current	I_{ENDN}	T_J = 25°C , V_{EN} = 2V		--	2.5	--	μA
V_{FB} Voltage							
FB Voltage	V_{FB}	T_J = –40°C to 125°C		0.594	0.6	0.606	V
		T_J = –40°C to 150°C		0.594	0.6	0.609	
$R_{DS(ON)}$							
High-Side Switch On-Resistance	$R_{DS(ON)_H}$	T_J = 25°C, V_{CC} = 4.7V		--	9.8	--	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)_L}$	T_J = 25°C, V_{CC} = 4.7V		--	4.5	--	mΩ
Current Limit							
Low-Side Switch Sourcing Current Limit	I_{LIM_1}	Valley current	T_J = 25°C	14	17	19.2	A
			T_J = –40°C to 150°C	13.5	--	19.7	
	I_{LIM_2}		T_J = 25°C	11.7	14	16.3	
			T_J = –40°C to 150°C	11	--	17	
Low-Side Switch Negative Current Limit	I_{LIM_NEG}	Valley current		--	--	–5	A
Switching Frequency							
Switching Frequency	f_{SW1}	T_J = 25°C, CCM		320	400	480	kHz
	f_{SW2}	T_J = 25°C, CCM		640	800	960	kHz
	f_{SW3}	T_J = 25°C, CCM		960	1200	1440	kHz
On-Time Timer Control							
Minimum On Time	t_{ON_MIN}	V_{IN} = 17V, V_{OUT} = 0.6V, f_{SW} = 1200kHz		40	54	70	ns
Minimum Off Time	t_{OFF_MIN}	T_J = 25°C, V_{FB} = 0.5V		200	--	310	ns

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft Start						
Soft-Start Time	t_{SS}	Internal soft-start time	0.4	1.2	2	ms
Soft-Start Charge Current	I_{SS}		4.9	6	7.1	μA
UVLO						
UVLO Rising Threshold	V_{UVLOH}	V_{LDO} rising	4	4.3	4.5	V
UVLO Hysteresis	ΔV_{UVLO}	V_{LDO} hysteresis	--	730	--	mV
LDO Output						
LDO Output Voltage	V_{CC}		4.58	4.7	4.83	V
LDO Output Current Limit	I_{LIM_LDO}		50	--	200	mA
Output Under-Voltage and Over-Voltage Protections						
Output UVP Threshold	V_{UVP}	UVP detect	61	68	75	$\%V_{FB}$
Power Good						
Power Good Threshold	V_{TH_PGLH}	V_{FB} rising threshold, PGOOD from low to high (GOOD)	86	93	100	$\%V_{FB}$
	ΔV_{TH_PGLH}	V_{FB} falling hysteresis, PGOOD from high to low (FAULT)	2	9	16	$\%V_{FB}$
	V_{TH_PGHL}	V_{FB} rising threshold, PGOOD from high to low (FAULT)	109	116	123	$\%V_{FB}$
	ΔV_{TH_PGHL}	V_{FB} falling hysteresis, PGOOD from low to high (GOOD)	2	9	16	$\%V_{FB}$
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	T_{HYS}		--	15	--	°C
LDO Thermal Shutdown Threshold	T_{SD_LDO}		--	171	--	°C
LDO Thermal Shutdown Hysteresis	ΔT_{SD_LDO}		--	18	--	°C

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Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 76mm x 76mm, furthermore, all layers with 2 oz. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

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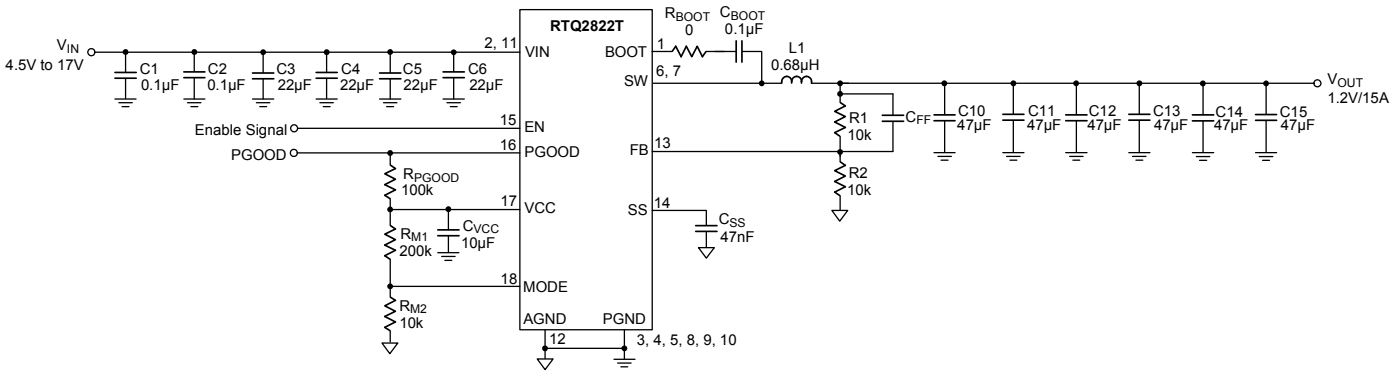
Typical Application Circuit



Note:

(1) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

Table 2. Suggested Component Selections for the Application of 400kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1(µH)	C_{OUT_MIN} (µF)	$C_{OUT_TYPICAL}$(µF)	C_{FF} (pF)
1.2	10	10	0.68	188	282	NC
3.3	45.2		1	188	282	100 to 200
5	73.2		2	188	282	100 to 200

Table 3. Suggested Component Selections for the Application of 800kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	C_{OUT_MIN} (µF)	$C_{OUT_TYPICAL}$ (µF)	C_{FF} (pF)
1.2	10	10	0.33	188	282	NC
3.3	45.2		0.68	188	282	100 to 200
5	73.2		1	188	282	100 to 200

Table 4. Suggested Component Selections for the Application of 1200kHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	C_{OUT_MIN} (µF)	$C_{OUT_TYPICAL}$ (µF)	C_{FF} (pF)
1.2	10	10	0.22	188	282	NC
3.3	45.2		0.47	188	282	100 to 200
5	73.2		0.68	188	282	100 to 200

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Table 5. Suggested Inductors for Typical Application Circuit

Inductance (μH)	Part No.	I_{SAT} (A)	DCR (mΩ)	Dimensions (mm)	Component Supplier
0.22	744316022	25	1.25	5.5x 5.5 x 4.0	WE-HCI
0.33	744316033	20	1.75	5.6 x 5.6 x 4.0	WE-HCI
0.47	744314047	20	1.35	7.0 x 7.0 x 5.0	WE-HCI
0.68	744311068	20	3.1	7.0 x 7.0 x 4.0	WE-HCI
1	744323100	21	4.79	10.6 x 10.6 x 3	WE-HCI
2	7443551200	22	2.6	13 x 13 x 6.5	WE-HCI

Table 6. Suggested Capacitor for Typical Application Circuit

Capacitance (μF)	Part No.	Case Size	Component Supplier
22	GRM21BR61E226ME44	0805	Murata
47	GRM21BR61A476ME15	0805	Murata
10	GRM188R60J106ME47	0603	Murata
0.1	C1608X7R1H104K080AA	0603	TDK

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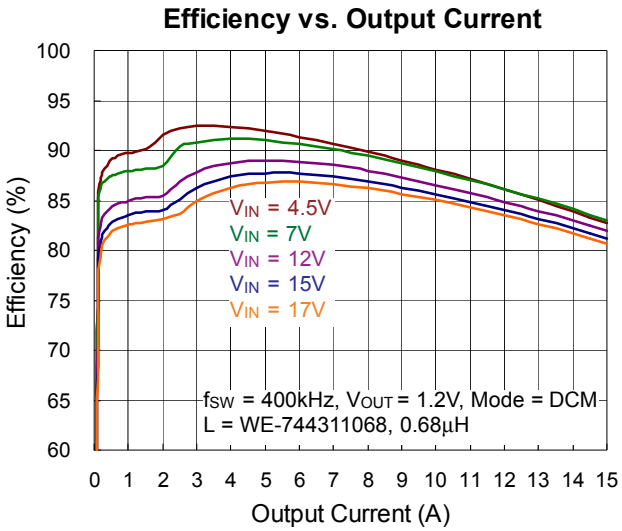
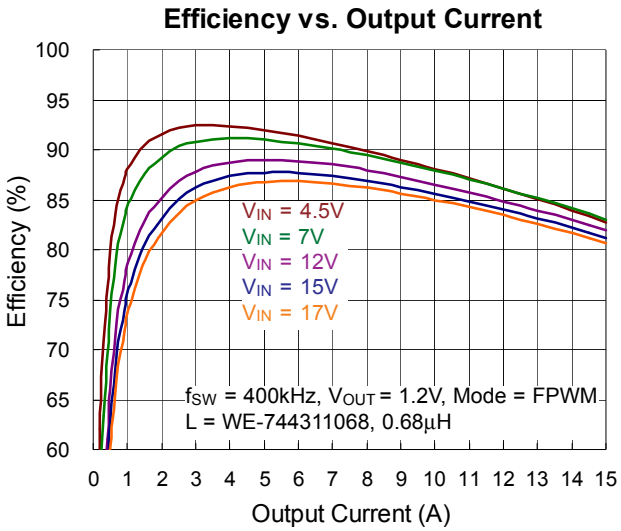
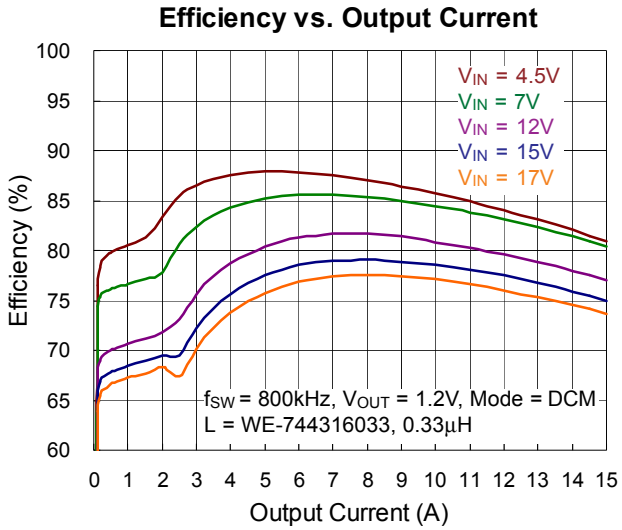
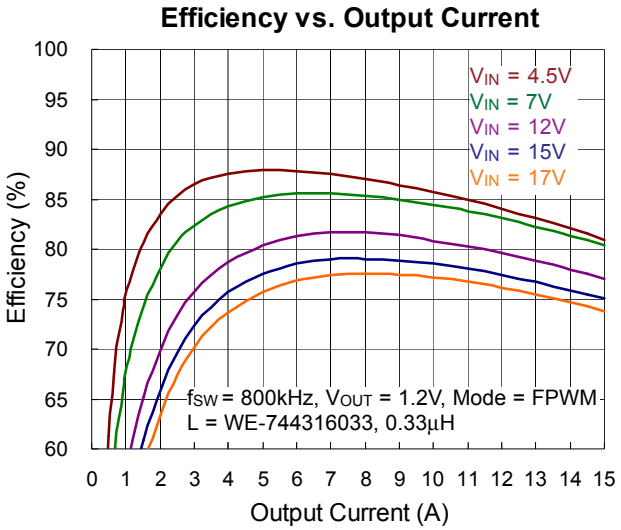
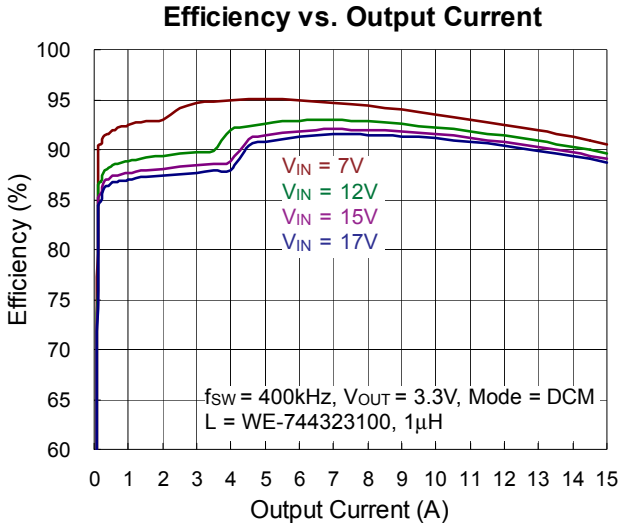
Typical Operating Characteristics

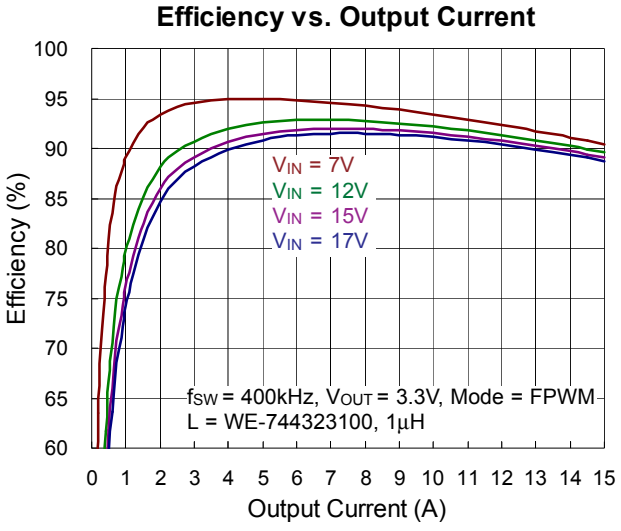












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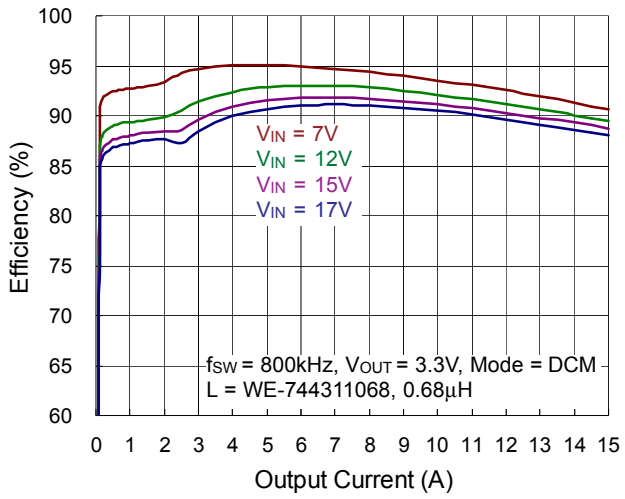
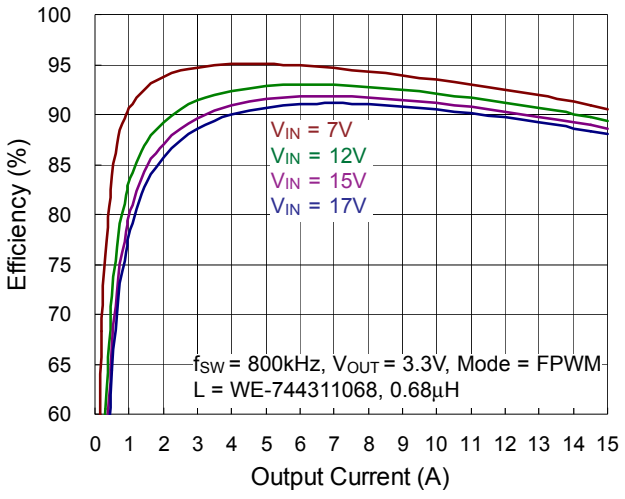
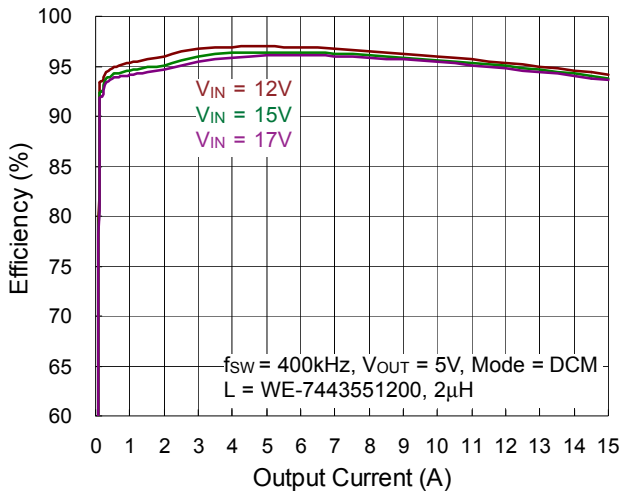
Efficiency vs. Output Current



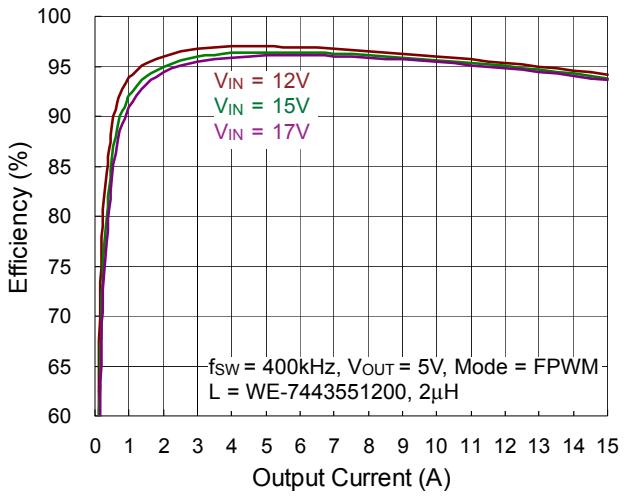
Efficiency vs. Output Current



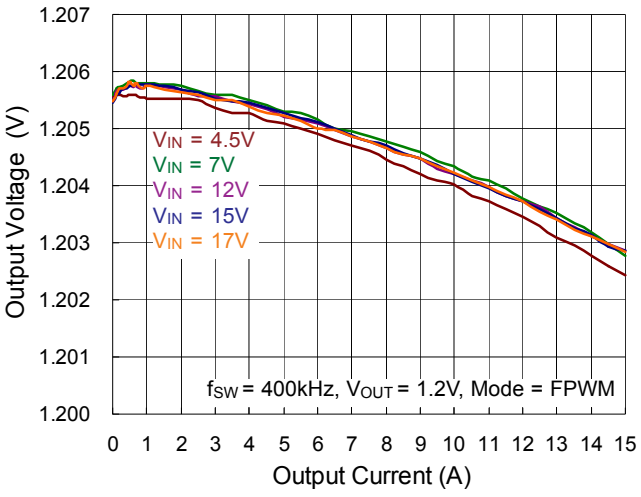
Efficiency vs. Output Current



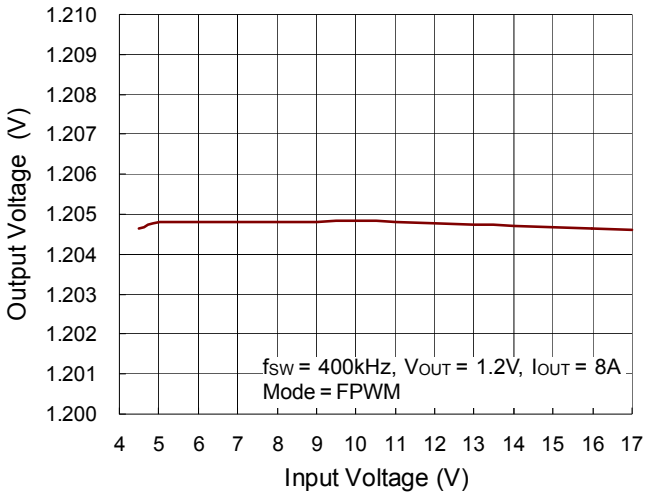
Efficiency vs. Output Current



Output Voltage vs. Output Current



Output Voltage vs. Input Voltage



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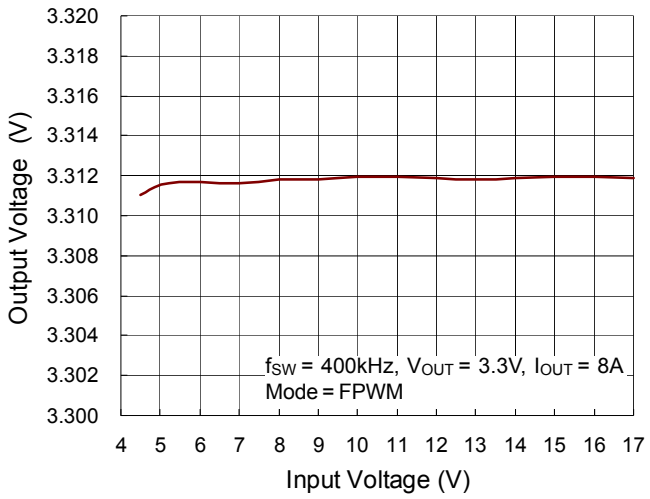
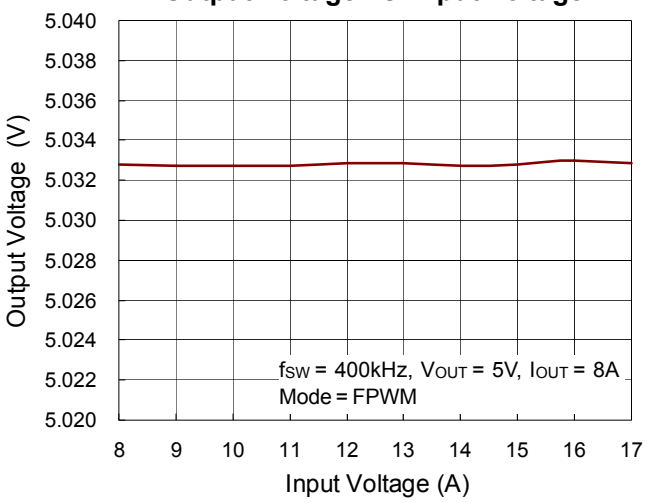
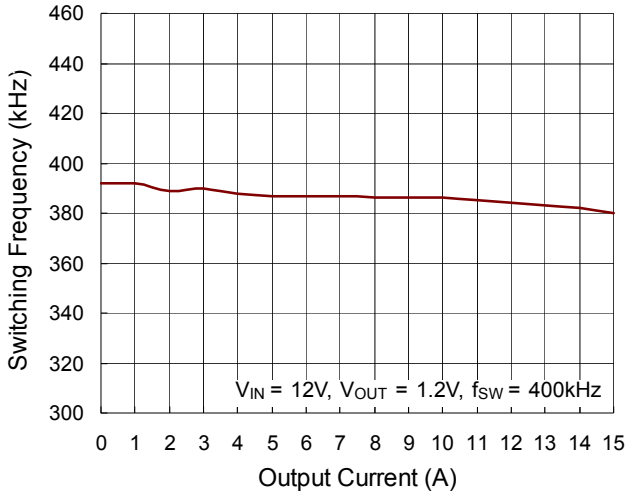
Output Voltage vs. Input Voltage



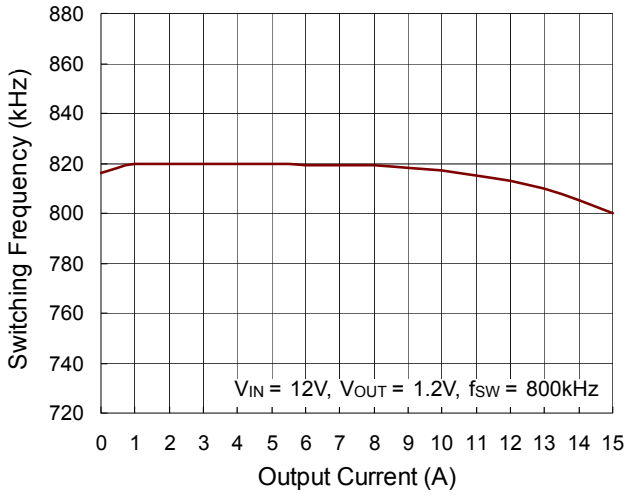
Output Voltage vs. Input Voltage



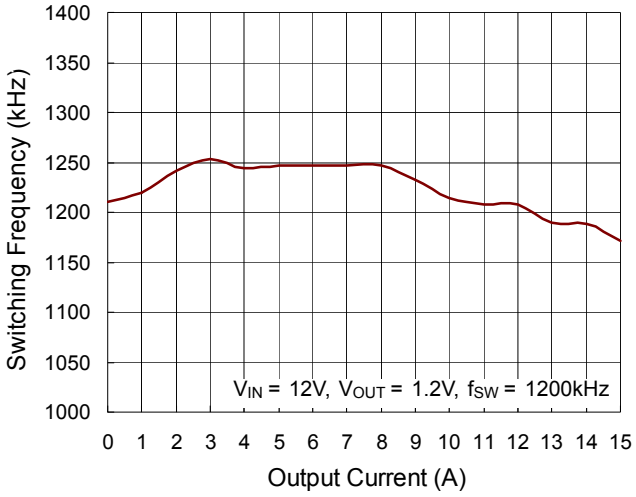
Switching Frequency vs. Output Current



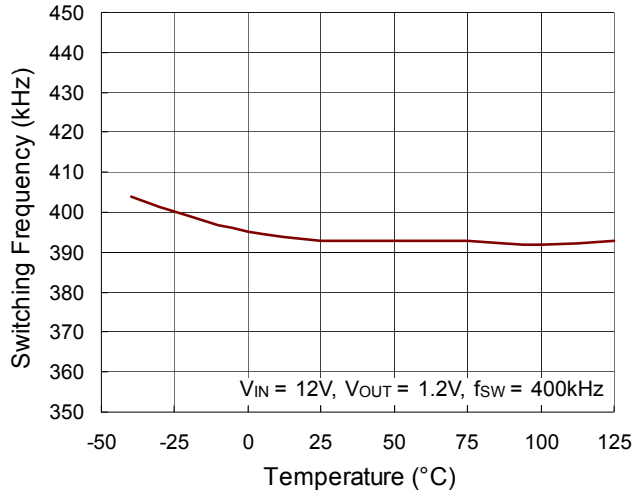
Switching Frequency vs. Output Current



Switching Frequency vs. Output Current



Switching Frequency vs. Temperature



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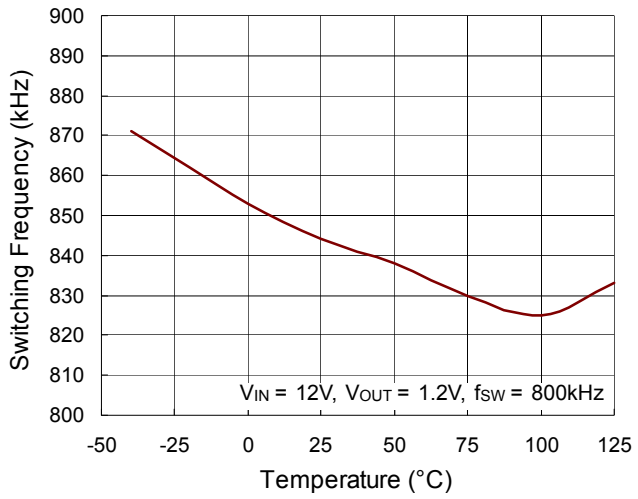
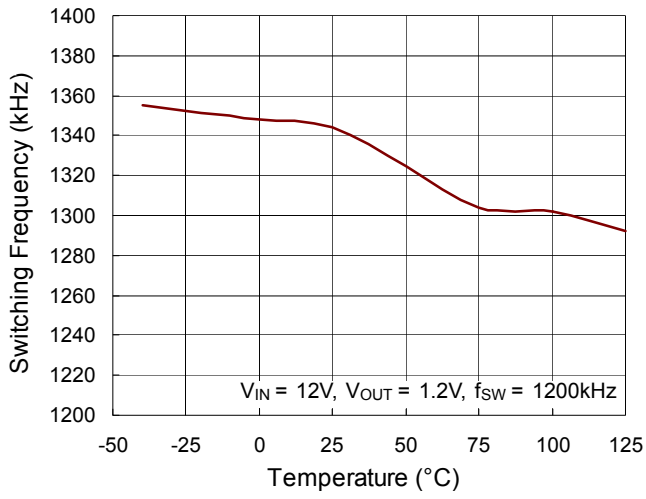
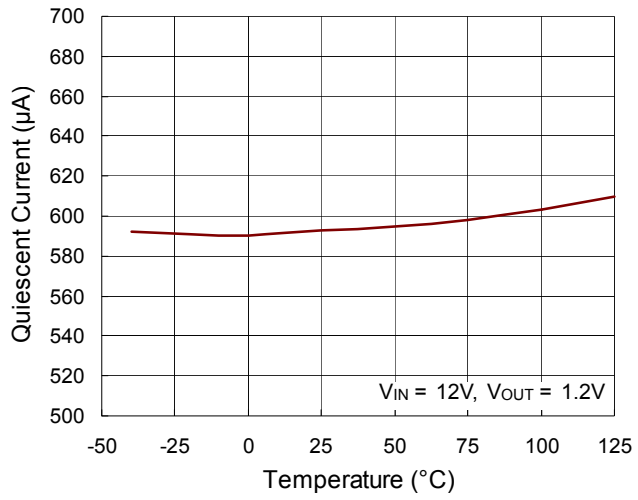
Switching Frequency vs. Temperature



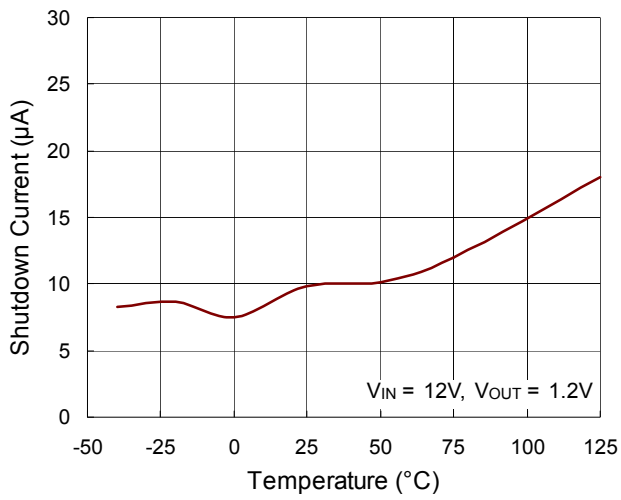
Switching Frequency vs. Temperature



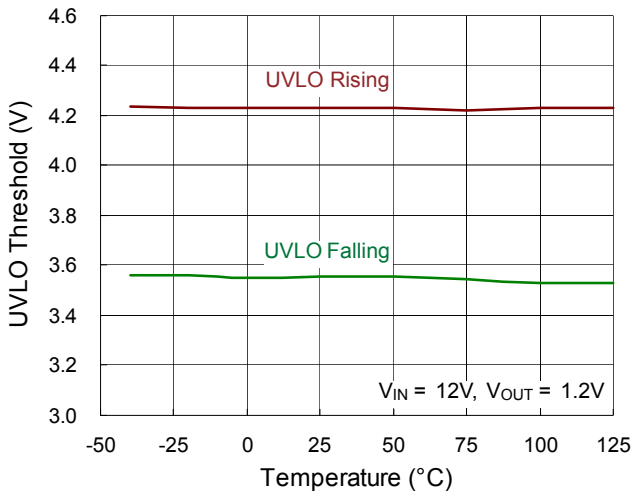
Quiescent Current vs. Temperature



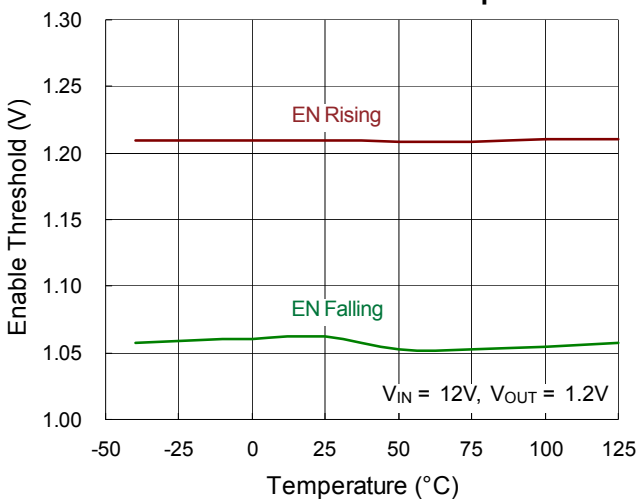
Shutdown Current vs. Temperature



UVLO Threshold vs. Temperature



Enable Threshold vs. Temperature



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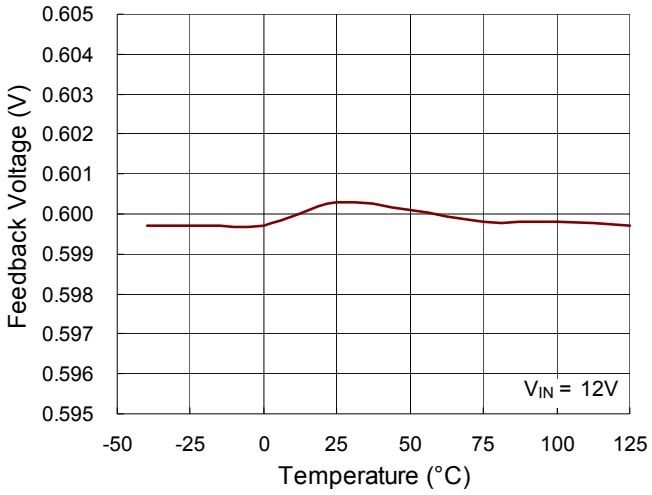
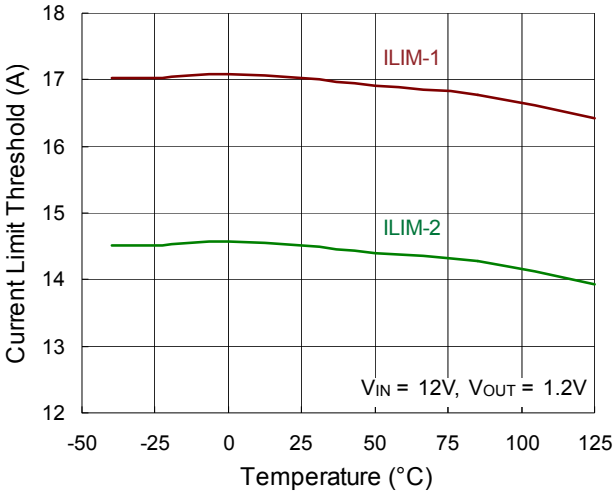
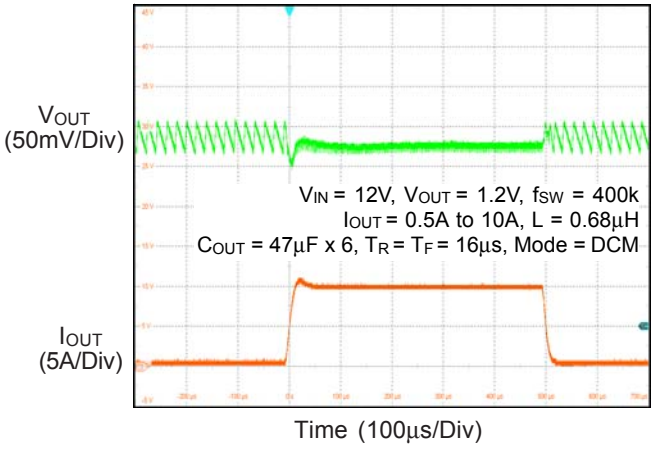
Feedback Voltage vs. Temperature



Current Limit Threshold vs. Temperature



Load Transient Response



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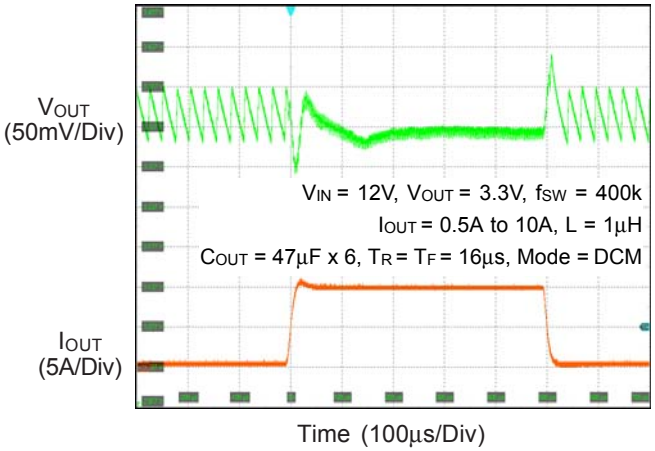

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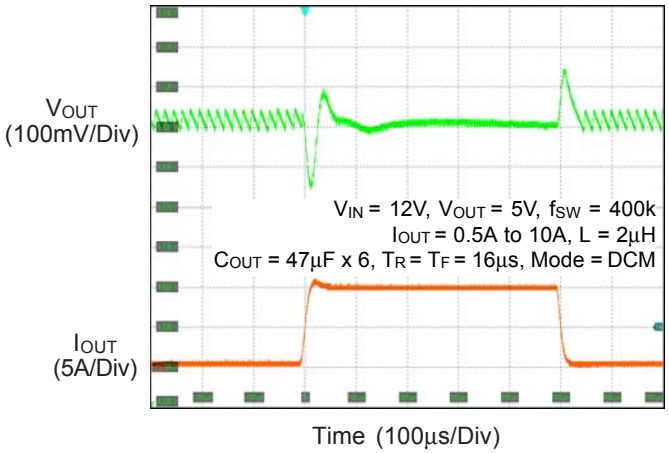
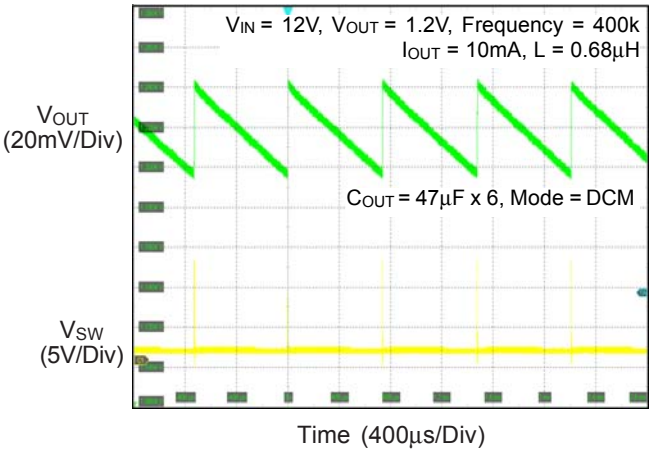


Output Ripple Voltage



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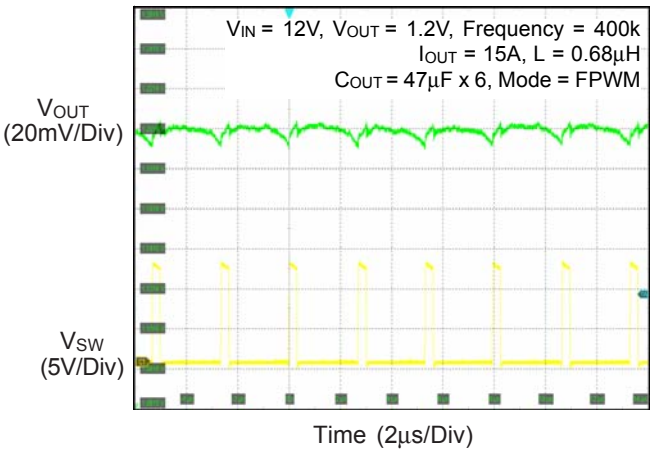
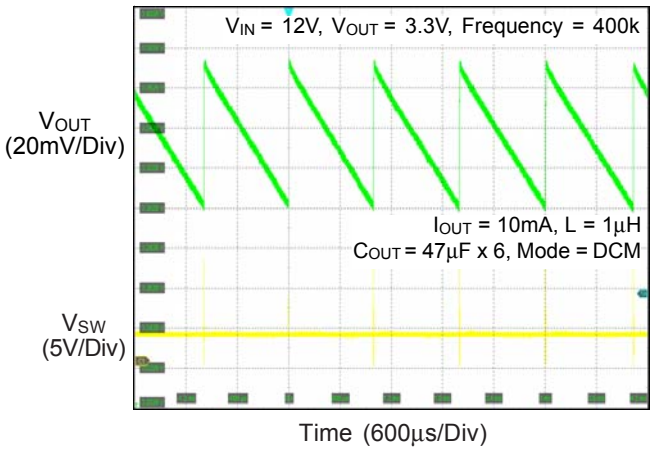
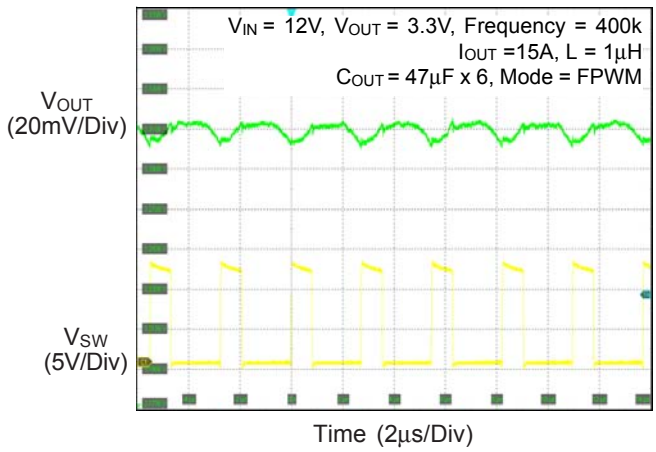
Output Ripple Voltage



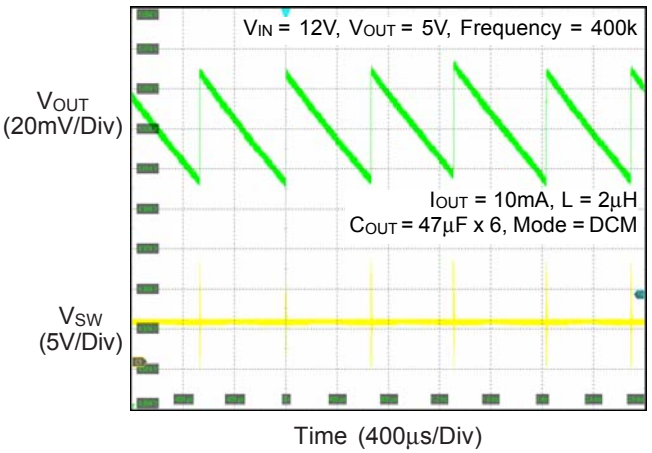
Output Ripple Voltage



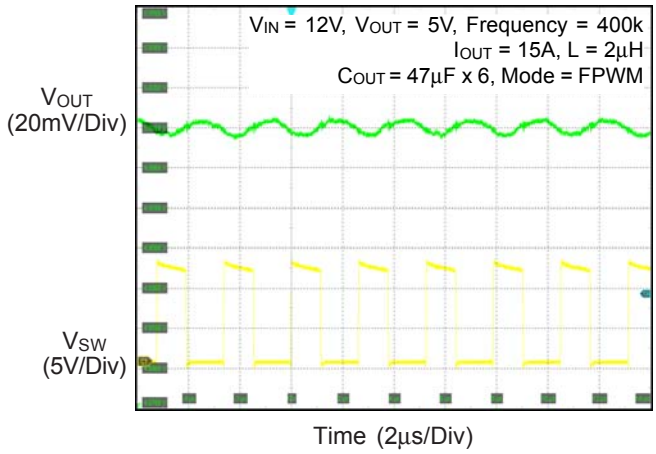
Output Ripple Voltage



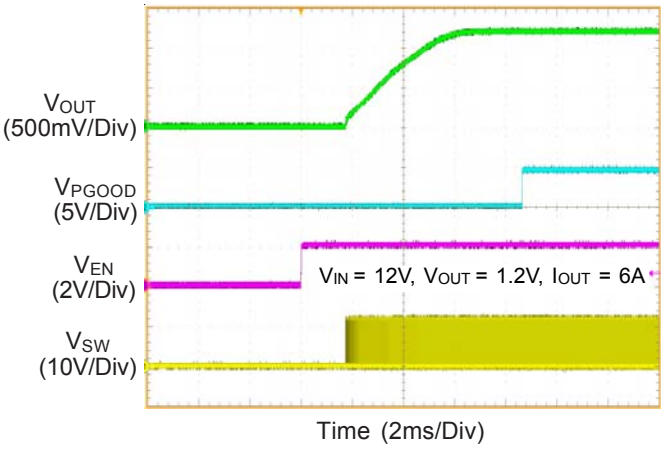
Output Ripple Voltage



Output Ripple Voltage



Power On from EN



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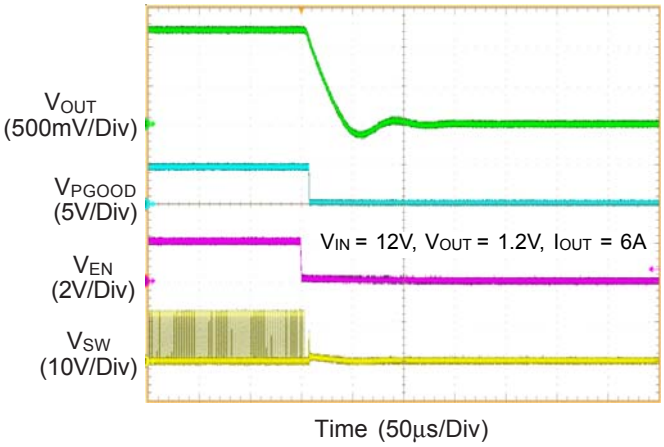
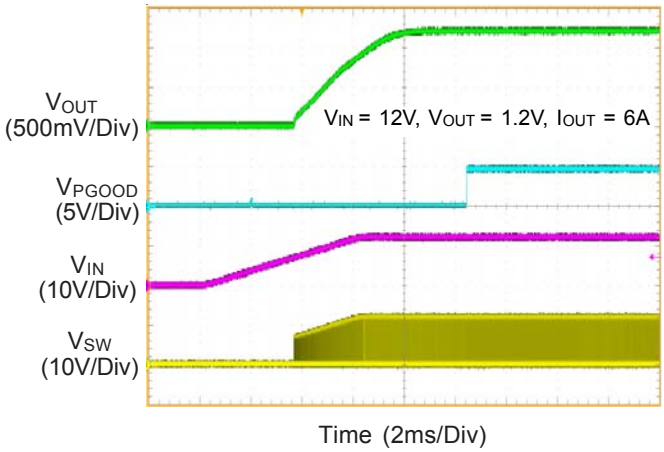
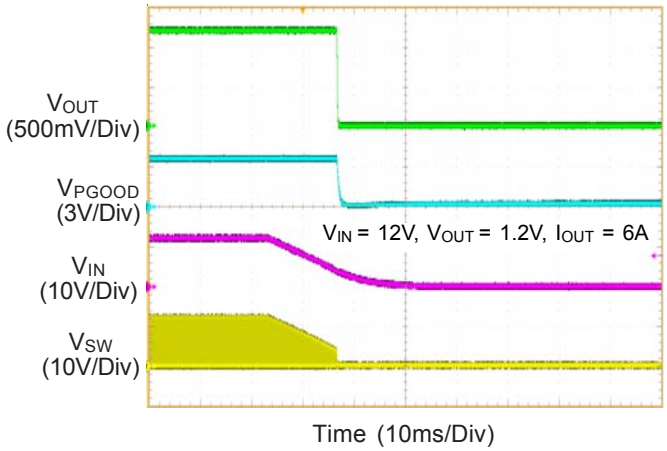
Power Off from EN



Power On from VIN



Power Off from VIN



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Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

A general RTQ2822T application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement and begins with the selection of the operating frequency and light load operating mode by setting the MODE pin voltage. Next, the inductor L is chosen and then the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} can be selected. Next, feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as the EN and UVLO threshold, external soft-start time, and PGOOD.

Switching Frequency and MODE Selection

The switching frequency, current limit and switching mode (DCM or FCCM) are set by a voltage divider from, and is only from, VCC to GND connected to the MODE pin. Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold and increases the AC losses in the inductor. To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs.

The selected inductor should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L_PEAK} = I_{OUT_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

The reverse inductor current should be take into account, in FCCM operation, the design of inductor valley current should be higher than I_{LIM_NEG} –5A (max.) to prevent triggering NOC at no load operation.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. The C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

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$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low. The ripple which is caused by ESR can be ignored, and the minimum input capacitance can be estimated as equation below :

$$C_{IN_MIN} = I_{OUT_MAX} \times \frac{D(1-D)}{\Delta V_{CIN_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} = 2 00mV for typical application (V_{IN} > 7V)

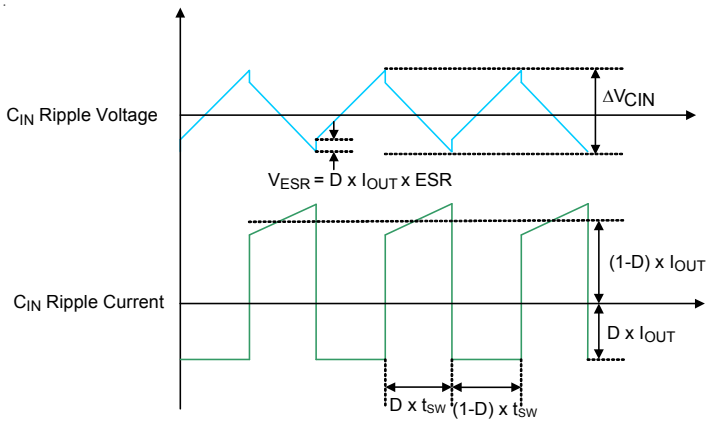

Figure 6. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of :

$$I_{RMS} \cong I_{OUT_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worse $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of its small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2822T circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, two small ceramic capacitors of 0.1µF should be placed close to the part. Place one between the VIN1 and PGND1 pins, and place the other between the VIN2 and PGND2 pins. These capacitors should be 0402 or 0603 in size.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple, the transient loads and to ensure that control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, and can be expressed as below :

$$\Delta V_{OUT} = \Delta V_{P-P_ESR} + \Delta V_{P-P_C}$$

$$\Delta V_{P-P_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}. The highest output ripple is at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF_MIN}}$$

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The worst-case output sag voltage can be determined by :

$$\Delta V_{OUT_SAG} = \frac{L \times (I_{L_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of overshoot due to stored inductor energy when the load is removed can be calculated as :

$$\Delta V_{OUT_SOAR} = \frac{L \times (I_{L_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Internal VCC Regulator

Good bypassing at VCC pin is necessary to supply the high transient currents required by the power MOSFET gate drivers. Place a low ESR MLCC capacitor with capacitance ≥ 4.7μF as close as possible to VCC pin. The rated voltage of C_{VCC} should be higher than 10V with 0603 or 0805 in size.

Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Do not connect VCC to provide power to other devices or loads.

HSFET Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal MOSFET switch to a voltage equal to approximately V_{VCC} each time the LSFET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle.

The selection of C_{BOOT} considers the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BOOT} such that the available gate-drive voltage is not significantly degraded when determining C_{BOOT}. A typical range of ΔV_{BOOT} is from 100mV to 300mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. For most applications, a 0.1μF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

It is recommended to add an external bootstrap Schottky diode between an external 5V voltage supply and the BOOT pin as shown in Figure 7 to improve enhancement of the internal MOSFET switch and improve efficiency when the input voltage, V_{IN}, is below 5V. The bootstrap Schottky diode can be a low-cost one, such as BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RTQ2822T. Note that the BOOT voltage V_{BOOT} must be lower than 5.5V. The figure 8 shows the efficiency with/without an external 5V supply.

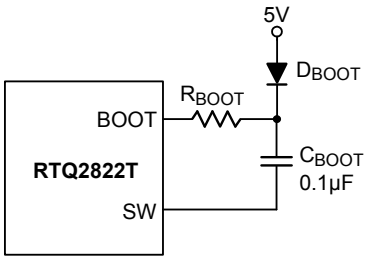

Figure 7. External Bootstrap Diode and Resistor at the BOOT Pin

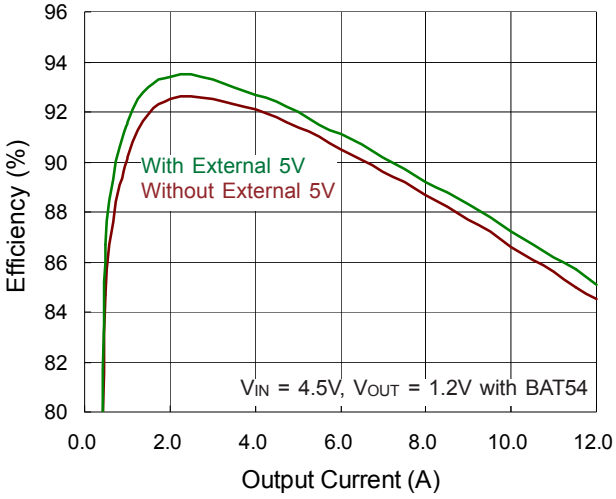

Figure 8. Efficiency Comparison with/without external 5V supply

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EMI issue is worse when the switch is turned on rapidly due to high di/dt noises. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 20Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 8, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor/diode connection.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

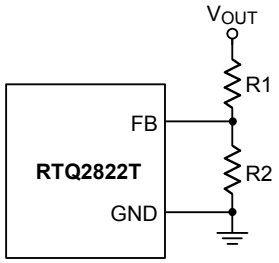

Figure 9. Output Voltage Setting

For a given R2, the resistance of R1 can be calculated as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

1% resistance is recommended to maintain output voltage accuracy. The total resistance of the FB resistor divider should be selected to be as large as possible when good low load efficiency is desired: The resistor divider generates a small load on the output, which should be minimized to optimize the quiescent current at low loads.

Place resistors R1 and R2 very close to the FB pin to minimize PCB trace length and noise. Great care should be taken to route the FB trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feed-forward capacitor (C_{FF}) may be used.

Feedforward Capacitor (C_{FF})

The RTQ2822T is optimized for low duty-cycle applications and the control loop is stable with low ESR ceramic output capacitors. In higher duty-cycle applications (higher output voltages or lower input voltage), the internal ripple signal will increase in amplitude. Before the ACOT® control loop can react to an output voltage fluctuation, the voltage change on the feedback signal must exceed the internal ripple amplitude. Because of the large internal ripple in this condition, the response may become too slow, and may show an under-damped response. This can cause some ringing in the output, and is especially visible at higher output voltage applications like 12V to 5V where duty-cycle is high and the feedback network attenuation is large, adding to the delay. As shown in Figure 10, adding a feedforward capacitor (C_{FF}) across the upper feedback resistor is recommended. This increases the damping of the control system.

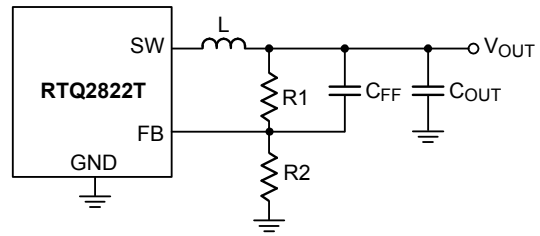

Figure 10. Feedback Loop with Feedforward Capacitor

Loop stability can be checked by viewing the load transient response. A load step with a speed that exceeds the converter bandwidth must be applied. For the ACOT®, loop bandwidth can be in the order of 100 to 200kHz, so a load step with 500ns maximum rise time (di/dt ≈ 2A/μs) ensures the excitation frequency is sufficient. It is important that the converter operates in PWM mode, outside the light load efficiency range, and below any current limit threshold. A load transient from 30% to 60% of maximum load is reasonable which is shown in Figure 11.

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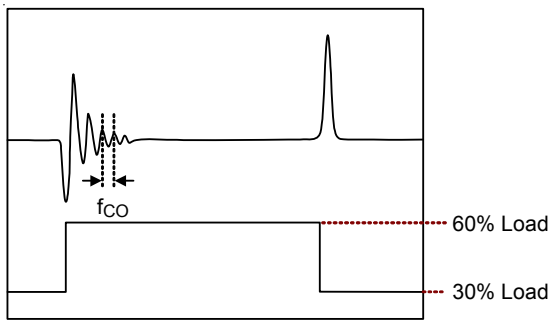

Figure 11. Example of Measuring the Converter BW by Fast Load Transient

C_{FF} can be calculated based on below equation :

$$C_{FF} = \frac{1}{2\pi \times BW} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Figure 12. shows the transient performance with and without feedfoward capacitor.

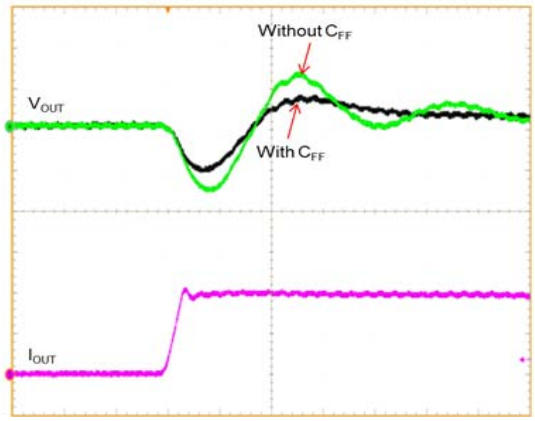

Figure 12. Load Transient Response with and without Feedforward Capactior

Note that, after defining the C_{FF}, please also check the load regulation because feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage is over specification caused by calculated C_{FF}, please decrease the value of feedforward capacitor C_{FF}.

Enable and Adjustable UVLO

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching. It stops switching when the EN pin voltage falls below the turn-off threshold (V_{ENL}). The RTQ2822T internally week pull-down the EN pin. Figure 13 shows an example if an enable time delay is required.

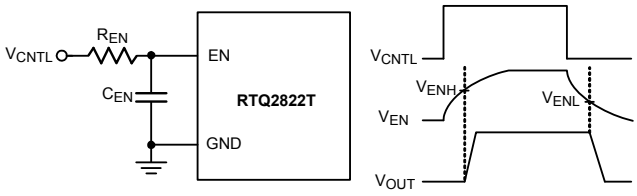

Figure 13. Enable Timing Control

Thermal Considerations

In many applications, the RTQ2822T does not generate much heat due to its high efficiency and low thermal resistance of its flip-chip VQFN-18L 3.5x3.5 package. However, in applications which the RTQ2822T runs at a high ambient temperature, high input voltage and high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 160°C, the RTQ2822T stops switching the power MOSFETs until the temperature cools down by 15°C.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA(EFFECTIVE)}$$

Where

$T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Table 7 shows the simulated thermal resistance of the RTQ2822T which is mounted on PCB with difference tack-up and copper thickness. The layout of thermal model

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refers to the RTQ2822T evaluation board.

Table 7. Simulated Thermal Resistance with Difference Tack-Up and Copper Thickness

Simulated θ_{JA}	θ_{JA} (°C/W)
4 Layer with 2oz copper	28
4 Layer with 1oz copper	40
2 Layer with 1oz copper	52.5

As an example, consider the case when the RTQ2822T is used in applications where V_{IN} = 12V, I_{OUT} = 15A, f_{SW} = 400kHz, V_{OUT} = 1.2V.

The efficiency at 1.2V, 15A is 82% by using WE-744311068 (0.68µH, 3.1mΩ DCR) as the inductor and measured at room temperature. The core loss 0.16W can be obtained from its website. In this case, the power dissipation of the RTQ2822T is

$$P_{D,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 3.1W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 28°C/W by using the RTQ2822T evaluation board with 4 layers PCB and 2oz copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

$$T_J = 3.1W \times 28°C/W + 25°C = 112°C$$

Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2822T :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- The VIN pins should have equal input capacitors on each side of IC. Place these input capacitors as close to the VIN pins as possible.
- Place the VCC decoupling capacitor, C_{VCC}, as close to the VCC pin as possible.
- Place bootstrap capacitor, C_{BOOT}, as close to IC as possible. Rout the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and PGND and, close to input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible. Add thermal vias under and near the RTQ2822T to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Connect the feedback sense network behind via of output capacitor.
- Place the feedback components R1/R2/C_{FF} near the IC.
- The ground connection between analog ground and power ground should be close to IC to minimum the ground current loops. If there is only one ground plane, it should keep enough isolation between analog return signals and high power signals.

Figure 14 is the layout example which uses 3"x3" (76mm x76mm), four-layer PCB with 2oz copper.

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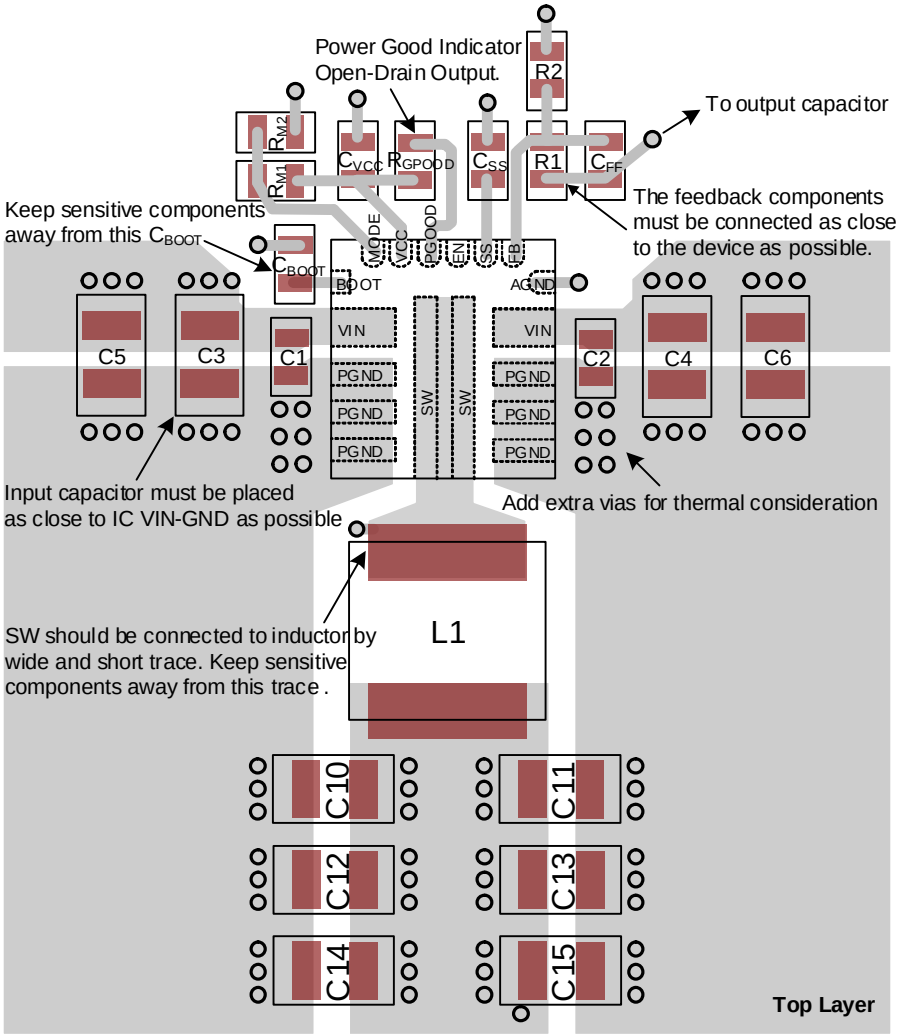

Figure 14. Layout Guide (Top Layer)

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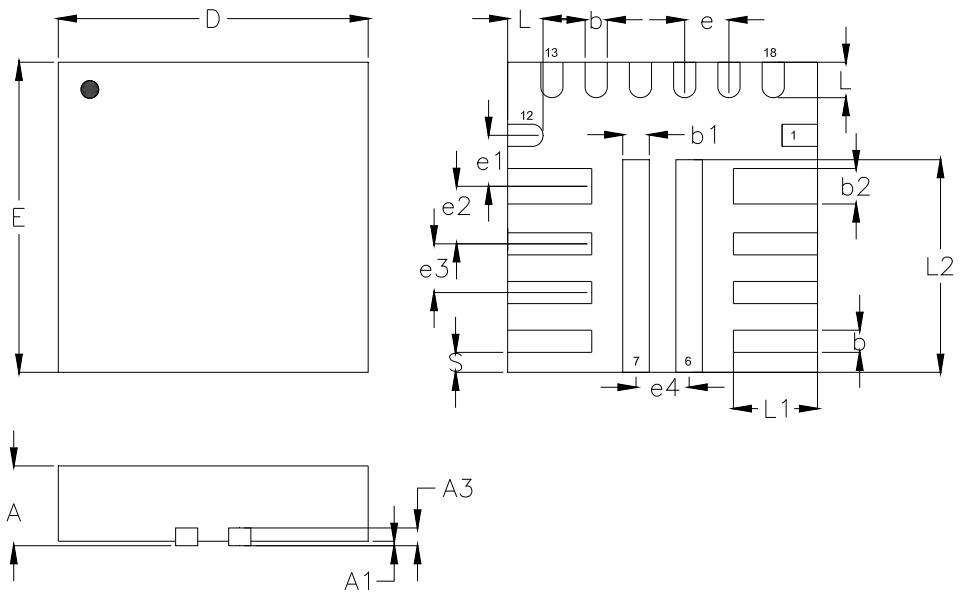
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
b1	0.250	0.350	0.010	0.014
b2	0.350	0.450	0.014	0.018
D	3.400	3.600	0.134	0.142
E	3.400	3.600	0.134	0.142
e	0.500		0.020	
e1	0.575		0.023	
e2	0.650		0.026	
e3	0.550		0.022	
e4	0.600		0.024	
S	0.225		0.009	
L	0.350	0.450	0.014	0.018
L1	0.900	1.000	0.035	0.039
L2	2.350	2.450	0.093	0.096

V-Type 18L QFN 3.5x3.5 (FC) Package

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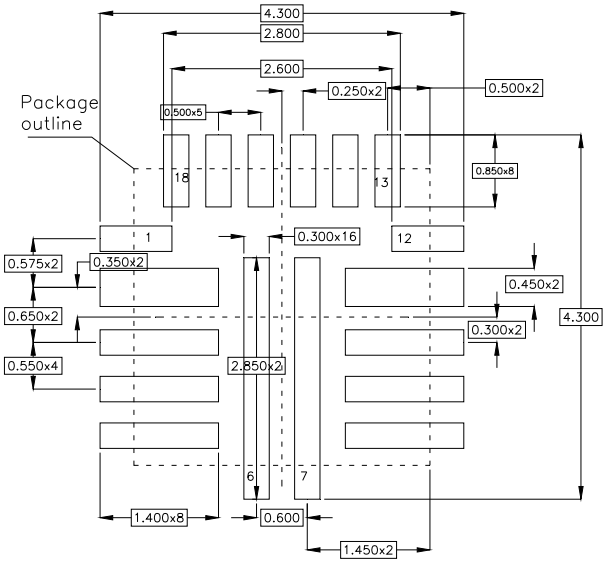
Footprint Information



Package	Number of Pin	Tolerance
V/W/U/XQFN3.5x3.5-18(FC)	18	±0.05

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Datasheet Revision History

Version	Date	Description	Item
02	2023/2/17	Modify	Absolute Maximum Ratings on P10 ESD Ratings on P10 Thermal Information on P10 Note 2, Note 3, Note 4, Note 5 on P13 Application Information on P23, 29

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