RICHTEK®

RTQ5162

DDR5 Client Extreme VR on DIMM PMIC

1 General Description

The RTQ5162 is an integrated power management IC designed for DDR5 SODIMM, UDIMM, CSODIMM, and CUDIMM applications. This device provides three buck converters (SWA, SWB, and SWC) and two LDOs (VLDO_1.0V and VLDO_1.8V). The voltage regulators, SWA and SWB can operate in either single-phase or dual-phase mode. Additionally, the RTQ5162 supports a selectable interface (I^2C or I3C Basic) to accommodate various application environments. A comprehensive protection mechanism is embedded to ensure safe power distribution, with the capability to record fault events in registers and signal them through the PWR_GOOD and GSI_n open-drain indicators. The RTQ5162 is available in a WQFN-28L 3x4 (FC) package. The recommended junction temperature range is from -40°C to 125°C.

2 Ordering Information

RTQ5162 □□-□□□

- **MTP Serial Number**
  0: JEDEC Default Code
- **Single Phase**
  1: SWA/SWB Single Phase
  2: SWA/SWB Dual Phase
- **Version**
- **Package Type**(1)
  QWF: WQFN-28L 3x4 (FC) (W-Type)
- **Lead Plating System**
  G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates that Richtek products are Richtek Green Policy compliant.

3 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

4 Features

- **Meet JEDEC DDR5 PMIC5120 Specification**
- **VIN_Bulk with Input Supply Range: 4.25V to 5.5V**
- **High Integration:**
  - **Three High Efficiency Buck Converters:**
    - **SWA: I_{TDC} = 6 A, I_{MAX} = 8.5 A**
    - **SWB: I_{TDC} = 6 A, I_{MAX} = 8.5 A**
    - **SWC: I_{TDC} = 2 A, I_{MAX} = 3 A**
  - **Two LDOs:**
    - **VLDO_1.8V: I_{MAX} = 25mA**
    - **VLDO_1.0V: I_{MAX} = 20mA**
- **Programmable Dual-Phase and Single-Phase Regulators for SWA and SWB**
- **0.75% Converter Output Accuracy**
- **Fast Transient Response with A^2RCOT Control**
- **Support I^2C and I3C Basic Interfaces**
- **Error Log Counter and Data Storage (NVM)**
- **MTP Registers with Secured R/W Access**
- **Programmable DIMM Specific Registers for Customization**
- **Programmable Mode for Debug and Validation**
- **Telemetry for Output Current, Voltage, and Power**
- **Complete Protection Mechanisms**
  - **VIN_Bulk Input Supply UVP and OVP**
  - **OVP, UVP, OCP, and HCW for Each Rail**
  - **High-Temperature Warning and OTP**
- **General Status Interrupt Function**
- **Power-Good Indicator**

5 Applications

- DDR5 SODIMM, UDIMM
- DDR5 CSODIMM, CUDIMM

6 Simplified Application Circuit

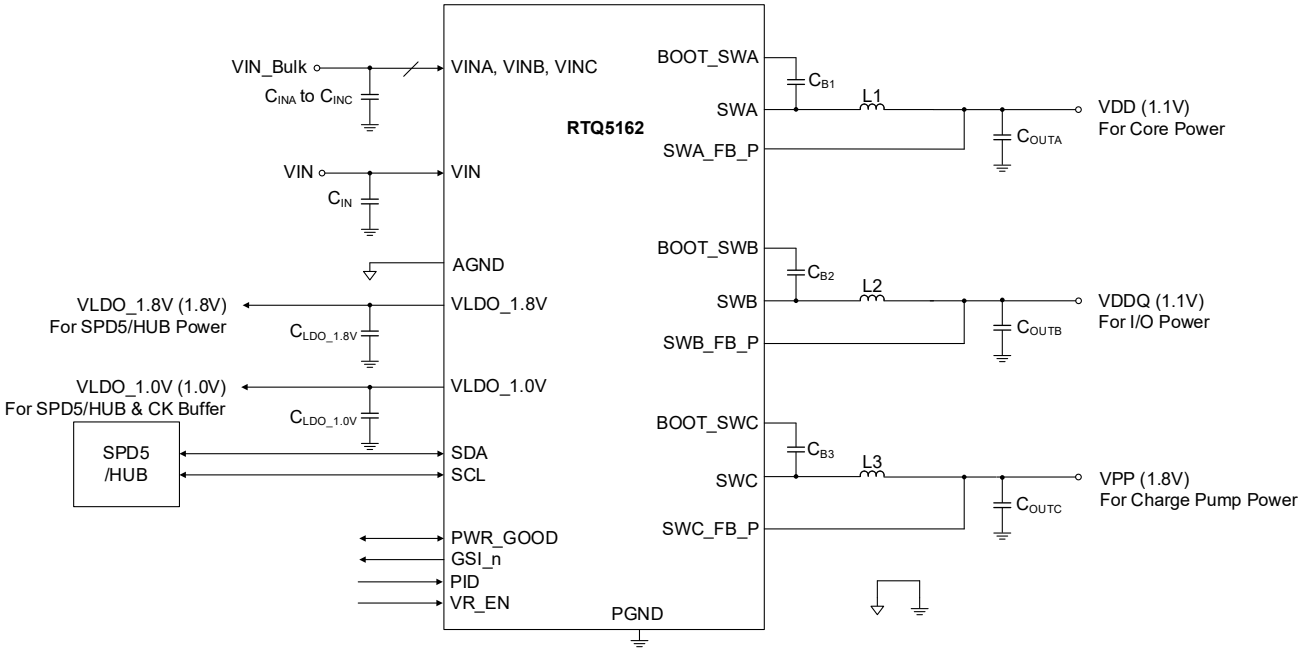

Figure 1. SWA and SWB are Operating in Single-Phase Mode

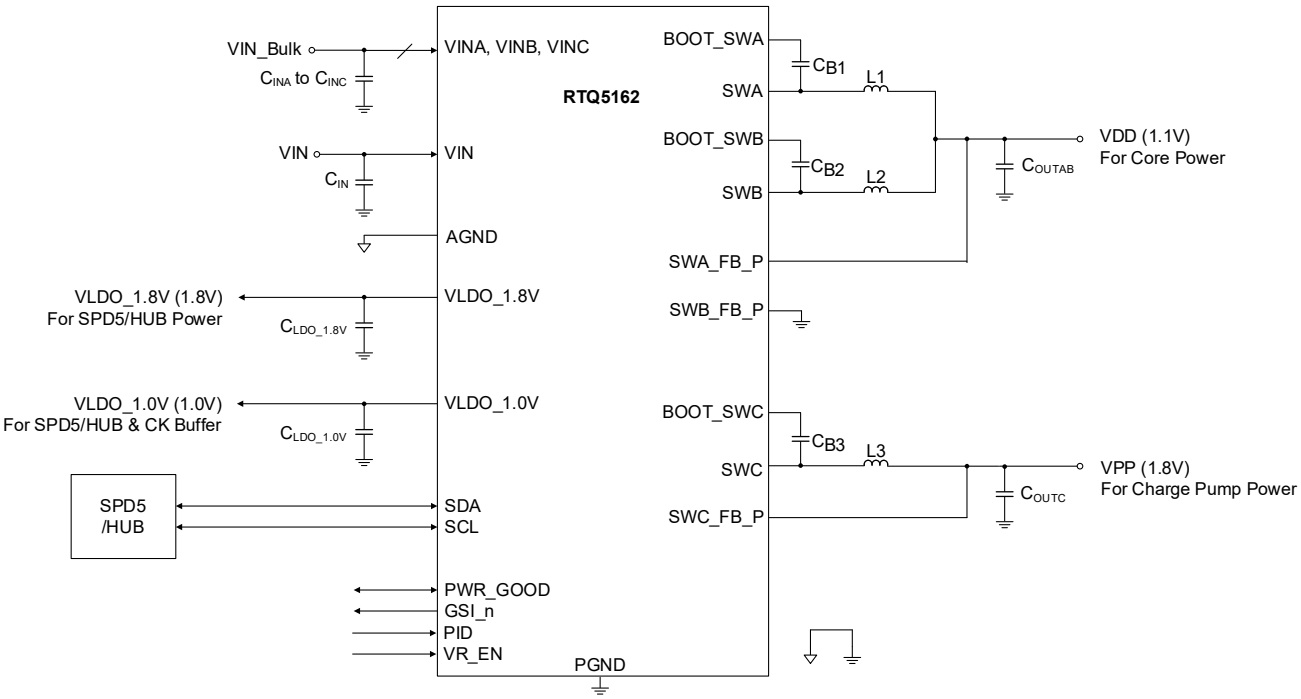

Figure 2. SWA and SWB are Combined as Dual-Phase Mode

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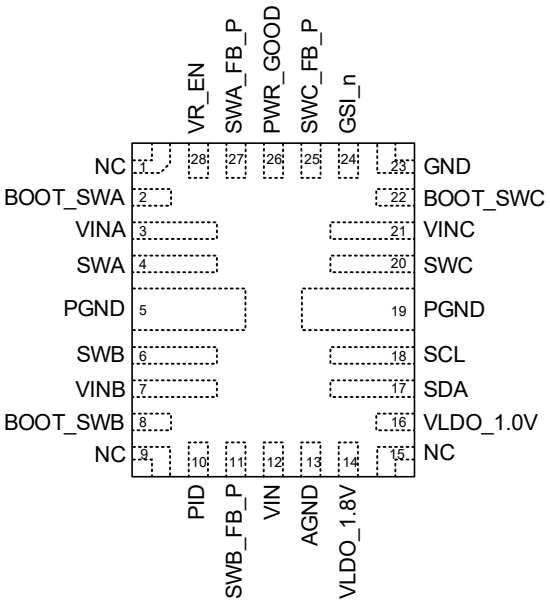
7 Pin Configuration

(TOP VIEW)



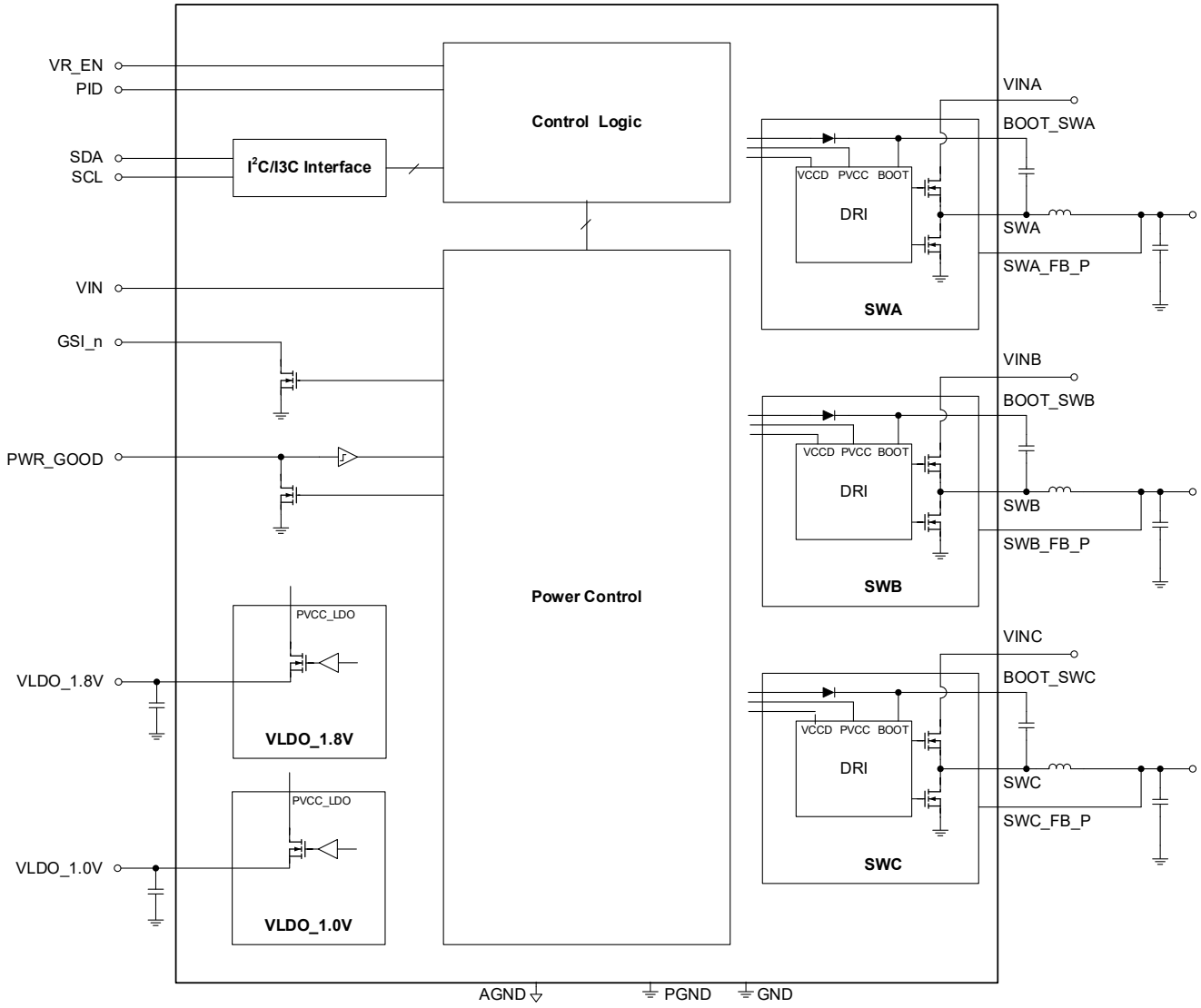
WQFN-28L 3x4 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 9, 15	NC	Non-functional pins. No internal connections to the IC. Connecting these pins to GND allows users to extend the GND copper coverage on the PCB top layer to enhance the thermal convection.
2	BOOT_SWA	Buck A bootstrap. The bootstrap node for the SWA switch node's high-side NMOS driver. Connect a capacitor between SWA and BOOT_SWA to form a floating supply across the high-side switch driver of Buck A.
3	VINA	Input supply of Buck A. VINA is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
4	SWA	Buck A switch output. Output switch node SWA regulator. This pin is connected to an external inductor (L1). In single-phase mode of operation, the SWA output must not be connected to the SWB or SWC output, even if these switch nodes are configured to have the same output voltage.
5, 19	PGND	Common Power ground. Connect PGND to DIMM ground plane. PGND pins require special consideration during PCB layout.
6	SWB	Buck B switch output. Output switch node SWB regulator. This pin is connected to an external inductor (L2). In single-phase mode of operation, the SWB output must not be connected to the SWA or SWC output, even if these switch nodes are configured for the same output voltage.
7	VINB	Input supply of Buck B. VINB is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
8	BOOT_SWB	Buck B bootstrap. The bootstrap node for the SWB switch node's high-side NMOS driver. Connect a capacitor between SWB and BOOT_SWB to form a floating supply across the high-side switch driver of Buck B.
10	PID	PMIC ID pin for I^2C and I3C Basic bus.

Pin No.	Pin Name	Pin Function
11	SWB_FB_P	Positive feedback of Buck B. In a single-phase output regular configuration, this pin is connected to the SWB remote positive sense feedback. Otherwise, it must be connected to AGND.
12	VIN	5V power input supply to the PMIC for analog circuits.
13	AGND	Analog ground. Connect AGND to the power ground pin with a single via.
14	VLDO_1.8V	PMIC 1.8V LDO supply. Connect a 4.7μF decoupling capacitor near this pin.
16	VLDO_1.0V	PMIC 1.0V LDO supply for I3C push-pull driver. Connect a 4.7μF decoupling capacitor near this pin.
17	SDA	Bus data of I^2C and I3C.
18	SCL	Bus clock of I^2C and I3C.
20	SWC	Buck C switch output. Output switch node for the SWC regulator. This pin is connected to an external inductor (L3).
21	VINC	Input supply of Buck C. VINC is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
22	BOOT_SWC	Buck C bootstrap. The bootstrap node for the SWC switch node's high-side NMOS driver. Connect a capacitor between SWC and BOOT_SWC to form a floating supply across the high-side switch driver of Buck C.
23	GND	Thermal connection to GND. This pin is connected to GND on the PCB and is connected to GND on the die internally.
24	GSI_n	General status interrupt. Open-Drain Output. The RTQ5162 asserts this pin low to communicate one or more events to the host. This pin remains asserted until the appropriate registers are explicitly cleared and the event is no longer present.
25	SWC_FB_P	Positive feedback of Buck C. Switch node SWC remote positive sense feedback.
26	PWR_GOOD	Power-good indicator. This pin can be configured as an open-drain output pin or as an input pin. As an open-drain output pin: The RTQ5162 allows this pin to float high when the VIN_Bulk input supply, all enabled buck output regulators, and all LDO regulators maintain the tolerance thresholds configured in the appropriate registers. The RTQ5162 drives this pin low if the VIN_Bulk input falls below the threshold, or if any of the enabled buck output regulators or any LDO output regulator exceeds the configured threshold tolerance. As an input pin: The RTQ5162 disables its output regulators when this pin is driven low; however, the LDO outputs should remain on.
27	SWA_FB_P	Positive feedback of Buck A. This pin is connected to the SWA remote positive sense feedback.
28	VR_EN	PMIC enable. When this pin is high, the RTQ5162 turns the regulator on. Conversely, when the pin is low, the RTQ5162 turns the regulator off. This pin should not be left floating. If unused, it should be connected to GND.

9 Function Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VINA, VINB, VINC ---------- –0.3V to 6V
- Supply Input Voltage, VIN ---------- –0.3V to 6V
- AGND to PGND ---------- –0.3V to 0.3V
- Switching Nodes, SWA, SWB, SWC
  - DC ---------- –0.3V to 6V
  - < 25ns ---------- –3V to 9V
- Boot Voltage
- BOOT to SWA (BOOT-SWA) ---------- –0.3V to +6V
- BOOT to SWB (BOOT-SWB) ---------- –0.3V to +6V
- BOOT to SWC (BOOT-SWC) ---------- –0.3V to +6V
- Other I/O ---------- –0.3V to +6V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-28L 3x4 (FC) ---------- 2.28W
- Package Thermal Resistance (Note 3)
  - WQFN-28L 3x4 (FC), θ_{JA} ---------- 43.86°C/W
  - WQFN-28L 3x4 (FC), θ_{JC} ---------- 19.7°C/W
  - WQFN-28L 3x4 (FC), θ_{JB} ---------- 6.51°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 155°C
- Storage Temperature Range ---------- –55°C to 150°C
- ESD Susceptibility (Note 4)
  - HBM ---------- 2kV
  - CDM ---------- 500V

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at TA = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, V_{INA}, V_{INB}, V_{INC} ---------- 4.25V to 5.5V
- Supply Input Voltage, V_{IN} ---------- 4.25V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{INA} = V_{INB} = V_{INC} = 5V, V_{IN} = 5V, T_A = –40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
(VIN) Shutdown Current	I_{SHDN_VIN}	T_A = 25°C ; VIN = VIN_Bulk = 5V, VR_EN = 0, all circuitry including output regulators and LDOs are off.	10	--	25	μA
VIN Supply Current (Non-Switching)	$I_{Q\_VIN\_NSW}$	T_A = 25°C ; I_{OUT} = 0mA, all LDOs, SWA to SWC on, no switching	--	1.9	--	mA
VIN Undervoltage Lockout and OVP Threshold						
VIN Undervoltage Lockout Rising Threshold	$V_{IN\_UVLO\_R}$	Rising edge	--	4	--	V
VIN Undervoltage Lockout Falling Threshold	$V_{IN\_UVLO\_F}$	Falling edge	--	3.5	--	V
VIN Overvoltage Rising Threshold	$V_{IN\_OVP\_R}$	Setting by reg_0x1B"[7] = "0"	--	6	--	V
I^2C, I3C and Interface DC Electrical Specification						
SDA or SCL Operate Frequency	f_{SCL}		0.4	--	12.5	MHz
SDA or SCL Input High Voltage	V_{IH_I2C}		0.7	--	3.6	V
SDA or SCL Input Low Voltage	V_{IL_I2C}		–0.3	--	0.3	V
PWR_GOOD Input High Voltage	V_{IH_PGOOD}		1.26	--	3.6	V
VR_EN Input High Voltage	V_{IH_EN}		1.26	--	3.6	V
PWR_GOOD Input Low Voltage	V_{IL_PGOOD}		–0.3	--	0.3	V
VR_EN Input Low Voltage	V_{IL_EN}		–0.3	--	0.3	V
PID Input High Voltage	V_{IH_PID}		1.2	--	1.8	V
PID Input Low Voltage	V_{IL_PID}		0	--	0.2	V
SDA Output High Voltage	V_{OH_SDA}	I_O = –3mA	0.75	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
(SDA, GSI_n, or PWR_GOOD) Output Low Voltage	V_{OL}	I_O = 3mA	0	--	0.3	V
SDA Output High Current	I_{OH_SDA}		–3	--	--	mA
(SDA, GSI_n, or PWR_GOOD Output Low Current	I_{OL}		--	--	3	mA
SDA Output Pull-Up Impedance	R_{PU_SDA}		--	40	--	Ω
SDA Output Pull-Down Impedance	R_{PD_SDA}		--	20	--	Ω
GSI_n Output Pull-Down Impedance	$R_{PD\_GSI\_n}$		--	50	--	Ω
PWR_GOOD Output Pull-Down Impedance	R_{PD_PGOOD}		--	50	--	Ω
SWA/B Rail – VDD/VDDQ (1.1V) - Single Phase Regulator (0.8V to 1.435V, ITDC = 6A for each rail)						
Output Voltage Setting	V_{OUT_AB}	SWA (single phase) or SWA+SWB (dual phase) setting by reg_0x21"[7:1] (without applying resolution change by reg_0x2B"[5]=”0”)	0.8	--	1.435	V
		SWB (single phase) setting by reg_0x25"[7:1] (without applying resolution change by reg_0x2B"[4]=”0”)				
Output Voltage Accuracy	$V_{OUT\_AB\_ACC}$	I_{OUT} = 0A, operating at CCM	–0.75	--	0.75	% of V_{OUT_AB}
VID Slew Rate	SR_{VID_AB}		--	1	--	mV/ μs
SWA/B Soft-Start/Stop Time						
Soft-Start Time	t_{SS}	t_{set} = 1ms to 14ms	–15	--	15	% of t_{SS}
Soft-Stop Time	t_{STOP}	t_{set} = 1ms to 8ms	–20	--	20	% of t_{STOP}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWA/B Internal MOSFET Turn On Resistance						
On-Resistance of High-Side MOSFET	R_{DSON_H}	T_A = 25°C	--	16	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	T_A = 25°C	--	10	--	mΩ
SWA/B Switching Frequency						
Switching Frequency	f_{SW_AB}	Setting by reg_0x29"[5:4]/0x2A"[7:6] = "00" (default)	0.6375	0.75	0.8625	MHz
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "01"	0.85	1	1.15	
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "10"	1.0625	1.25	1.4375	
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "11"	1.275	1.5	1.725	
SWA/B Power-Good Indicator						
(Power-Good) Falling Threshold	$V_{OUT\_AB\_PGOOD\_F}$	Setting by reg_0x21"[0]/0x25"[0] = "0" (default)	--	–5	--	% of V_{OUT_AB}
		Setting by reg_0x21"[0]/0x25"[0] = "1"	--	–7.5	--	
(Power-Good) Falling Propagation Delay	$t_{DLY\_PGOOD\_F\_AB}$		--	5	--	µs
(Power-Good) Rising Threshold	$V_{OUT\_AB\_PGOOD\_R}$	Setting by reg_0x22"[7:6]/0x26"[7:6] = "00"	--	5	--	% of V_{OUT_AB}
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "01" (default)	--	7.5	--	
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "10"	--	10	--	
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "11"	--	2.5	--	
(Power-Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_AB}$		--	5	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWA/B Protections						
Output Overvoltage Rising Threshold	$V_{OUT\_AB\_OVP\_R}$	Setting by reg_0x22"[5:4]/0x26"[5:4] = "00"	--	7.5	--	% of V_{OUT_AB}
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "01"	--	10	--	
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "10" (default)	--	12.5	--	
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "11"	--	20	--	
Output Overvoltage Protection Propagation Delay	$t_{DLY\_OVP\_AB}$		--	5	--	µs
Output Undervoltage Falling Threshold	$V_{OUT\_AB\_UVP\_F}$	Setting by reg_0x22"[3:2]/0x26"[3:2] = "00" (default)	--	–10	--	% of V_{OUT_AB}
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "01"	--	–12.5	--	
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "10"	--	–7.5	--	
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "11"	--	–20	--	
Output Undervoltage Protection Propagation Delay	$t_{DLY\_UVP\_AB}$		--	5	--	µs
SWA/B Current Limit						
Positive Inductor Valley Current Limit	$I_{LIM\_VALLEY\_AB}$	Valley current limited Setting by reg_0x20"[7:6]/[5:4] = "00"	--	4.5	--	A
		Setting by reg_0x20"[7:6]/[5:4] = "01"	--	5.5	--	
		Setting by reg_0x20"[7:6]/[5:4] = "10"	--	6.5	--	
		Setting by reg_0x20"[7:6]/[5:4] = "11"(default)	--	8	--	
SWC Rail – VPP(1.8V) – Single Phase Regulator (1.5V to 2.135V, ITDC = 2A)						
Output Voltage Setting	V_{OUTC}	Setting by reg_0x27"[7:1]	1.5	1.8	2.135	V
Output Voltage Accuracy	$V_{OUT\_C\_ACC}$	I_{OUT} = 0A, operating at CCM	–0.75	--	0.75	% of V_{OUT_C}
VID Slew Rate	SR_{VID_C}		--	1	--	mV/µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWC Soft-Start/Stop Time						
Soft-Start Time	t_{SS}	t_{set} = 1ms to 14ms	−15	--	15	% of t_{SS}
Soft-Stop Time	t_{STOP}	t_{set} = 1ms to 8ms	−20	--	20	% of t_{STOP}
SWC Internal MOSFET Turn On Resistance						
On-Resistance of High-Side MOSFET	R_{DSON_H}	T_A = 25°C	--	55	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	T_A = 25°C	--	45	--	mΩ
SWC Switching Frequency						
Switching Frequency	f_{SW_C}	Setting by reg_0x2A"[1:0] = "00" (default)	0.6375	0.75	0.8625	MHz
		Setting by reg_0x2A"[1:0] = "01"	0.85	1	1.15	
		Setting by reg_0x2A"[1:0] = "10"	1.0625	1.25	1.4375	
		Setting by reg_0x2A"[1:0] = "11"	1.275	1.5	1.725	
SWC Power-Good Indicator						
(Power-Good) Falling Threshold	$V_{OUT\_C\_PGOOD\_F}$	Setting by reg_0x27"[0] = "0" (default)	--	−5	--	% of V_{OUT_C}
		Setting by reg_0x27"[0] = "1"	--	−7.5	--	
(Power-Good) Falling Propagation Delay	$t_{DLY\_PGOOD\_F\_C}$		--	5	--	µs
(Power-Good) Rising Threshold	$V_{OUT\_C\_PGOOD\_R}$	Setting by reg_0x28"[7:6] = "00"	--	5	--	% of V_{OUT_C}
		Setting by reg_0x28"[7:6] = "01" (default)	--	7.5	--	
		Setting by reg_0x28"[7:6] = "10"	--	10	--	
		Setting by reg_0x28"[7:6] = "11"	--	2.5	--	
(Power-Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_C}$		--	5	--	µs
SWC Protections						
Output Overvoltage Rising Threshold	$V_{OUT\_C\_OVP\_R}$	Setting by reg_0x28"[5:4] = "00"	--	7.5	--	% of V_{OUT_C}
		Setting by reg_0x28"[5:4] = "01"	--	10	--	
		Setting by reg_0x28"[5:4] = "10" (default)	--	12.5	--	
		Setting by reg_0x28"[5:4] = "11"	--	20	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Overvoltage Protection Propagation Delay	$t_{DLY\_OVP\_C}$		--	5	--	μs
Output Undervoltage Falling Threshold	$V_{OUT\_C\_UVP\_F}$	Setting by reg_0x28"[3:2] = "00" (default)	--	−10	--	% of V_{OUT_C}
		Setting by reg_0x28"[3:2] = "01"	--	−12.5	--	
		Setting by reg_0x28"[3:2] = "10"	--	−7.5	--	
		Setting by reg_0x28"[3:2] = "11"	--	−20	--	
Output Undervoltage Protection Propagation Delay	$t_{DLY\_UVP\_C}$		--	5	--	μs
SWC Current Limit						
Positive Inductor Valley Current Limit	$I_{LIM\_VALLEY\_C}$	For Low Current, valley current limited Setting by reg_0x20"[1:0] = "00"	--	1.5	--	A
		Setting by reg_0x20"[1:0] = "01"	--	2	--	
		Setting by reg_0x20"[1:0] = "10"	--	2.5	--	
		Setting by reg_0x20"[1:0] = "11" (default)	--	3	--	
VLDO_1.8V (1.8V, I_{MAX} = 25mA)						
Output Voltage	$V_{LDO\_1.8V}$	Setting by reg_0x2B"[7:6] = "00"	1.66	1.7	1.74	V
		Setting by reg_0x2B"[7:6] = "01" (default)	1.76	1.8	1.84	
		Setting by reg_0x2B"[7:6] = "10"	1.85	1.9	1.95	
		Setting by reg_0x2B"[7:6] = "11"	1.95	2.0	2.05	
Soft-Start Time	t_{SS}		--	0.25	--	ms
(Power-Good) Rising Threshold	$V_{LDO\_1.8V\_PGOOD\_R}$	Setting by reg_0x1A"[2] = "0"	--	1.6	--	V
(Power-Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_LDO\_1.8V}$		--	5	--	μs
Current Limit	$I_{LIM\_LDO\_1.8V}$		50	--	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VLDO_1.0V (1.0V, I_{MAX} = 20mA)						
Output Voltage	$V_{LDO\_1.0V}$	Setting by reg_0x2B"[2:1] = "00"	0.88	0.9	0.92	V
		Setting by reg_0x2B"[2:1] = "01" (default)	0.98	1.0	1.02	
		Setting by reg_0x2B"[2:1] = "10"	1.08	1.1	1.12	
		Setting by reg_0x2B"[2:1] = "11"	1.18	1.2	1.22	
Soft-Start Time	t_{SS}		--	0.12	--	ms
(Power-Good) Rising Threshold	$V_{LDO\_1.0V\_PGOOD\_R}$	Setting by reg_0x1A"[0] = "0" (default)	--	−10	--	% of V_{LDO}
		Setting by reg_0x1A"[0] = "1"	--	−15	--	
(Power-Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_LDO\_1.0V}$		--	5	--	µs
Current Limit	$I_{LIM\_LDO\_1.0V}$		50	--	--	mA

Note 6. $I_{peakmax}$ is measured over a short period of time. Typically > 20µs but less than 50µs.

13 Typical Application Circuit

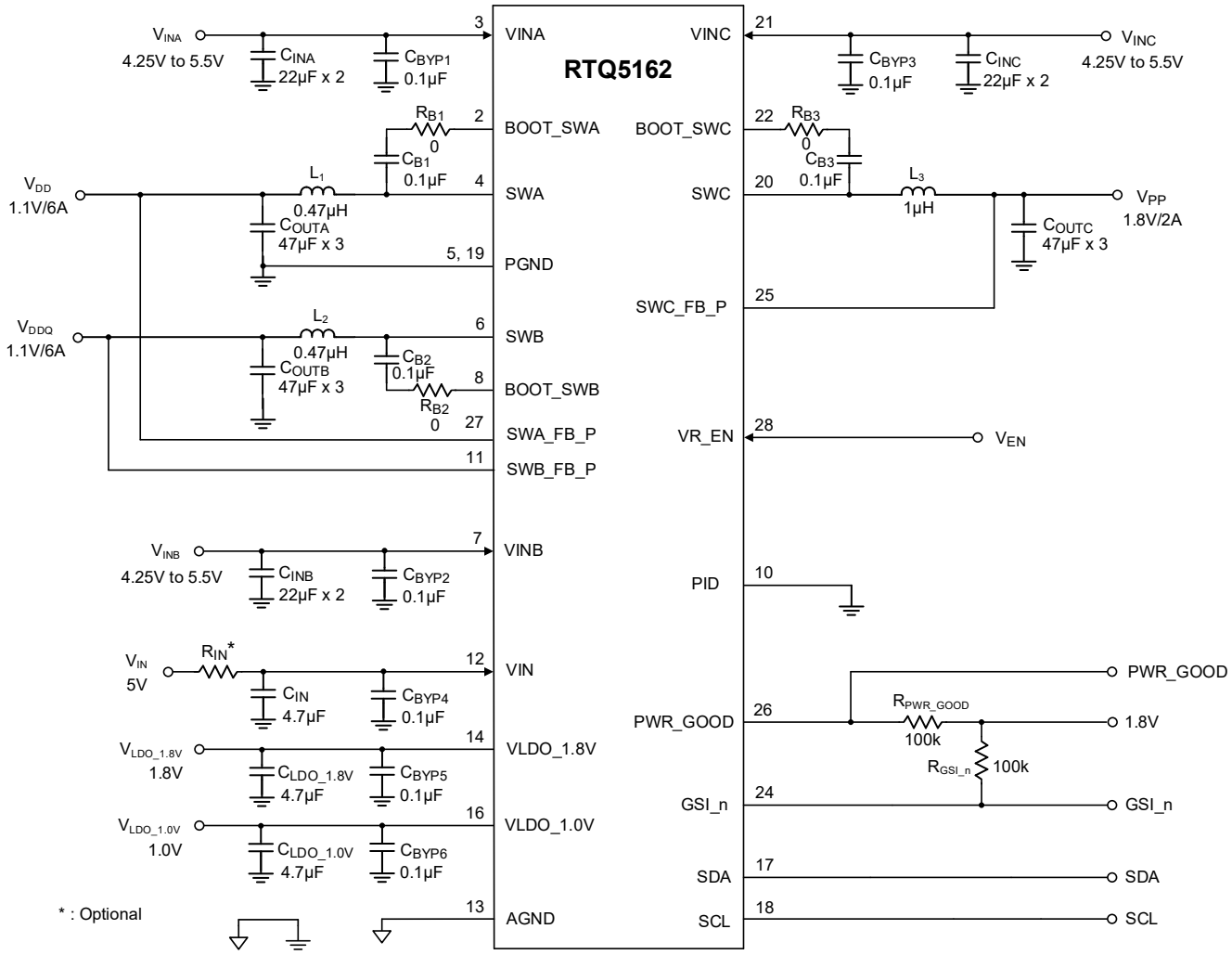


Figure 3. Typical Application Circuit When SWA and SWB Separated for 2-Outputs

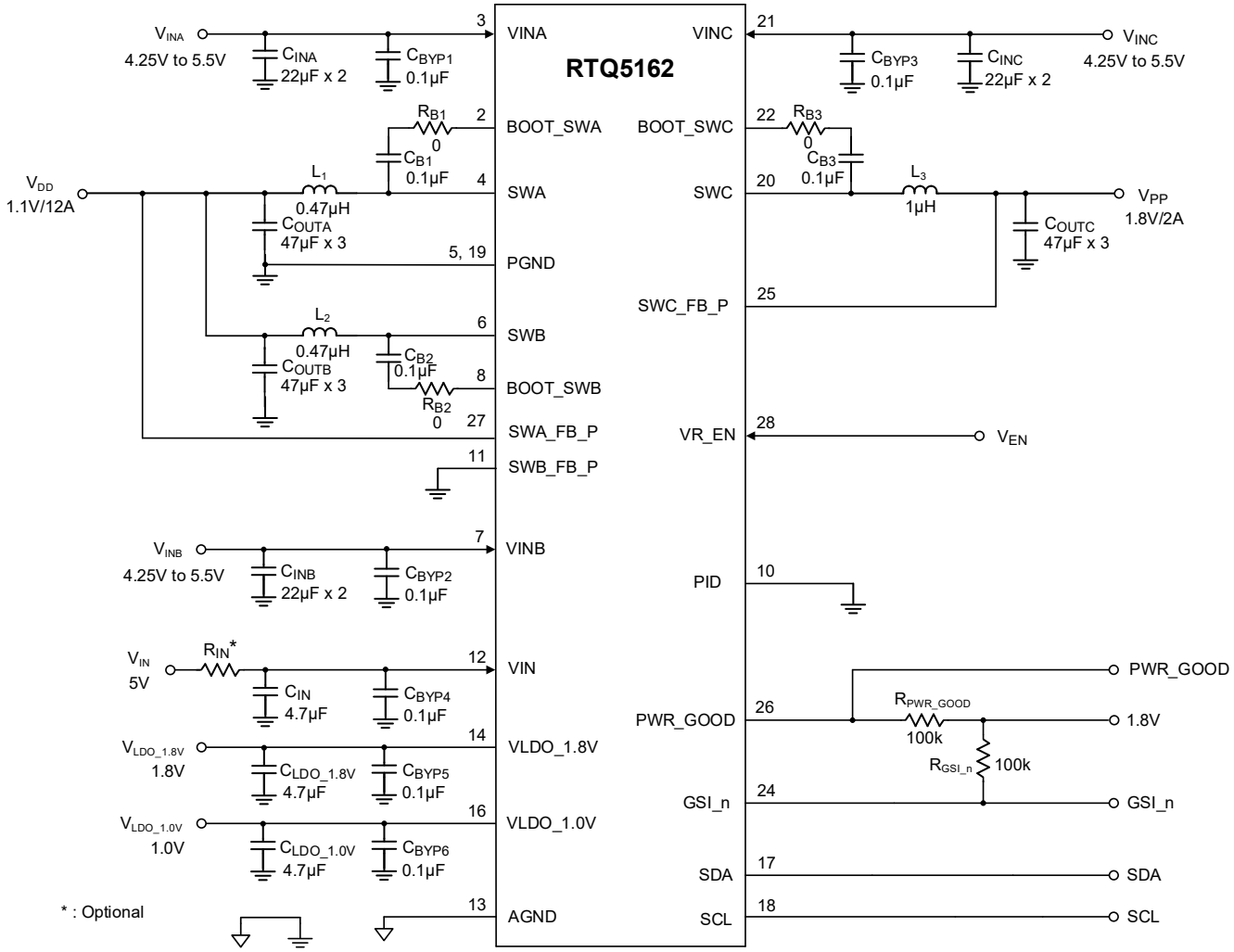


Figure 4. Typical Application Circuit When SWA and SWB Combined as Dual-phase

13.1 Recommended Component Selection

Table 1. Suggested Components for SWA and SWB

Component	Value	Physical Size	Part No.
L1, L2	0.47µH	3.2 x 2.5 x 1.2	HTTD32251B-R47MMIR-57/ LSEDM3225MKTR47M1/ CIGT322512BMR47RLE
L1, L2	0.47µH	4.1 x 4.1 x 1.2	HTED041B-R47MST/ LSEDM4040MKTR47MV/ CIGT404012BMR47RLN
C_{BYPx}	0.1µF	10V; 0201	GRM033C81E104KE14
C_{INx}	22µF (x2)	10V; 0603	GRM1880R61A226ME15
C_{OUTx}	47µF (x2)	6.3V; 0603	GRM1880R60J476ME01

Table 2. Suggested Components for SWC

Component	Value	Physical Size	Part No.
L3	1.0µH	2.5 x 2.0 x 1.2	HTTD25201B-1R0MSR-57/ LSEDB2520MKT1R0M00B/ CIGW252012TM1R0MLE
C_{BYPC}	0.1µF	10V; 0201	GRM033C81E104KE14
C_{INC}	22µF (x2)	10V; 0603	GRM1880R61A226ME15
C_{OUTC}	47µF (x2)	6.3V; 0603	GRM1880R60J476ME01

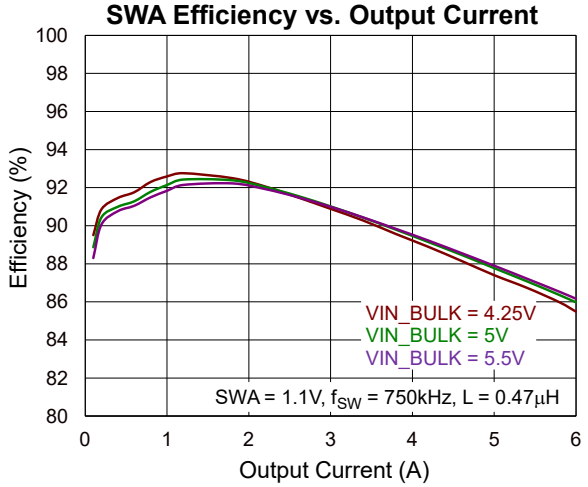
Table 3. Suggested Components for VLDO_1.8V and VLDO_1.0V

Component	Value	Physical Size	Part No.
C_{BYP}	0.1µF	10V; 0201	GRM033C81E104KE14
C_{IN}	4.7µF	10V; 0402	GRM1550R61A475MEAA
$C_{LDO\_1.8V}$	4.7µF	6.3V; 0402	GRM1550R60J475ME47
$C_{LDO\_1.0V}$	4.7µF	6.3V; 0402	GRM1550R60J475ME47

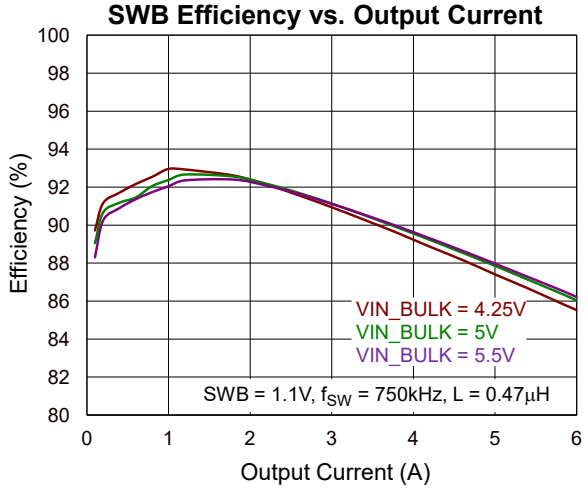
14 Typical Operating Characteristics

(Performance waveforms are tested on the evaluation board of the Typical Application Circuit, VIN_BULK = 5V, V_{DD} = 1.1V, V_{DDQ} = 1.1V, V_{PP} = 1.8V, L1 = L2 = 0.47µH, L3 = 1µH, T_A = 25°C, unless otherwise noted.)

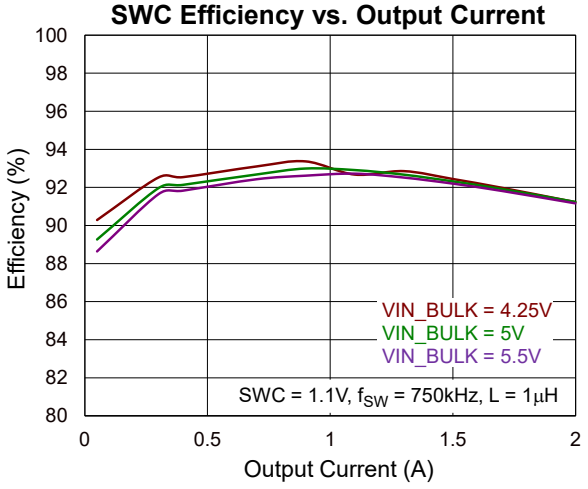
SWA Efficiency vs. Output Current



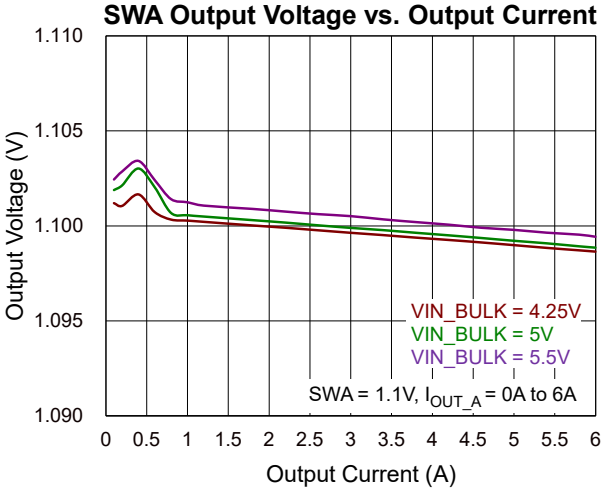
SWB Efficiency vs. Output Current



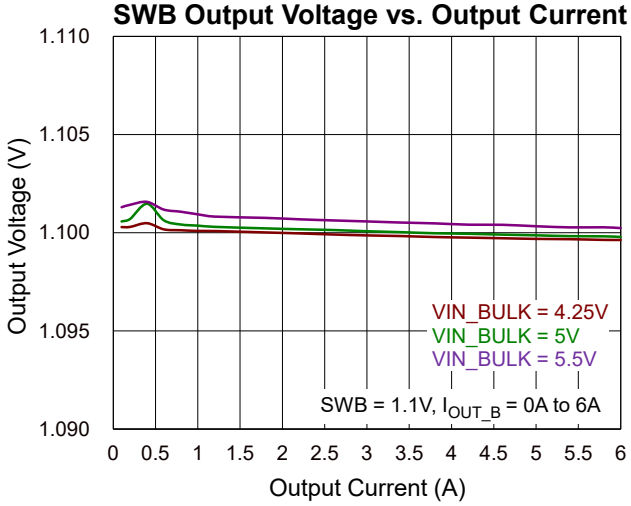
SWC Efficiency vs. Output Current



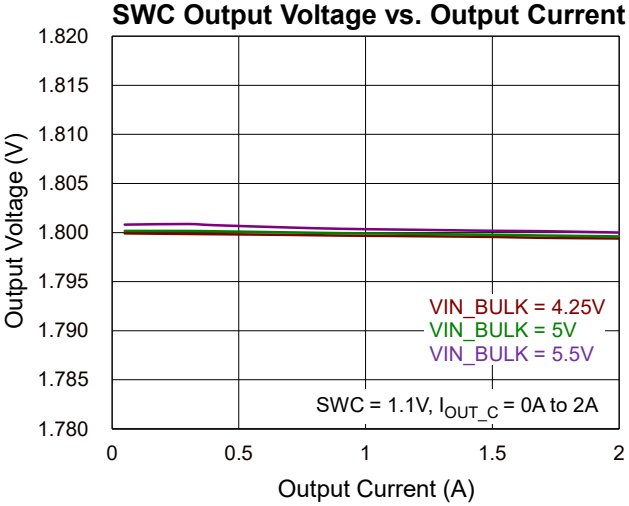
SWA Output Voltage vs. Output Current

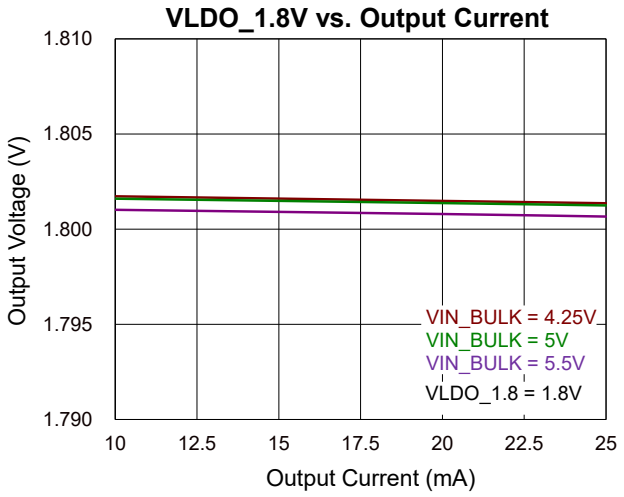


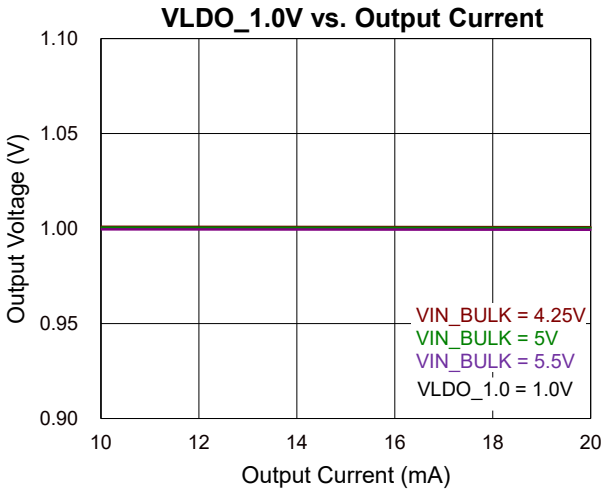
SWB Output Voltage vs. Output Current

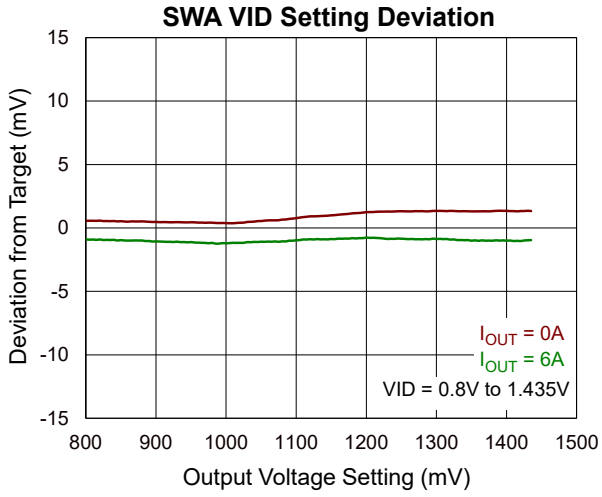


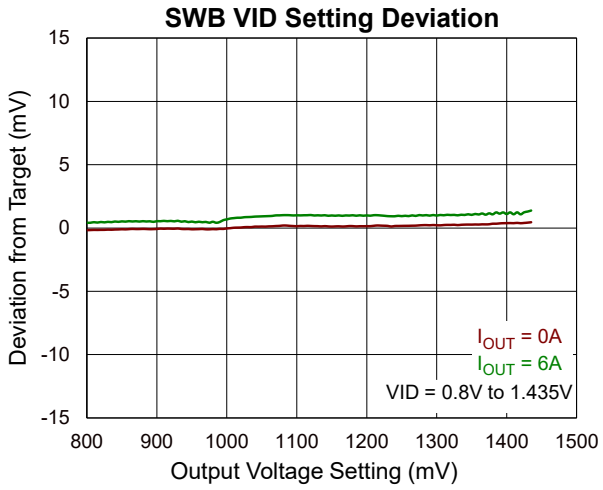
SWC Output Voltage vs. Output Current

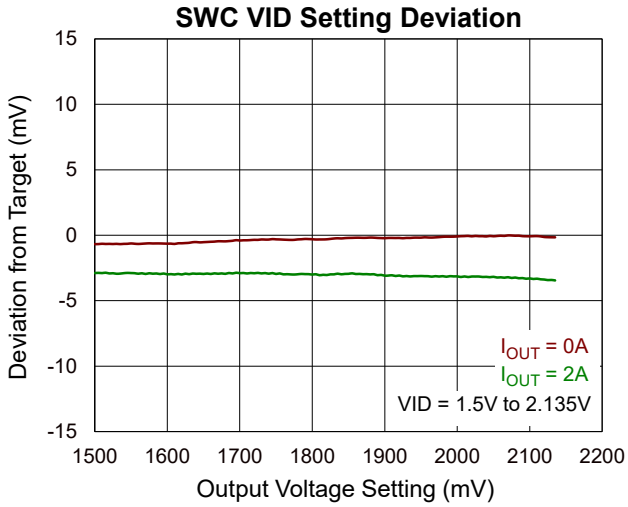


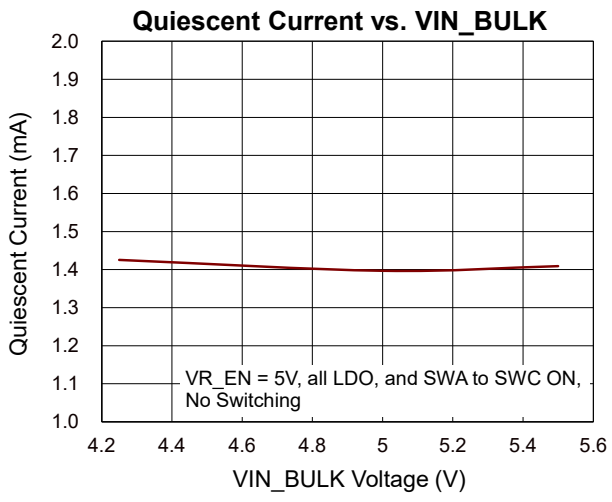




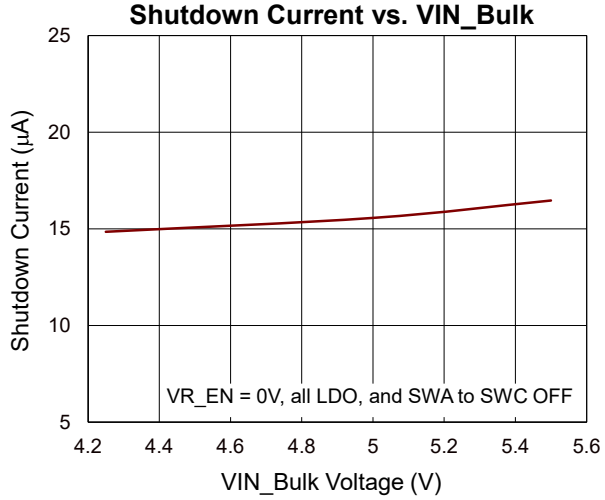




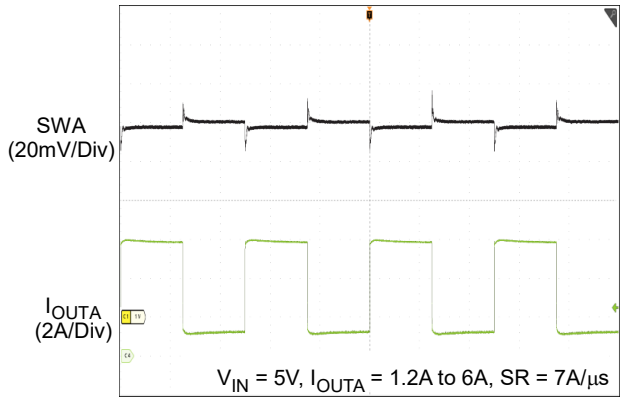




Shutdown Current vs. VIN_Bulk

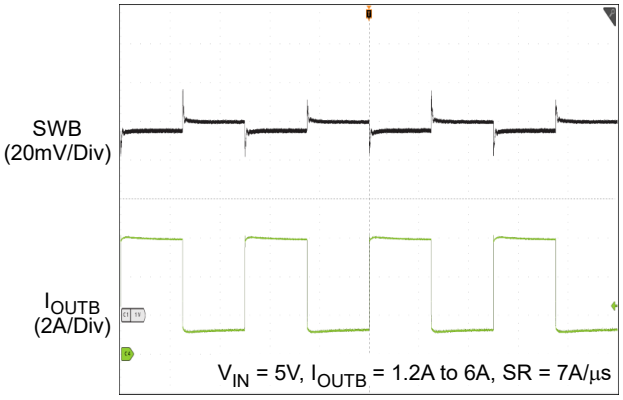


SWA Load Transient Response



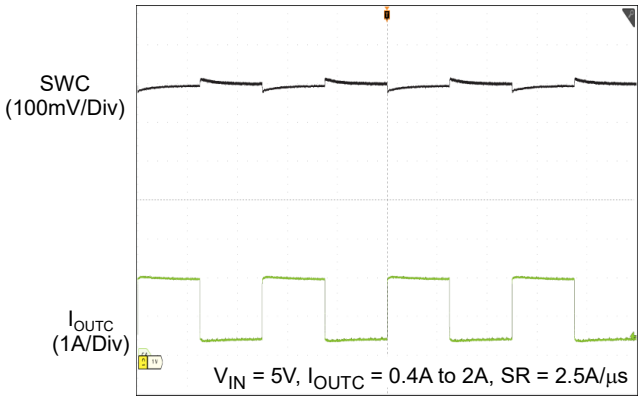
Time (400μs/Div)

SWB Load Transient Response



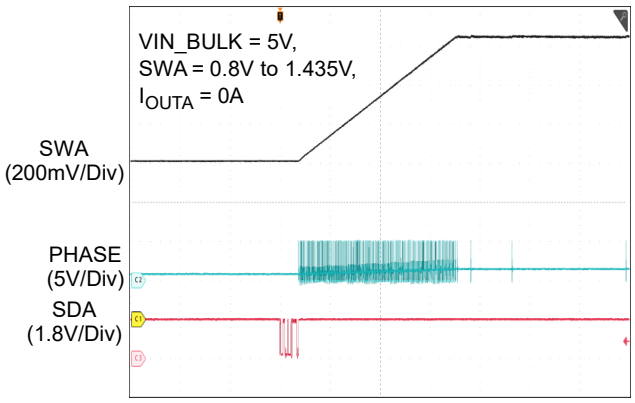
Time (400μs/Div)

SWC Load Transient Response



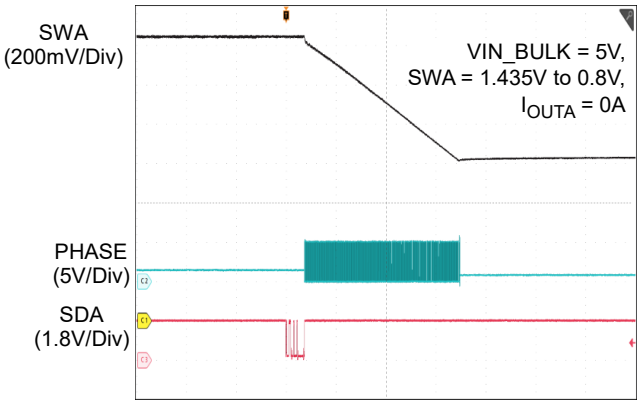
Time (400μs/Div)

SWA VID Up



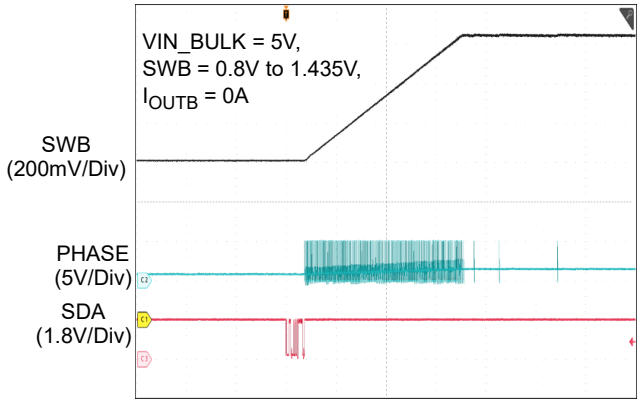
Time (200μs/Div)

SWA VID Down

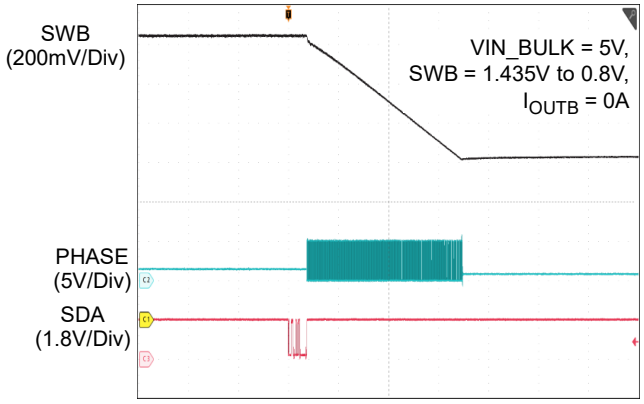


Time (200μs/Div)

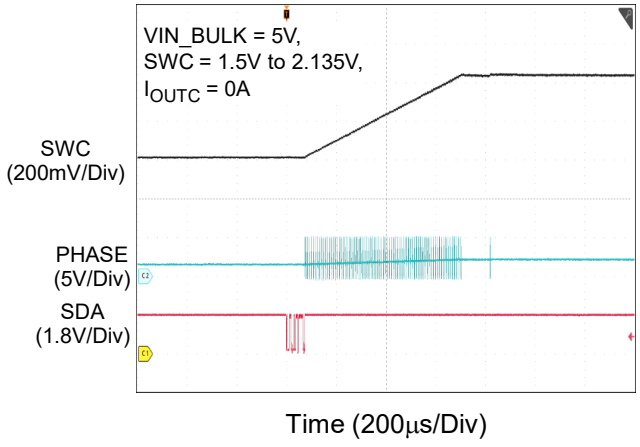
SWB VID Up



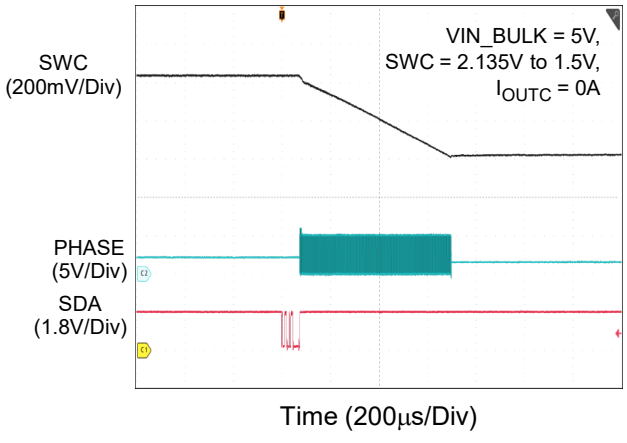
SWB VID Down



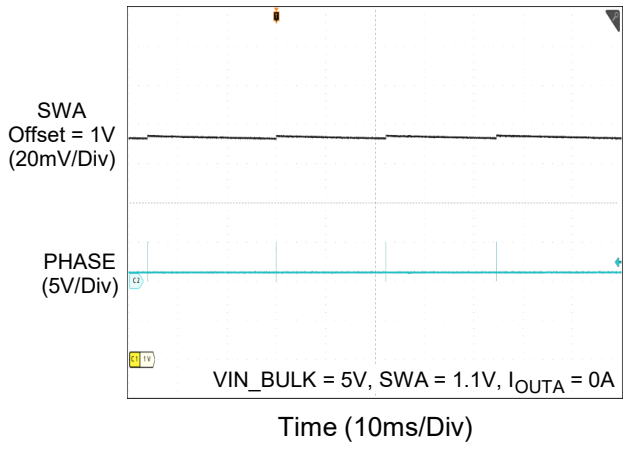
SWC VID Up



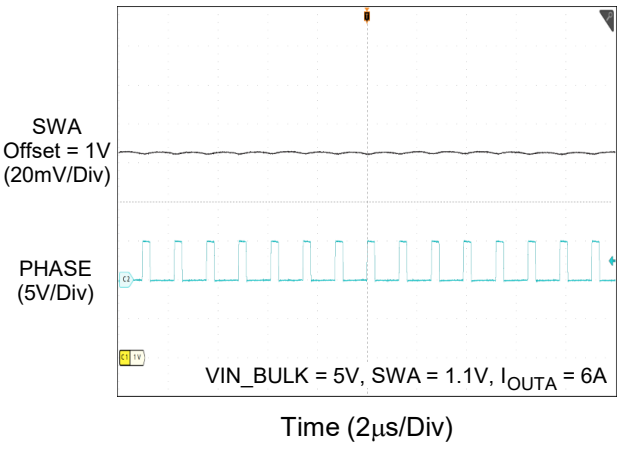
SWC VID Down



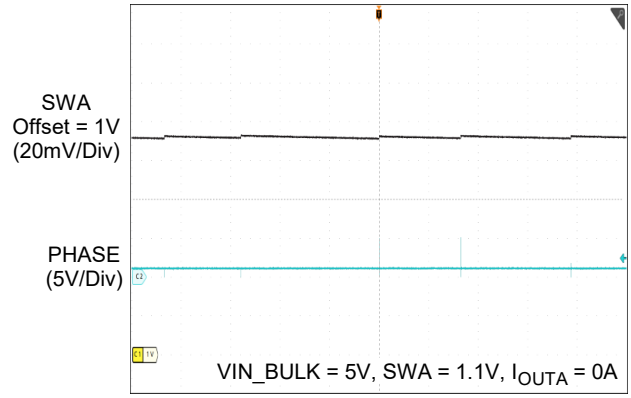
SWA Stability in DEM



SWA Stability in CCM

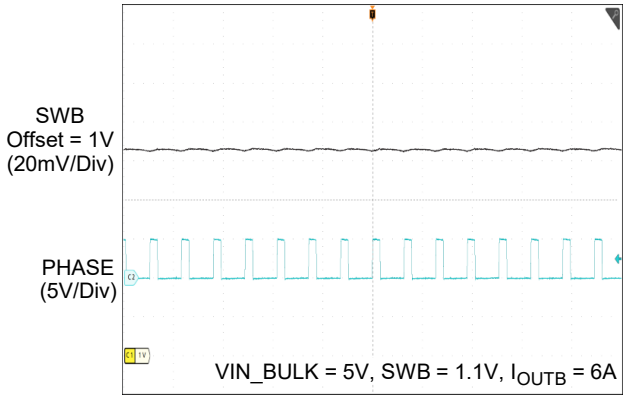


SWB Stability in DEM



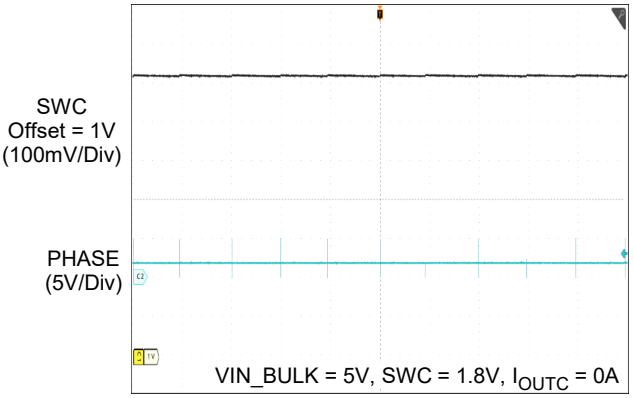
Time (10ms/Div)

SWB Stability in CCM



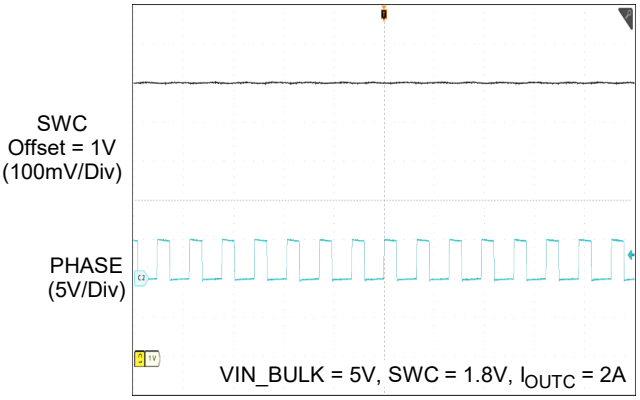
Time (2µs/Div)

SWC Stability in DEM



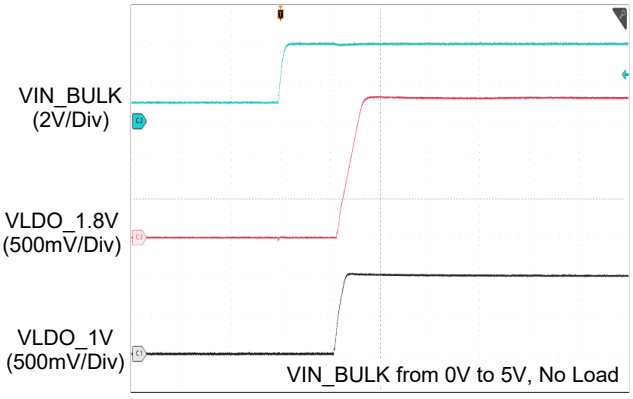
Time (10ms/Div)

SWC Stability in CCM



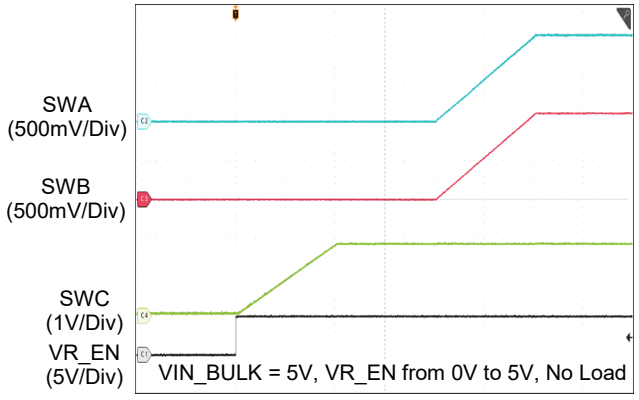
Time (2µs/Div)

VLDO_1.8V and VLDO_1.0V Power-On Sequence



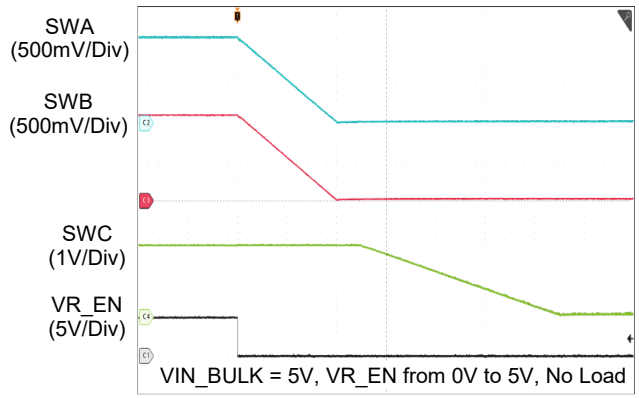
Time (200µs/Div)

PMIC Power-On Sequence by VR_EN

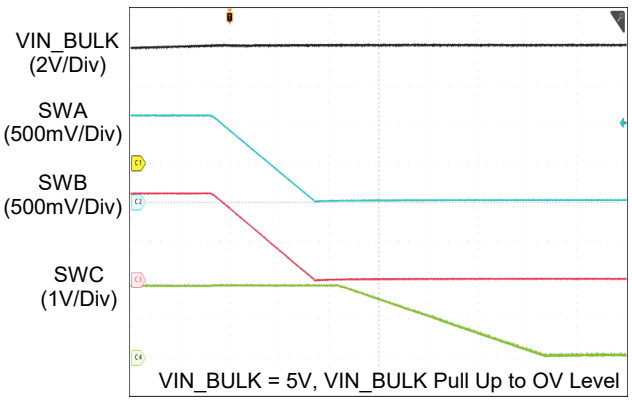


Time (1ms/Div)

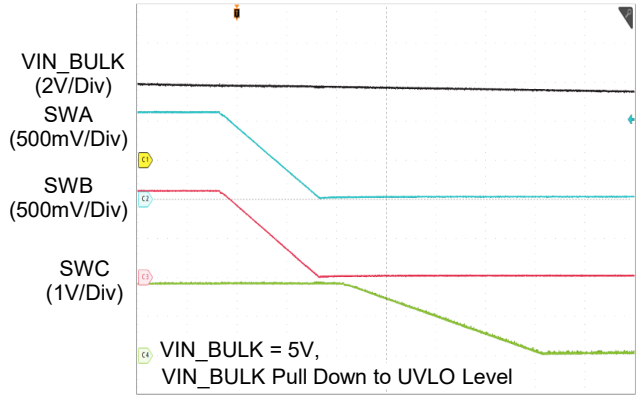
PMIC Power-Off Sequence by VR_EN



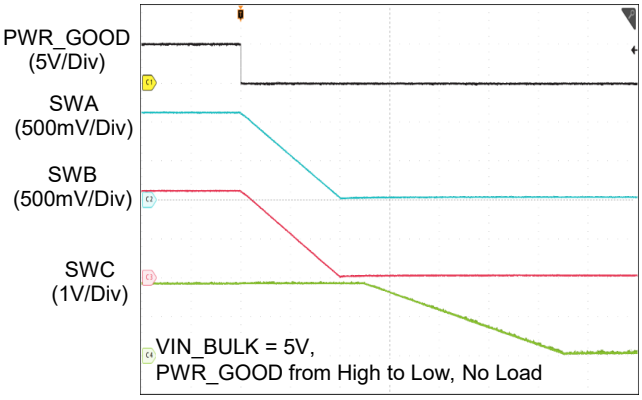
PMIC Power-Off Sequence by VIN_BULK OVP



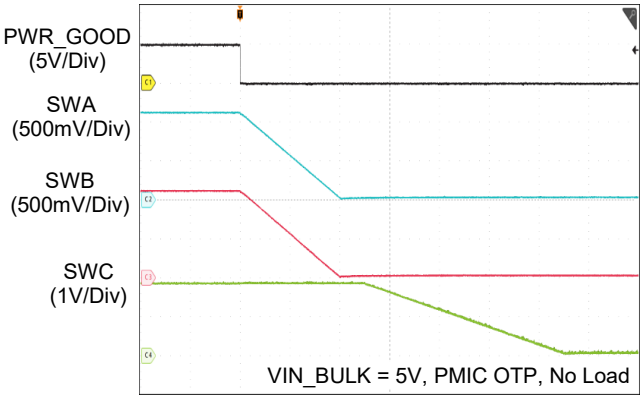
PMIC Power-Off Sequence by VIN_BULK UVLO



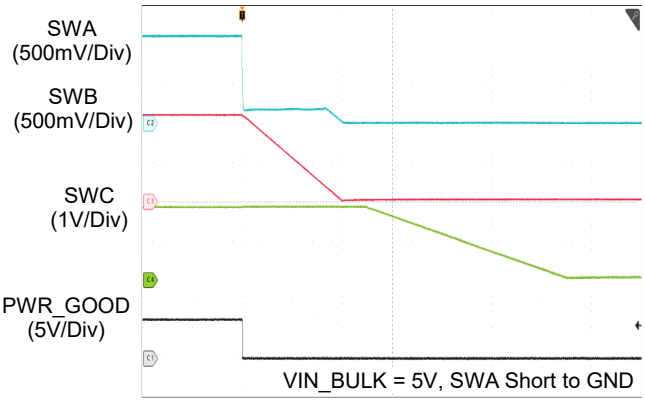
PMIC Power-Off Sequence by PWR_GOOD



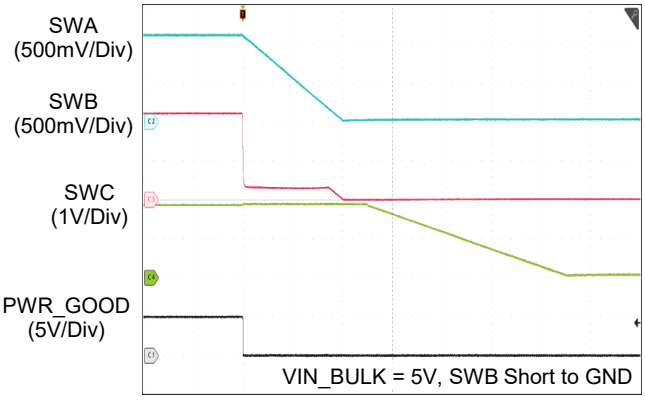
PMIC Power-Off Sequence by OTP



PMIC Power-Off Sequence by SWA Short to GND

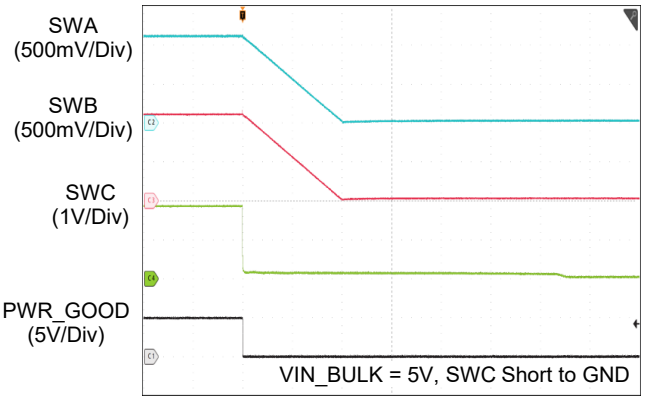


PMIC Power-Off Sequence by SWB Short to GND



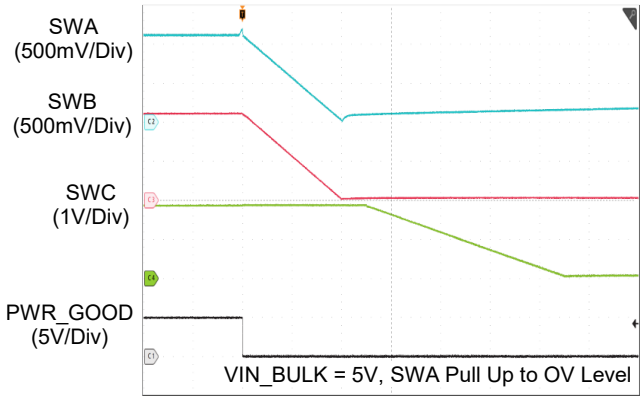
Time (2ms/Div)

PMIC Power-Off Sequence by SWC Short to GND



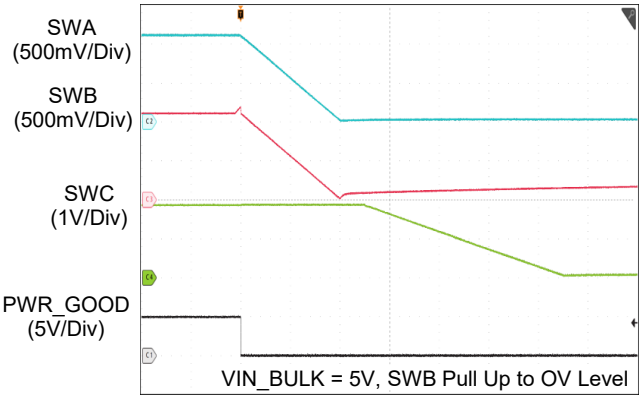
Time (2ms/Div)

PMIC Power-Off Sequence by SWA OVP



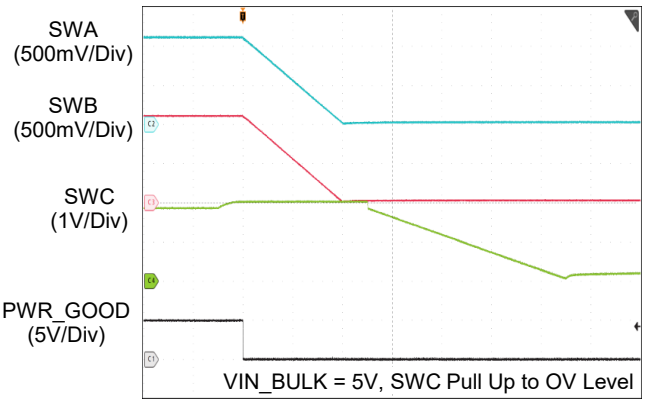
Time (2ms/Div)

PMIC Power-Off Sequence by SWB OVP



Time (2ms/Div)

PMIC Power-Off Sequence by SWC OVP



Time (2ms/Div)

15 Operation

15.1 PMIC Input Voltage Supply and Ramp Condition

The RTQ5162 has one input supply from the platform: VIN_Bulk. The VIN_Bulk supply is used by the RTQ5162 for all three switch (SWA, SWB, SWC) output regulators and two LDO outputs (VOUT_1.8V & VOUT_1.0V) regulators. Note that the VOUT_1.8V LDO output is separate and independent from SWC output, which is for the DRAM VPP rail. The VOUT_1.0V LDO output is separate and independent from SWA or SWB.

At first power on, the VIN_Bulk input supply shall reach a minimum threshold voltage of 4.25V before it can be detected as a valid input supply to the RTQ5162. Once the VIN_Bulk supply is valid and stable, the RTQ5162 shall assert PWR_GOOD output low, drive VOUT_1.8V and VOUT_1.0V supply within t1.8V_Ready and t1.0V_Ready time respectively. The RTQ5162 drives PWR_GOOD output signal low only when VIN_Bulk input supply reaches minimum of 4.25V. The PWR_GOOD output is pulled up to either 1.8V or 3.3V on the platform or on the host controller.

The PWR_GOOD pullup voltage (either 1.8V or 3.3V) can be available before or after VIN_Bulk is valid and stable. If PWR_GOOD pullup voltage is available before VIN_Bulk is applied, the PWR_GOOD signal is High and remains High with no leakage path or damage to the RTQ5162. When VIN_Bulk is applied to the RTQ5162, the RTQ5162 asserts PWR_GOOD output low. The RTQ5162 shall enable I^2C/I3C Basic bus interface function within tManagement_Ready. The host shall not attempt to access the RTQ5162's memory registers until tManagement_Ready timing requirement is satisfied.

15.2 Power-Up Initialization Sequence

During power on, the host shall:

1. Ramp up VIN_Bulk supply.
2. Hold VIN_Bulk supply stable for a minimum of tVIN_Bulk_to_VR_Enable time.
3. Hold VR_EN pin to static low or high. There is no timing relationship required on VR_EN pin with respect to VIN_Bulk input supply ramp up as long as VR_EN pin is held to static level to either low or high.
4. During VIN_Bulk ramp, if VR_EN signal is held low, it can transition to high only once. Once high, it shall remain high. The VR_EN signal is not allowed to transition to low during VIN_Bulk ramp up.
5. If VR_EN pin is held High during VIN_Bulk ramp up or transitions to High during VIN_Bulk ramp up, the RTQ5162 turns on its output rails.
6. If VR_EN pin is held Low during VIN_Bulk Ramp, assert VR_EN signal High to turn on PMIC output rails. Alternatively, host can issue VR Enable command by setting register 0x32 [7] = 1 via I^2C/I3C Basic bus or via DEVCTRL CCC to turn on PMIC output rails.

15.2.1 Power-Up Sequence

Figure 5 to Figure 8 show examples of the RTQ5162 power up initialization sequence. Note that the specific sequence of ramping the output regulators (SWA, SWB, SWC) is for example purpose only. The specific ramp up sequence is configurable through power on sequence configuration registers.

After VR Enable command is registered on the I^2C or I3C Basic bus or VR_EN pin is registered high, the RTQ5162 shall complete the following steps within tPMIC_PWR_GOOD_OUT:

1. Check VIN_Bulk Power Good status is valid.
2. Power up itself: PMIC executes Power On Sequence Config 0 to Power On Sequence Config 2 registers and configures PMIC internal registers as programmed in DIMM vendor memory space registers.
3. Power up all enabled output switch regulators and ready for normal operation.
4. Update status Register 0x08 [5,3:2] and floats PWR_GOOD signal within maximum of tPMIC_PWR_GOOD_OUT time.

If the RTQ5162 PWR_GOOD signal is not floated within tPMIC_PWR_GOOD_OUT time, the host can access the RTQ5162 status registers for detailed information after tPMIC_PWR_GOOD_OUT time. The RTQ5162 may NACK for any host request on I^2C or I3C Basic bus after VR Enable command (either with VR_EN pin high or on I^2C/I3C Basic Bus) until tPMIC_PWR_GOOD_OUT time expires.

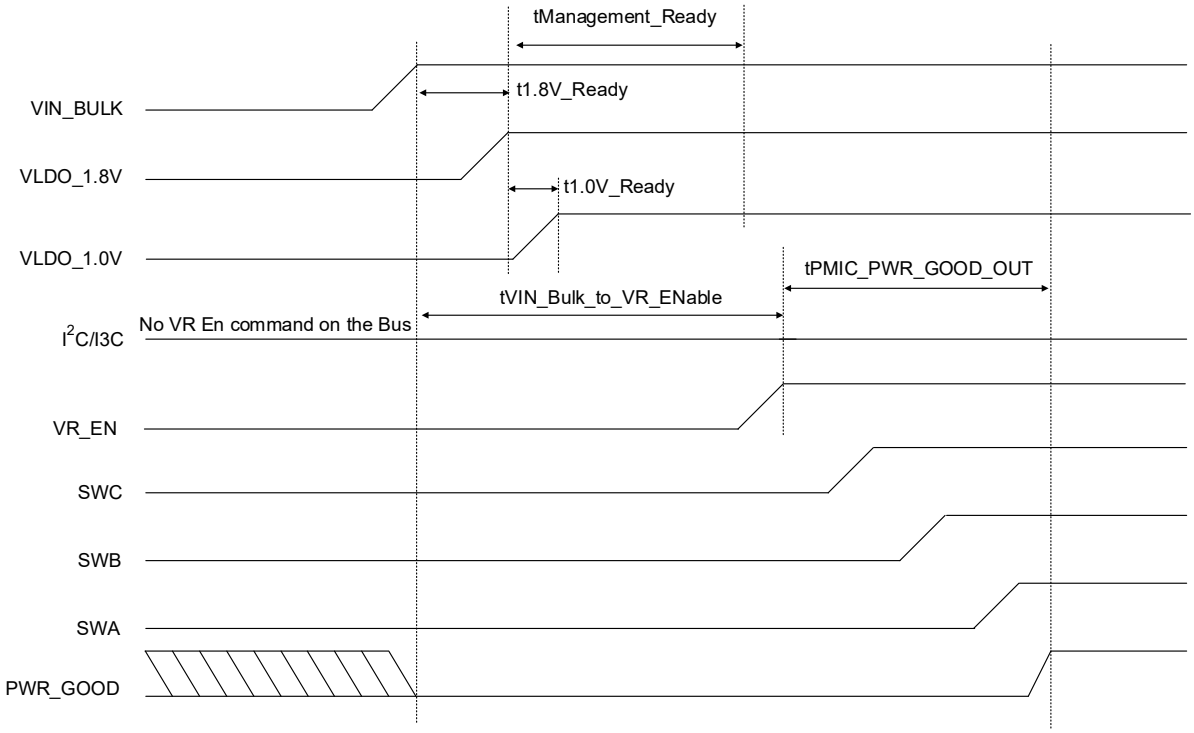


Figure 5. Power-Up Sequence; VR_EN Pin High After VIN_Bulk Ramp; No Bus Command

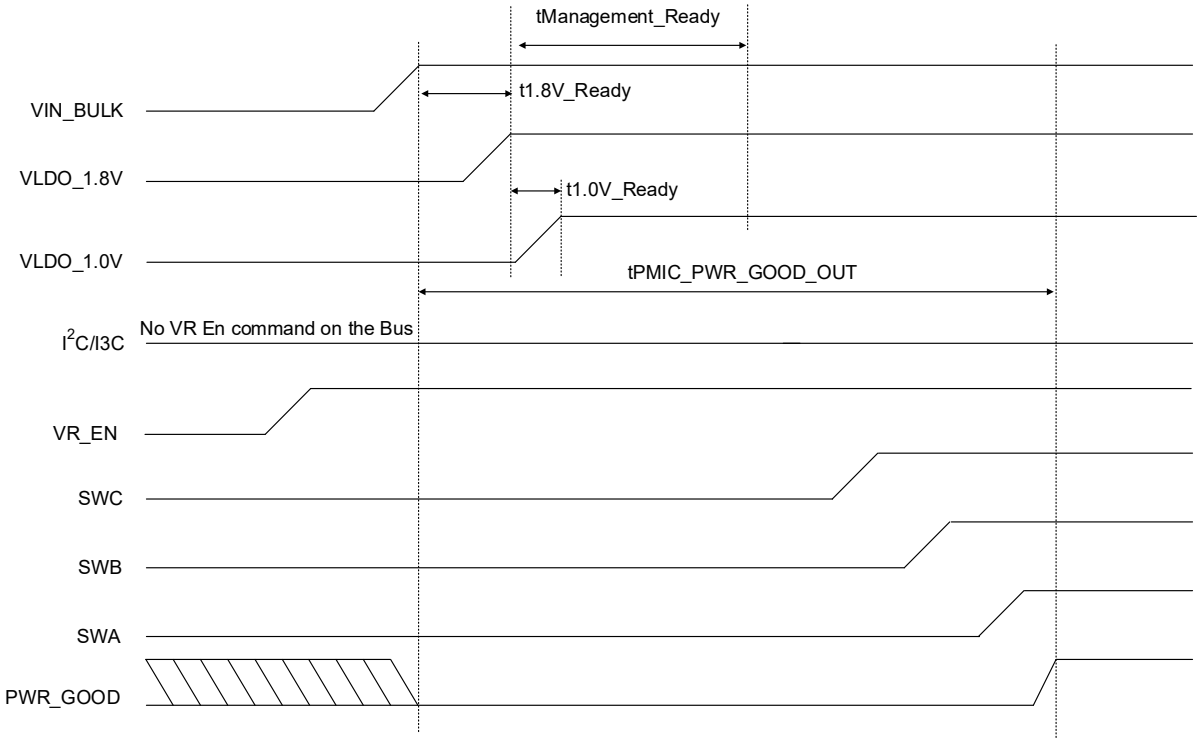


Figure 6. Power-Up Sequence; VR_EN Pin High Before VIN_Bulk Ramp; No Bus Command

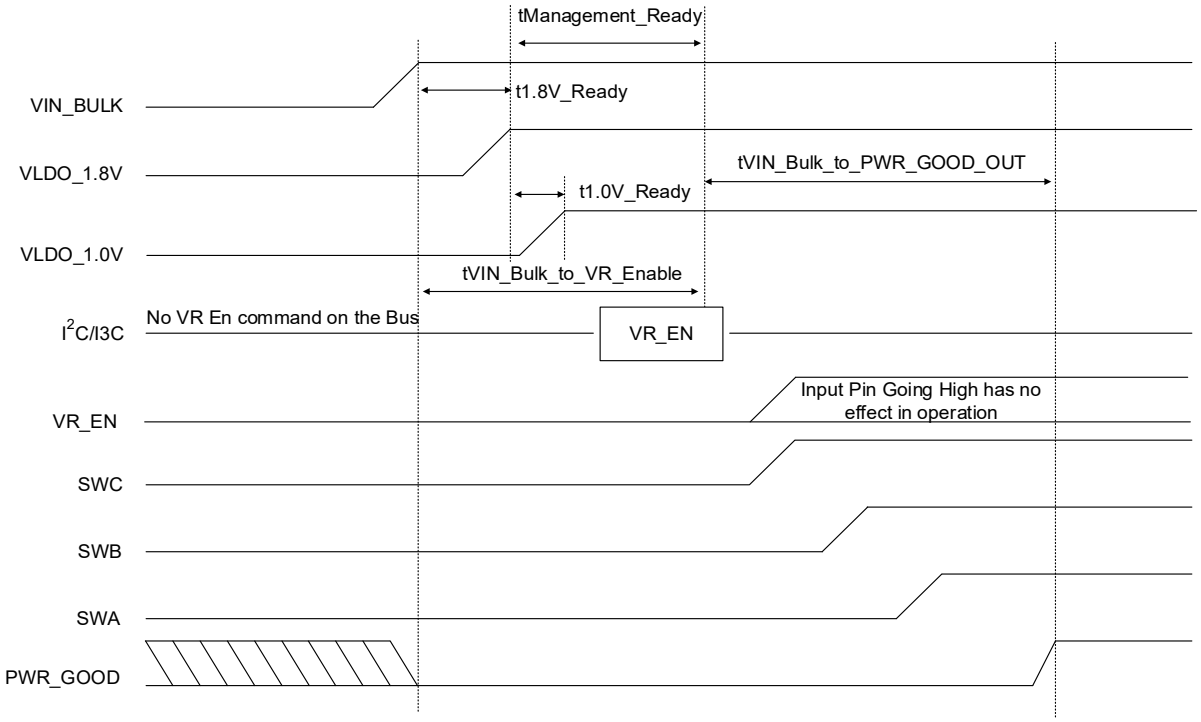


Figure 7. Power-Up Sequence; with Bus Command

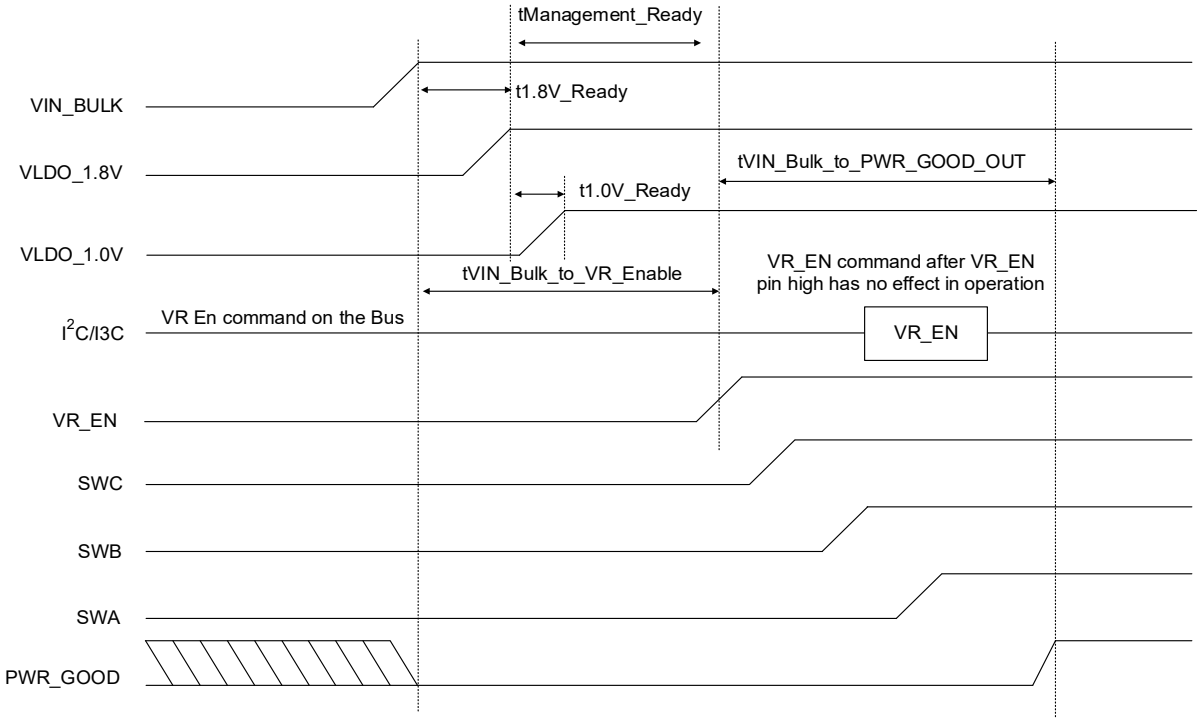


Figure 8. Power-Up Sequence; with VR_EN Pin Followed by Bus Command

15.3 Output Rail Turn On Timing

Figure 9 shows the timing relationship once the RTQ5162 receives VR Enable command (either with VR_EN pin or on (I^2C/I3C Basic bus) and when it floats PWR_GOOD output signal; timing parameter tPMIC_PWR_GOOD_OUT applies. This timing parameter is a sum of maximum soft start time and configured delay for each power on sequence configuration registers that are executed plus additional 5ms timing margin error. The waveform shows each buck regulator output soft start time and delay time once the soft start time expires for each power on sequence config0 to power on sequence config2 registers. Note that if more than one regulators are enabled in a power on sequence config register and if those regulators have different soft start time programmed, then the larger value of that soft start time is used as a reference for delay timer to start. Each regulator will still follow different soft start time to turn on the buck regulator.

The specific example in Figure 9 uses three power on sequence config0 to config2 registers and only one buck regulator is enabled in each power on sequence config 0 to config 2 registers.

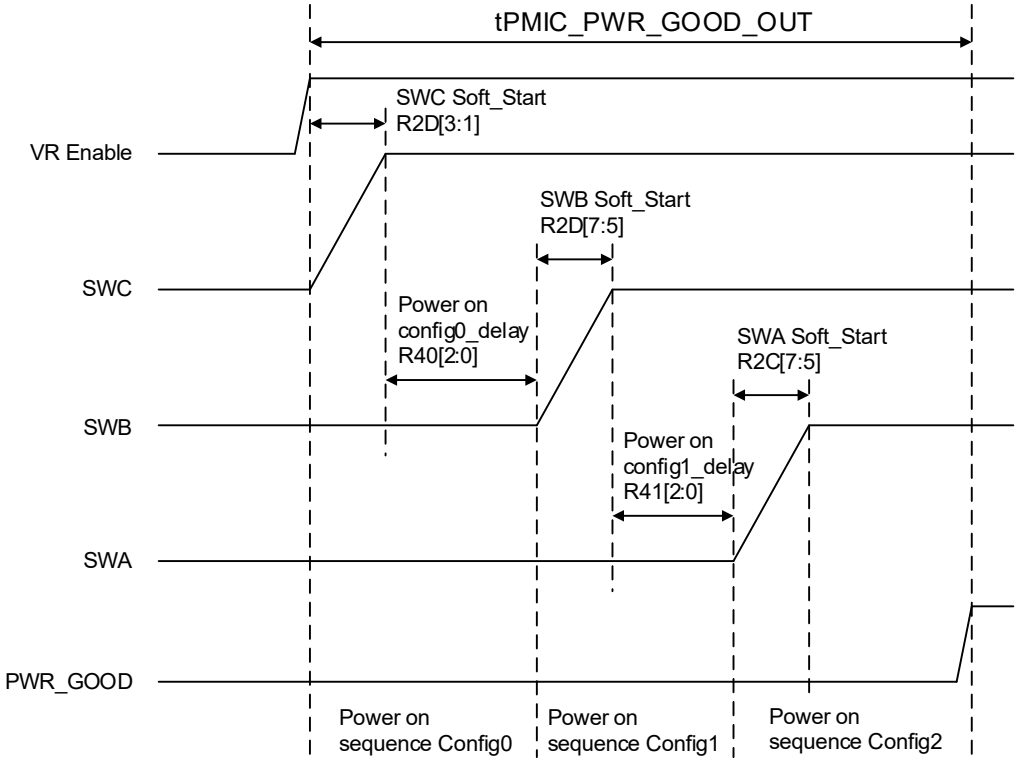


Figure 9. Rails Power On Timing

15.4 Secure Mode and Programmable Mode of Operation

Prior to issuing VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus), the host must configure the Register 0x2F [2] appropriately as desired. The RTQ5162 offers two modes of operation after VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus) is registered.

1. Programmable Mode: In this mode, independent of when host issues VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus), the RTQ5162 allows modification to any register in the host region as desired by the host and the RTQ5162 responds appropriately.
2. Secure Mode: In this mode, after host issues VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus), the RTQ5162 does not allow modification to Register 0x15 to Register 0x2F, Register 0x32 [7,5:0], Register 0x35, or Register 0x36 in the host region as well as Register 0x40 to Register 0x6F in the DIMM vendor region and Register 0x70 through Register 0xFF in the PMIC vendor region. These registers are write-protected.

The PMIC simply ignores the host request. Throughout JEDEC specification, when it refers to as PMIC allows access to the registers, it refers to write operation to the registers that are not write-protected in secure mode or programmable mode. There is no restriction for the read operation in secure mode or programmable mode. The host must power cycle the PMIC to make any modifications to the registers. The PMIC power cycle is defined as complete removal of VIN_Bulk input supply to the PMIC and this definition is applied to the entire specification.

The Secure Mode is only applicable once VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus) is registered. This is important because by default Register 0x2F [2] = 0 when PMIC is first powered up. Prior to VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus), PMIC allows modification to any registers in the host region.

Note that there is one exception in Secure mode of operation. The exception is for Register 0x32[7]. This register can get updated with VR_EN pin assertion/de-assertion or PWR_GOOD signal input assertion to low or when PMIC internally generates its own VR Disable command due to some fault condition. This register cannot be updated with I^2C or I3C Basic bus command or with DEVCTRL CCC command.

15.5 Power-Down Output Regulators

Under normal operating condition with valid VIN_Bulk input supply, to disable the PMIC output regulators, the RTQ5162 allows the following three methods for normal power-down sequence.

- VR_EN pin de-assertion from High to Low
- VR Disable command on I^2C or I3C bus (if PMIC registers are not in secure mode)
- PWR_GOOD input from High to Low (if PWR_GOOD pin is configured as IO)

All three methods trigger the RTQ5162 to generate an internal VR Disable command, after which the RTQ5162 executes the normal power down sequence as programmed in Power Off Sequence Config0 to Power Off Sequence Config2 (Register 0x58 to Register 0x5A), in DIMM vendor region MTP memory.

The PMIC requires a valid VIN_Bulk input supply (i.e., minimum of 4.25V) to execute the normal power down sequence. In a platform where the VIN_Bulk input supply ramp down rate is very slow (starting from VIN_Bulk nominal condition of 5V until it ramps down to 4.25V), the PMIC may be able to execute the normal power down sequence before the VIN_Bulk input supply is completely removed, depending on the ramp down rate, programmed soft stop time, and the delay time in the Power Off Sequence Config registers. If the VIN_Bulk ramp down is very fast (e.g., instantaneous with 0ns), the PMIC cannot execute the normal power down sequence to turn off all buck regulators. Figure 10 shows one example of a normal power down sequence where PMIC regulators are turned off by de-asserting the VR_EN pin from high to low. The PMIC executes Power Off Sequence Config0 to Power Off Sequence Config2 (Register 0x58 to Register 0x5A). The example shows the power down sequence spread out over all three Power Off Sequence Config (0 to 2) registers where only one buck regulator is turned off in each Power Off Sequence Config register. The sequence shows the order where SWA is turned off first followed by delay. Then SWB is turned off followed by delay. Lastly. SWC is turned off followed by delay. Each buck regulator follows its own timing for soft stop time, as configured. The PMIC allows any combination where all three buck regulators can be turned off only in the first Power Off Sequence Config0 register, or one or more buck regulators can be turned off in any given Power Off Sequence Config register.

See additional details about PMIC register status, PWR_GOOD signal, as noted in 15.5.1 to 15.5.4, depending on how the PMIC is configured to operate in normal mode.

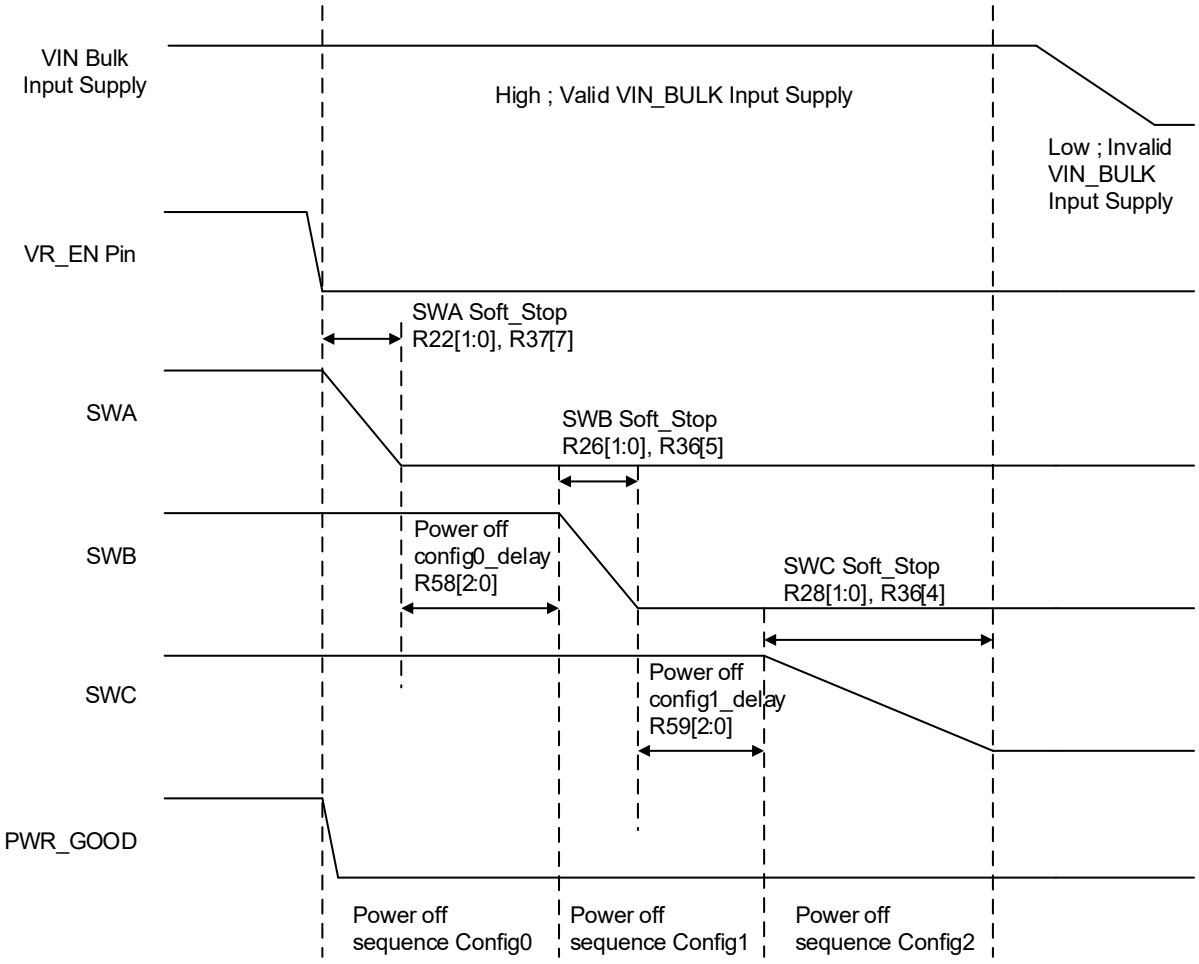


Figure 10. Normal Power Down Sequence with VR Disable Command

15.5.1 Programmable Mode Operation; R1A[4]=0

The RTQ5162 allows host to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (Register 0x32 [7] = 0 or VR_EN pin transitions to low). The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers.

   The PMIC controls the PWR_GOOD signal as following in bullet a and bullet b:

   a. If VR Disable command with a pin (i.e., VR_EN pin transitions to Low), PMIC asserts PWR_GOOD signal Low. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.

   b. If VR Disable command on a I^2C/I3C Bus (i.e., Register 0x32 [7] = 0), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The host can re-enable the PMIC's output regulators by issuing VR_EN command on the I^2C/I3C bus (i.e., Register 0x32 [7] = 1).

      The PMIC executes power on sequence config0 to power on sequence config2 registers and continues to float the PWR_GOOD signal until tPMIC_PWR_GOOD_OUT time at which point, PMIC assumes normal control of PWR_GOOD signal. The PMIC does not require power cycle

c. The simultaneous usage of VR_EN pin and I²C/I3C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet a and PWR_GOOD signal remains low even if there is a subsequent I²C/I3C bus command as described in bullet b.

2. Configuring one or more bits in Register 0x2F [6,4:3] to 0 in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in Register 0x2F [6,4:3] to 1 in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating.
3. If Register 0x32 [5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. If host re-enables PMIC's output regulators by issuing VR_EN command on the I²C/I3C Basic bus (i.e., Register 0x32 [7] = 1), the PMIC executes power on sequence config0 to power on sequence config2 registers and floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 7 under column 'Trigger VR Disable'. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers. The PMIC asserts PWR_GOOD signal low. The host can re-enable PMIC's output regulators with VR Enable command with either Register 0x32 [7] =1 or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

15.5.2 Programmable Mode Operation; R1A[4]=1

The RTQ5162 allows host to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (Register 0x32 [7] =0 or VR_EN pin transitions to low). The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The PMIC controls the PWR_GOOD signal as following in bullet a and bullet b:
   a. If VR Disable command with a pin (i.e., VR_EN pin transitions to Low), PMIC asserts PWR_GOOD signal Low. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.
   b. If VR Disable command on a I²C/I3C Basic Bus (i.e., Register 0x32 [7] =0), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The PMIC exits from P1 state with only VR_EN pin transition to High. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High and PMIC executes power on sequence config 0 to power on sequence config 2 registers. The PMIC continues to float PWR_GOOD signal until tPMIC_PWR_GOOD_OUT timing parameter is satisfied and at that point PMIC assumes normal control of PWR_GOOD signal. The PMIC does not require power cycle.

c. The simultaneous usage of VR_EN pin and I²C/I3C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet a and PWR_GOOD signal remains low even if there is a subsequent I²C/I3C bus command as described in bullet b.

2. Configuring one or more bits in Register 0x2F [6,4:3] to 0 in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in Register 0x2F [6,4:3] to 1 in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating.
3. If Register 0x32 [5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. The PMIC does not enter in P1 state. If host re-enables PMIC's output regulators by issuing VR_EN command on I²C/I3C Basic bus (i.e., Register 0x32 [7] = 1), the PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 7 under column "Trigger VR Disable". The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The host can re-enable PMIC's output regulators with VR Enable command with either Register 0x32 [7] = 1 or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

15.5.3 Secure Mode Operation; R1A[4]=0

The RTQ5162 allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC executes power on sequence config0 to power on sequence config2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.
    1. Note that VR Disable or Enable command on a I²C/I3C Basic Bus (i.e., Register 0x32 [7] = 0 or 1) has no effect on the PMIC. Also, configuring one or more bits in Register 0x2F [6,4:3] to 0 has no effect on the PMIC.
2. If Register 0x32 [5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only Register 0x32 [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write-protected registers locked except for the Register 0x32 [7]. When host issues VR Enable command by I²C/I3C Basic bus, the PMIC executes Power on sequence config0 to Power on sequence config2 registers, floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks Register 0x32 [7]. The PMIC does not require power cycle to re-enable PMIC's output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 7 under column “Trigger VR Disable”. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either Register 0x32 [7] = 1 or VR_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

15.5.4 Secure Mode Operation; R1A[4]=1

The RTQ5162 allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and executes power on sequence config0 to config2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.
   a. Note that VR Disable or Enable command on a I^2C/I3C Basic Bus (i.e., Register 0x32 [7] = 0 or 1) has no effect on the PMIC. Also, configuring one or more bits in Register 0x2F [6,4:3] to ’0’ has no effect on the PMIC.
2. If Register 0x32 [5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only Register 0x32 [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write-protected registers locked except for the Register 0x32 [7]. The PMIC does not enter in P1 state. When host issues VR Enable command by I^2C/I3C Basic bus, the PMIC executes Power on sequence config0 to Power on sequence config2 registers, floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks Register 0x32 [7]. The PMIC does not require power cycle to re-enable PMIC’s output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 7 under column “Trigger VR Disable”. The PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either Register 0x32 [7] = 1 or VR_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

15.6 PMIC Output Rail Off Timing

Figure 11 shows the timing relationship once the PMIC registers VR Disable command internally due to fault condition as listed in Table 7. The waveform shows each buck regulator output soft stop time and delay time once the soft stop time expires from each power off sequence config0 to power off sequence config2 registers. Note that if more than one regulators are disabled in a power off sequence config register and if those regulators have different soft stop time programmed, then the larger value of that soft stop time is used as a reference for delay timer to start. Each regulator will still follow different soft stop time to turn off the buck regulator. The specific example in Figure 11 uses only three power off sequence config0 to config2 registers and only one buck regulator is disabled in power off sequence config0, config1 and config2 registers.

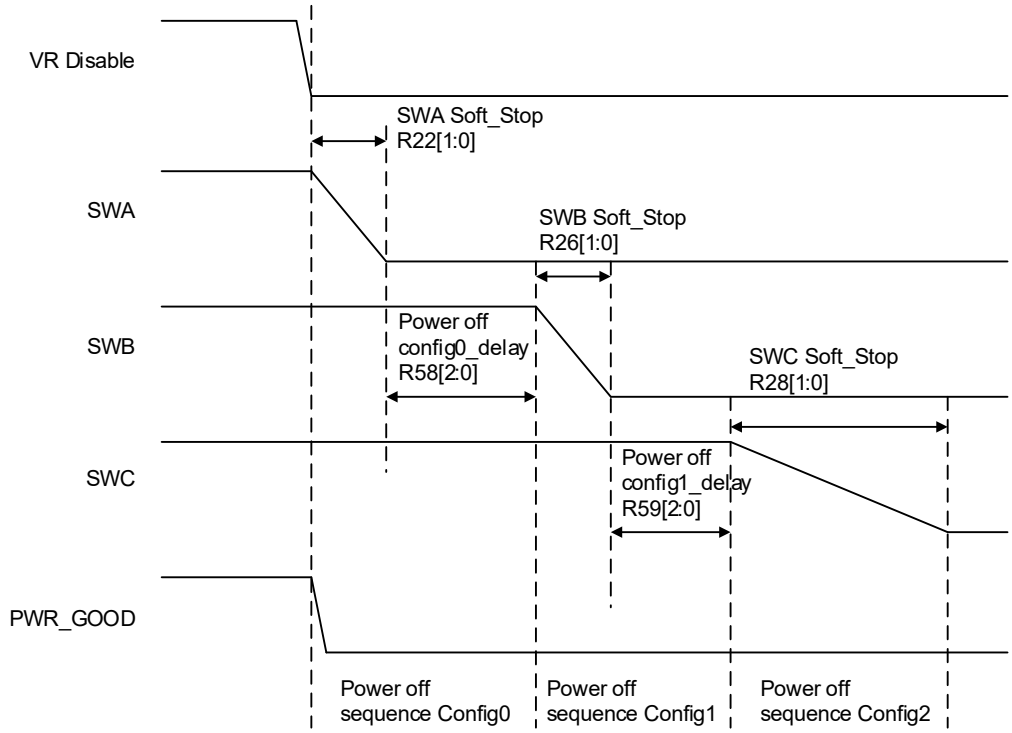


Figure 11. Power Off Timing Due to Internal Fault Condition

15.7 Power Down Output Regulators During Power-On Sequence

During power on as described in 15.2 it is possible that RTQ5162 can trigger VR Disable command on its own as described in Table 7 when one or more regulators are already turned on even while other remaining output regulators are not yet turned on because PMIC has not completed the power on sequence config registers. For these type of cases, the PMIC will not execute the remaining power on sequence config registers and will immediately jump to executing the power off sequence config0 to power off sequence config2 registers. The PMIC will update the status registers and error log registers appropriately as normal because it generated VR Disable command on its own. The PWR_GOOD output signal would remain low.

15.8 Power-Good (PWR_GOOD) Signal

The PWR_GOOD output signal type can be configured as either output only or input and output through Register 0x32 [5]. By default, PWR_GOOD is an output signal. The PWR_GOOD signal can only be configured once, at power on, before issuing VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus). The PWR_GOOD signal configuration applies to both secure mode or programmable mode of operation.

15.8.1, 15.8.2, Table 4, and Table 5 describe PMIC's behavior.

Table 4. RTQ5162 Operation ; PWR_GOOD Type: Input and Output

External PWR_GOOD Input	PMIC's Internal PWR_GOOD	PMIC Operation
High	High	High (Power Good); Normal Operation
High	Low	Low (Power Not Good); PMIC Communicates its Status;
Transition from High to Low	High	Low(Power Good); PMIC Executes VR Disable Command
Low	Low	Low (Power Not Good); PMIC Internally Generates VR Disable Command

Table 5. RTQ5162 Operation ; PWR_GOOD Type: Output Only

External PWR_GOOD Input	PMIC's Internal PWR_GOOD	PMIC Operation
X (High or Low)	High	(Power Good); Normal Operation
X (High or Low)	Low	(Power Not Good); PMIC Communicates its Status

15.8.1 PWR_GOOD as Output Only Signal

When Register 0x32 [5] = 0, the PWR_GOOD signal type is output only; the input of PWR_GOOD signal is ignored. The RTQ5162 PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V). The PMIC floats PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator's (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) tolerances are maintained as configured in the appropriate register space. At first power up, when input supply VIN_Bulk is ramped up and stable, the PMIC keeps PWR_GOOD pin asserted to low; however PMIC updates corresponding status register. By default, the Register 0x32 [5] = 0. Once PMIC receives VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus) from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters into operating state called as "Regulation". At this point, PMIC floats PWR_GOOD pin and the external board pullup resistor pulls the pin high as there may be other PMIC on different DIMM may be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e., no other PMIC is driving the PWR_GOOD pin low), the PMIC remains in "Regulation" state. Once the PWR_GOOD pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) that causes the PMIC to update its status registers to indicate the power status is not good, then PMIC asserts PWR_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR_GOOD pin float (i.e., get High) even if the condition that triggered the PMIC to assert the PWR_GOOD pin no longer exists. In other words, the PMIC's PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the host.

15.8.2 PWR_GOOD as Input and Output Signal

When Register 0x32 [5] = 1, the PWR_GOOD signal type is both input and output and is only applicable after host issues VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus). Also note that simultaneous usage of the PWR_GOOD pin as IO and the VR_EN pin is not allowed and considered an illegal configuration. In other words, if the VR_EN pin is intended to be used to turn on and turn off output rails, the PWR_GOOD pin must be configured as output only. If the PWR_GOOD pin is intended to be used as IO, the VR_EN pin must be connected to GND on the board. The PMIC PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V). The PMIC floats the PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator's (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) tolerances are maintained as configured in the appropriate register space.

At first power up, when input supply VIN_Bulk is ramped up and stable, the PMIC keeps the PWR_GOOD pin asserted to low; however PMIC updates corresponding status register. The host, prior to issuing VR Enable command on I²C/I3C Basic bus, can configure the Register 0x32 [5] = 1. When host issues VR Enable command on I²C/I3C Basic bus, the PMIC turns on its output regulators and updates corresponding status registers and enters into operating state called "Regulation". At this point, the PMIC floats the PWR_GOOD pin and waits for the external board pullup resistor to pull the pin high as there may be other PMICs on different DIMMs that may

be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e., no other PMIC is driving the PWR_GOOD pin low), the PMIC automatically enters in to operating state called “Bulk Control Link Monitor”. Once the PWR_GOOD pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) that causes the PMIC to update its status registers to indicate the power status is not good, then the PMIC asserts the PWR_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR_GOOD pin float (i.e., get High) even if the condition that triggered the PMIC to assert the PWR_GOOD pin no longer exists. In other words, the PMIC’s PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the host. In this “Bulk Control Link Monitor” operating state, the PMIC’s behavior is as follows:

If the PMIC is operating in Secure mode of operation, see 15.5.3 and 15.5.4 for additional information.

- The PMIC allows the PWR_GOOD input signal low at any time. The host must keep the PWR_GOOD signal low for a minimum of tPWR_GOOD_Low_Pulse_Width to issue a command to the PMIC to execute VR Disable. When the PMIC detects the PWR_GOOD signal low, the PMIC internally triggers a VR Disable command, shuts off all output regulators (the PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A), drives the PWR_GOOD signal low, and unlocks only Register 0x32 [7].
- The PMIC preserves all register contents including the MTP error log registers and keeps all writeprotected registers locked except for the Register 0x32 [7]. As long as there is a valid VIN_Bulk input supply, the PMIC allows read access to all its configuration registers. The PMIC allows write access to non-locked configuration registers and Register 0x32 [7]. If the host issues a VR Enable command on the I^2C/I3C bus, the PMIC executes the Power on sequence config0 to Power on sequence config2 registers, floats the PWR_GOOD signal and re-locks Register 0x32 [7].

  If the PMIC is in Programmable mode of operation, see 15.5.1 and 15.5.2 for additional information.

- The PMIC allows the PWR_GOOD input signal low at any time. The host must keep the PWR_GOOD signal low for a minimum of tPWR_GOOD_Low_Pulse_Width to issue a command to the PMIC to execute VR Disable. When the PMIC detects the PWR_GOOD signal low, the PMIC internally triggers a VR Disable command, shuts off all output regulators (the PMIC executes power off sequence config0 (Register 0x58) to power off sequence config2 (Register 0x5A)), and drives the PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. As long as there is a valid VIN_Bulk input supply, the PMIC allows read and write access to all its configuration registers. The host can issue a VR_EN command on the I^2C/I3C Basic bus (i.e.,Register 0x32 [7] = 1) again to turn on the PMIC’s output regulator, and the PMIC will execute the Power On Config0 to Config2 registers and float the PWR_GOOD signal.

15.9 Idle Condition and Quiescent Power State

Quiescent Power State definition: All circuits including PMIC switch output and LDO output regulators are off. VR_EN signal is at static low or high level. I^2C or I3C Basic interface access is not allowed and is pulled high. PID signal is at static low or high level. This state is only applicable if Register 0x1A [4] = 1. This state is labeled as P1 state.

Idle Condition definition: All circuits including PMIC switch output and LDO output regulators are on with 0 A load. VR_EN signal is at static low or high level. I^2C or I3C Basic interface access is allowed but bus is pulled high. PID signal is at static low or high level. The state transitions from each state is defined in Table 6.

Table 6. Power State Definition

State	Description
P0	1. VIN_Bulk is invalid
P1	1. 0x1A[4] = 1 2. Entry from P3 State Only
P2_B	1. Transition from P0 or P1 State; Before VR Enable Command 2. All Switch Regulators are OFF 3. All LDOs are ON 4. PWR_GOOD Output = L 5. VR_EN Input = L 6. 0x32[7] = 0
P2_A1 (No Fault Event)	1. Transition from P3; After VR Enable Command 2. All Switch Regulators are OFF 3. All LDOs are ON 4. PWR_GOOD Output = L or H 5. VR_EN Input = L or H 6. 0x32[7] = 0
P2_A2 (Fault Event)	1. Transition from P3; After VR Enable Command 2. All Switch Regulators are OFF 3. All LDOs are ON 4. PWR_GOOD Output = L 5. VR_EN Input = L or H 6. 0x32[7] = 0
P3 (Regulation Mode or Bulk Control Link Monitor Mode)	1. All Switch Regulators are ON 2. 0x32[7] = 1

15.10 GSI_n Signal

General Status Interrupt (GSI_n) is an Open Drain output signal. By default at power on, GSI_n output is disabled. The host can enable the GSI_n output by setting Register 0x1B [3] = 1. Typically, GSI_n output is pulled up to 1kΩ resistor to 1.8V or 3.3V. The PMIC asserts GSI_n output for the events as described in Table 7.

15.11 Function Interrupt: PWR_GOOD and GSI_n Output Signals

This section defined the output functionality of GSI_n pin and PWR_GOOD (Register 0x32 [5] = 0) pin. When mask register bits are not set, the PMIC asserts its GSI_n output and assert PWR_GOOD output signals as shown in Table 7 when any event occurs. The table also highlights 9 events that cause the PMIC to internally generate a VR Disable command. For remaining events that do not trigger internal VR Disable command, the PMIC continues to operate as normal.

Table 7. Events Interrupt Summary

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	Trigger VR Disable?	PWR_GOOD Output	GSI_n
VIN_BULK Overvoltage	0x08[0]	0x10[0]	0x15[0]	0x1B[7]	Yes	Low	Low
SWA Output Power Good	0x08[5]	0x10[5]	0x15[5]	0x21[0], 0x22[7:6]	No	Low	Low

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	Trigger VR Disable?	PWR_GOOD Output	GSI_n
SWB Output Power Good	0x08[3]	0x10[3]	0x15[3]	0x25[0], 0x26[7:6]	No	Low	Low
SWC Output Power Good	0x08[2]	0x10[2]	0x15[2]	0x27[0], 0x28[7:6]	No	Low	Low
1.8V LDO Power Good	0x09[5]	0x11[5]	0x16[5]	0x1A[2]	No	Low	Low
1.0V LDO Power Good	0x33[2]	0x14[2]	0x19[2]	0x1A[0]	No	Low	Low
SWA Output Overvoltage	0x0A[7]	0x12[7]	0x17[7]	0x22[5:4]	Yes	Low	Low
SWB Output Overvoltage	0x0A[5]	0x12[5]	0x17[5]	0x26[5:4]	Yes	Low	Low
SWC Output Overvoltage	0x0A[4]	0x12[4]	0x17[4]	0x28[5:4]	Yes	Low	Low
SWA Output Undervoltage	0x0B[3]	0x13[3]	0x18[3]	0x22[3:2]	Yes	Low	Low
SWB Output Undervoltage	0x0B[1]	0x13[1]	0x18[1]	0x26[3:2]	Yes	Low	Low
SWC Output Undervoltage	0x0B[0]	0x13[0]	0x18[0]	0x28[3:2]	Yes	Low	Low
VIN_BULK Input Undervoltage	0x33[3]	0x14[3]	0x19[3]	3.5V	Yes	Low	Low
SWA Output Current Limit	0x0B[7]	0x13[7]	0x18[7]	0x20[7:6]	No	High	Low
SWB Output Current Limit	0x0B[5]	0x13[5]	0x18[5]	0x20[3:2]	No	High	Low
SWC Output Current Limit	0x0B[4]	0x13[4]	0x18[4]	0x20[1:0]	No	High	Low
SWA Output High Current /Power	0x09[3]	0x11[3]	0x16[3]	0x1C[7:0]	No	High	Low
SWB Output High Current /Power	0x09[1]	0x11[1]	0x16[1]	0x1C[7:0]	No	High	Low
SWC Output High Current /Power	0x09[0]	0x11[0]	0x16[0]	0x1F[7:0]	No	High	Low
High Temperature Warning	0x09[7]	0x11[7]	0x16[7]	0x1B[2:0]	No	High	Low
Critical Temperature	0x08[6]	--	--	0x2E[2:0]	Yes	Low	Low
PEC Error	0x0A[3]	0x12[3]	0x17[3]	N/A	No	High	Low
Parity Error	0x0A[2]	0x12[2]	0x17[2]	N/A	No	High	Low

The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or PWR_GOOD signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or PWR_GOOD signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. Table 8 and Table 9 shows the PMIC's response of GSI_n signal and PWR_GOOD output signal for each event before and after host issues the Clear command. Table 8 and Table 9 assume that all mask bits are either '0' or '1' for simplicity.

Table 8. RTQ5162 Response for Clear Command by Host (Part I)

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			0x2F[1:0] = "00" or "01" or "10"		0x2F[1:0] = "00"		0x2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_BULK Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
1.8V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0V LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
VIN_BULK Input Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			0x2F[1:0] = "00" or "01" or "10"		0x2F[1:0] = "00"		0x2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Table 9. RTQ5162 Response for Clear Command by Host (Part II)

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	0x2F[1:0] = "01"		0x2F[1:0] = "01"		0x2F[1:0] = "10"		0x2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_BULK Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	High	Low	High	High	High	High	High	High
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
1.8V LDO Power Good	High	Low	High	High	High	High	High	High
1.0V LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
VIN_BULK Input Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	0x2F[1:0] = "01"		0x2F[1:0] = "01"		0x2F[1:0] = "10"		0x2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when host masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of PWR_GOOD output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of PWR_GOOD output signal.

The RTQ5162 assumes that there is no fuse protection on VIN_Bulk input rail on the DDR5 DIMM module to prevent short circuit type event.

15.12 Input Overvoltage Protection

An input overvoltage protection mechanism is implemented to limit the voltages to the PMIC. The PMIC actively monitors the input voltage VIN_Bulk rail.

There is one possibility where PMIC recognizes the input over voltage event.

1. VIN_Bulk input goes above the threshold set in Register 0x1B[7].

When this event occurs for a period longer than tInput_OV_GSI_Assertion time then PMIC sets the Register 0x08[0] accordingly and drives GSI_n output signal as shown in Table 7 at the same time. Note that at this point, the PMIC does not assert PWR_GOOD output signal. The PMIC allows access to all registers and PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may clear the VIN_Bulk input over voltage status register by writing '1' to Register 0x10 [0] appropriately or by writing '1' to global status clear Register 0x14[0]. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status Register 0x08[0] will remain at '1'.

In programmable mode (i.e., Register 0x2F [2] = 1), if VIN_Bulk input supply over voltage condition persists greater than tInput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts PWR_GOOD signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the VIN_Bulk input over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear Register 0x14[0] which triggers the GSI_n signal to be de-asserted. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status Register 0x08[0] will remain at

‘1’. Once the status register is cleared and GSI_n output signal is deasserted, the host may re-enable the PMIC’s output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal and input over voltage condition is no longer present.

In secure mode (i.e., Register 0x2F [2] = 0), if VIN_Bulk input supply over voltage condition persists greater than tInput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts PWR_GOOD signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

15.13 Output Power-Good Status

The RTQ5162 provides the voltage tolerance information to host that its output regulator may have crossed the desired dc+ac voltage tolerance from its nominal programmed setting. The nominal programmed setting for output regulator SWA, SWB and SWC is programmed in Register 0x21[7:1], Register 0x25[7:1] and Register 0x27[7:1] respectively. The PMIC offers the PWR_GOOD condition to be set independently for low side and high side.

In addition, PMIC has two LDO regulators: VOUT_1.8V and VOUT_1.0V.

There are four possibilities where PMIC recognizes the output power good event for any output regulator.

1. Output voltage goes below the threshold set in Register 0x21[0] for SWA or Register 0x25[0] for SWB or Register 0x27[0] for SWC.
2. Output voltage goes above the threshold set in Register 0x22[7:6] for SWA or Register 0x26[7:6] for SWB or Register 0x28[7:6] for SWC.
3. LDO output VOUT_1.8V goes below the threshold set in Register 0x1A [2].
4. LDO output VOUT_1.0V goes below the threshold set in Register 0x1A [0].

When either event occurs for a period longer than tOutput_PWR_GOOD_GSI_Assertion time then PMIC sets the Register 0x08[5,3:2] or Register 0x09[5] or Register 0x33[2] appropriately and drives PWR_GOOD and GSI_n output signal as shown in Table 7 at the same time. The PMIC may continue to operate but DDR5 DIMM functionality may not be guaranteed. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine and identify the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host may clear the appropriate status register individually or by writing ‘1’ to global status clear register “Register 0x14 [0]” which triggers the GSI_n signal to be de-asserted and PWR_GOOD signal to be asserted. If the output power not good condition is still present then PMIC will continue to assert GSI_n output signal and assert PWR_GOOD signal and the appropriate status Register 0x08[5,3:2] or Register 0x09[5] or Register 0x33 [2] will remain at ‘1’. If the output power not good condition persists, the host may set the appropriate mask register to remove GSI_n or PWR_GOOD output signal as shown in Table 8 and Table 9.

15.14 Output Overvoltage Protection

An output overvoltage protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulators. There are three possibilities where PMIC recognizes the over voltage event.

1. SWA output regulator goes above the threshold set in Register 0x22[5:4].
2. SWB output regulator goes above the threshold set in Register 0x26[5:4].
3. SWC output regulator goes above the threshold set in Register 0x28[5:4].

In programmable mode (i.e., Register 0x2F [2] = 1), if any output over voltage condition persists greater than tOutput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0A[7,5:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the appropriate output over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear Register 0x14[0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is deasserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal. In secure mode (i.e., Register 0x2F[2] = 0), if any output over voltage condition persists greater than tOutput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0A[7,5:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

15.15 Output Undervoltage and VIN_BULK Undervoltage-Lockout Protection

An output undervoltage-lockout protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulators.

There are four possibilities where PMIC recognizes the under voltage lockout event.

1. SWA output regulator goes below the threshold set in Register 0x22[3:2].
2. SWB output regulator goes below the threshold set in Register 0x26[3:2].
3. SWC output regulator goes below the threshold set in Register 0x28[3:2].
4. VIN_Bulk input voltage goes below vendor specific voltage.

In programmable mode (i.e.,Register 0x2F [2] = 1), if any output under voltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0B[3,1:0], Register 0x33[3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the appropriate output under voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear Register 0x14[0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command assuming valid VIN_Bulk input voltage. The PMIC enables

output switching regulators and floats PWR_GOOD signal High when all of its output regulators are normal.

In secure mode (i.e., Register 0x2F [2] = 0), if any output undervoltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0B[3,2:0], Register 0x33[3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

15.16 Output Currnet Limiter Warning Event

The RTQ5162 has output current limiter mechanism to limit the current on the PMIC output voltage regulators. The inductor current is actively monitored through the low-side MOSFET during conduction. The voltage drop across the phase node to PGND is compared with the current-limit threshold, which is set in Register 0x20, and the valley point of the inductor current is limited cycle-by-cycle. When output voltage regulators operate in current limit mode, the PWM on-time one-shot should wait for the inductor current discharging below the current-limit threshold to trigger the next on-time output, even if the output voltage has fallen below the reference feedback voltage. Hence, the output voltage starts dropping under current limit conditions due to insufficient energy to supply the output load. The output undervoltage event will occur if the output voltage falls below the undervoltage threshold, as described in 15.15. The protection mechanism of the output current limit is shown in Figure 12. There are three possibilities where PMIC recognizes the current limiter event.

1. SWA output regulator current goes above the threshold set in Register 0x20[7:6].
2. SWB output regulator current goes above the threshold set in Register 0x20[3:2].
3. SWC output regulator current goes above the threshold set in Register 0x20[1:0].

When either event occurs for a period longer than tOutput_Current_Limiter time then PMIC sets the Register 0x0B[7,5:4] appropriately, drives GSI_n output signal as shown in Table 7 at the same time. The PMIC continues to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion.

Once host determine the cause, the host may clear the appropriate output current limiter status register as well as any other status registers individually or by writing ‘1’ to global status clear register in Register 0x14[0] which triggers the GSI_n signal to be de-asserted. If the output current limiter condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in Register 0x0B[7,5:4] will remain at ‘1’. If the output current limiter condition persists, the host may set the appropriate mask register to remove the GSI_n output signal as shown in Table 8 and Table 9.

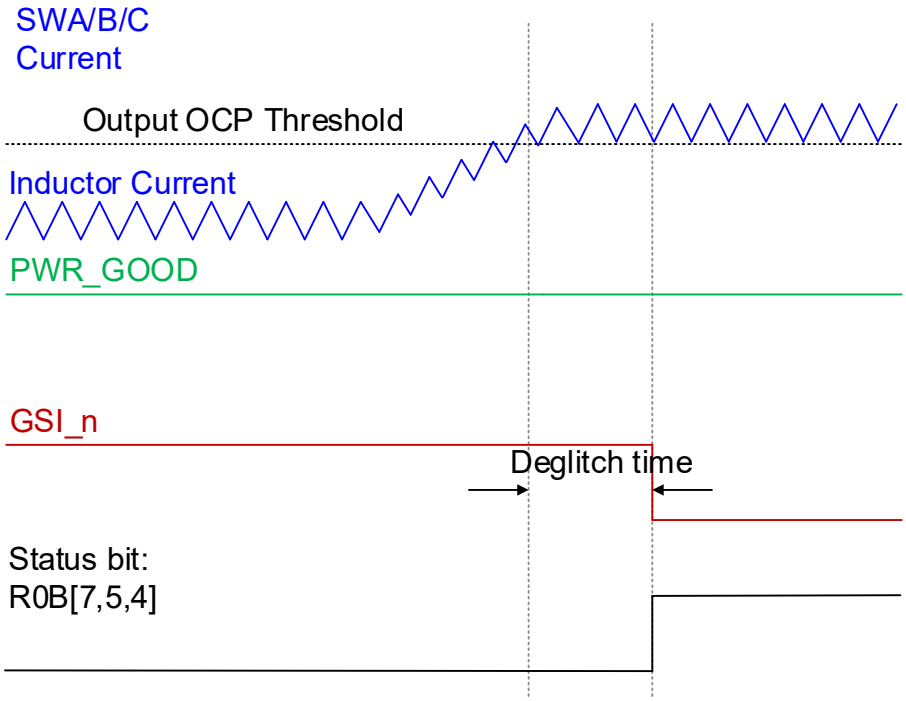


Figure 12. Output Current Limiter Protection

15.17 Output High Current Consumption Warning Event

The RTQ5162 supports high output current consumption warning mechanism for each of its regulator output. If enabled, the PMIC actively monitors the average output current of the regulator.There are three possibilities where PMIC recognizes the high output current consumption.

1. SWA output regulator average current goes above the threshold set in Register 0x1C[7:0].
2. SWB output regulator average current goes above the threshold set in Register 0x1E[7:0].
3. SWC output regulator average current goes above the threshold set in Register 0x1F[7:0].

When either event occurs then PMIC sets the Register 0x09[3,1:0] appropriately, drives GSI_n output signal as shown in Table 7 at the same time. The PMIC continues to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the appropriate output current consumption warning status register as well as any other status registers individually or by writing '1' to global status clear register in Register 0x14[0] which triggers the GSI_n signal to be de-asserted. If the output current consumption warning condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in Register 0x09[3,1:0] will remain at '1'. If the output current consumption warning condition persists, the host may set the appropriate mask register to remove GSI_n output signal as shown in Table 8 and Table 9.

15.18 PMIC High Temperature Warning and Critical Temperature Protection

The RTQ5162 provides a high temperature warning mechanism as well as critical temperature shutdown. There are two registers associated with PMIC temperature: The high temperature warning threshold Registe 0x1B[2:0] and shutdown temperature threshold Register 0x2E[2:0]. The value programmed in the shutdown temperature register must be equal or greater than value programmed in a warning threshold register.

There is one possibility where PMIC recognizes the high temperature event.

1. The PMIC temperature goes above the threshold set in Register 0x1B[2:0].

When the above event occurs for a period longer than tHigh_Temp_Warning time, the PMIC sets the Register 0x09[7] and drives GSI_n output signal as shown in Table 7 at the same time. The PMIC continues to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the temperature warning status register as well as any other status registers individually or by writing '1' to global status clear register in Register 0x14[0] which triggers the GSI_n signal to be de-asserted. If the high temperature warning condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in Register 0x09[7] will remain at '1'. If the high temperature warning condition persists, the host may set the appropriate mask register to remove GSI_n output signal as shown in Table 8 and Table 9.

If the PMIC temperature goes above the threshold set in Register 0x2E[2:0] for a period longer than tShut_Down_Temp time, the PMIC internally generates VR Disable command and disables all of its switching output regulators, sets the code in Register 0x05 [2:0], updates Register 0x08[6], drives GSI_n and PWR_GOOD output signal as shown in Table 7 at the same time. The PMIC keeps its VOUT_1.8V LDO and VOUT_1.0V LDO output regulator active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host is expected to monitor the temperature status registers. When the temperature drops below the threshold, the host must re-start the PMIC by going through the power cycle of the VIN_Bulk input supply.

15.19 Packet Error Code (PEC) and Parity Error Event

In I3C mode, PEC function and parity function can be enabled. If enabled, when PMIC detects either PEC error or Parity Error, the PMIC sets the Register 0x0A[3:2] appropriately, drives GSI_n output signal as shown in Table 7 and it continues to operate as normal and allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in Register 0x14[0] which triggers the GSI_n signal to be de-asserted.

In I^2C mode, for supported CCC, the PMIC supports parity function. When PMIC detects parity error, the PMIC sets the Register 0x0A[2], drives GSI_n output signal as shown in Table 7 and it continues to operate as normal and allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in Register 0x14 [0] which triggers the GSI_n signal to be deasserted.

15.20 Analog to Digital Converter (ADC)

The RTQ5162 supports an analog-to-digital converter (ADC) to monitor input supply voltages VIN as well as output voltage regulator voltages (SWA, SWB, SWC, VLDO_1.8V, and VLDO_1.0V). Register 0x30[7:3] allows to enable the ADC and select the desired input supply voltage or output supply voltage. Register 0x31[7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is as follows:

Table 10. ADC Accuracy Table

Input Rail	ADC Range	ADC Accuracy
SWA, SWB Output Voltage	1050mV to 1160mV	± 1 LSB
	Outside of 1050mV to 1160mV	± 3 LSB
SWC Output Voltage	1750mV to 1850mV	± 1 LSB
	Outside of 1750 mV to 1850mV	± 3 LSB
VLDO_1.8V, VLDO_1.0V Output Voltage	--	± 3 LSB
VIN_BULK Input Voltage	--	± 6 LSB

The RTQ5162 also monitors output voltage regulator current or power (SWA, SWB, and SWC) and updates Register 0x0C[7:0] for SWA, Register 0x0E[7:0] for SWB, and Register 0x0F[7:0] for SWC. Register 0x1B[6] allows the host to select whether the RTQ5162 should report current measurements or power measurements. The current or power measurement reported in this registers are an average measurement over time period defined in Register 0x30[1:0]. If Register 0x1B[6] = 1, Register 0x1A[1] allows host to select whether the RTQ5162 should report individual rail power or total power in Register 0x0C[7:0]. The register update frequency of this register is configured in Register 0x30[1:0]. Register 0x32[1:0] allows the user to change the LSB step size for current or power measurements.

Table 11. RTQ5162 ADC Current and Power Accuracy; R32[1:0] = 00

Load Current	SWA to SWC Rails Current Accuracy	SWA to SWC Rails Corresponding Power Accuracy	Total Power Accuracy
Less than 0.5A	± 4 LSB	± 7 LSB	± 12 LSB
Greater than or equal to 0.5A	± 3 LSB	± 6 LSB	

Table 12. RTQ5162 ADC Current and Power Accuracy; R32[1:0] = 01

Load Current	SWA to SWC Rails Current Accuracy	SWA to SWC Rails Corresponding Power Accuracy	Total Power Accuracy
Less than 0.5A	± 9 LSB	± 18 LSB	N/A (R32[1:0] must be set 00 when R1A[1]=1)
Greater than or equal to 0.5A	± 8 LSB	± 16 LSB	

15.21 RTQ5162 Address ID (PID)

The RTQ5162 has PID input pin which allows to assign up to three different unique ID for I^2C and I3C Basic protocol. At first power on, when VIN_Bulk input is applied, the PMIC automatically determines its ID. The PMIC offers three different ID as shown in Table 13.

Table 13. PMIC ID

PID Pin Connection on DIMM Board	PMIC ID	Comment
Short to GND	PID = 1001	PMIC can be configured
Floating	PID = 1000	
Short to 1.8V	PID = 1100	Connected to RTQ5162's VLDO_1.8V

15.22 Error Injection

The RTQ5162 offers error injection function for the purpose of debug, test, and validation at various stages.

15.22.1 Error Injection Function Usage prior to VR Enable (Either via VR_EN Pin or I²C/I3C Bus)

Prior to VR Enable command, the Error injection function may be invoked by setting error injection enable bit Register 0x35[7] = 1 during the configuration state. If any of either VIN_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected prior to VR Enable command, the PMIC shall not execute power on sequence and shall not enable PMIC output regulators when PMIC receives VR Enable command. The PMIC shall not update error log registers (Register 0x04 to Register 0x06). The PMIC shall update appropriate status registers (Register 0x08 to Register 0x0B, Register 0x33) accordingly. The PMIC shall enter in secure mode if Register 0x2F[2] = 0 and programmable mode if Register 0x2F[2] = 1.

15.22.2 Error Injection Function Usage after VR Enable (either via VR_EN Pin or I²C/I3C Bus)

After RTQ5162 output regulators are enabled with VR Enable command and PMIC is in programmable mode, the error injection function may be invoked by setting error injection enable bit Register 0x35[7] = 1. If any of either VIN_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected the PMIC shall execute Power Off Sequence to disable PMIC output regulators and shall update the error log registers (Register 0x04 to Register 0x06) as well as status registers (Register 0x08 to Register 0x0B, Register 0x33) accordingly. Note that if any of the output rails are not enabled through power on sequence configuration registers, the error injection on that output rail does not apply. After PMIC output regulators are enabled with VR Enable command and PMIC is in secure mode, the error injection enabling Register 0x35 [7] = 1 is disallowed. The PMIC shall ignore any attempts to inject any error and shall not execute Power Off Sequence to disable PMIC output regulators and shall not update any error log or status registers. To exit the error injection function, the host shall power cycle VIN_Bulk input supply.

15.23 Acoustic Noise

The RTQ5162 buck regulators normally operates in DCM (Discontinuous Current Mode). The buck regulator's switching frequency is a function of a current load on its output regulator. At light load (typically < 50mA), the buck regulator's switching frequency may approach to less than 100 KHz. The human ear audible frequency range is 20 Hz to 20 KHz. If buck regulator switching frequency falls within the human ear audible frequency range, then human ear can experience the acoustic noise. To prevent the acoustic noise to human ear, the RTQ5162 offers a feature which prevents the buck regulator switching frequency to go below the threshold frequency that is configured in register R36[3:1]. When the feature is enabled, the PMIC ensures that its switching frequency stays above the threshold frequency regardless of how low the output load current may be. The acoustic noise prevention control feature is in Register 0x36[3:1]. The control register applies to all three buck regulators. This feature is not applicable to any buck regulator that is configured to operate as Forced CCM (Continuous Current Mode). If PMIC is configured such that one or more buck regulators is configured as DCM and other buck regulator

is configured as Forced CCM, when this feature is enabled, it applies to any buck regulators that are configured as DCM. At light load, when this feature is enabled, there may be a slight difference in efficiency. However, the difference in efficiency may be insignificant and may be within the measurement noise.

15.24 Output Regulator Control Topology

The RTQ5162 applies A^{2}RCOT (Accurate Adaptive Ramp COT) to regulate the output voltage of VDD, VDDQ, and VPP. The SWA and SWB can operate in either single phase mode or dual-phase mode. When operating as dual-phase mode, the interleaving PWM control is applied to balance the output current.

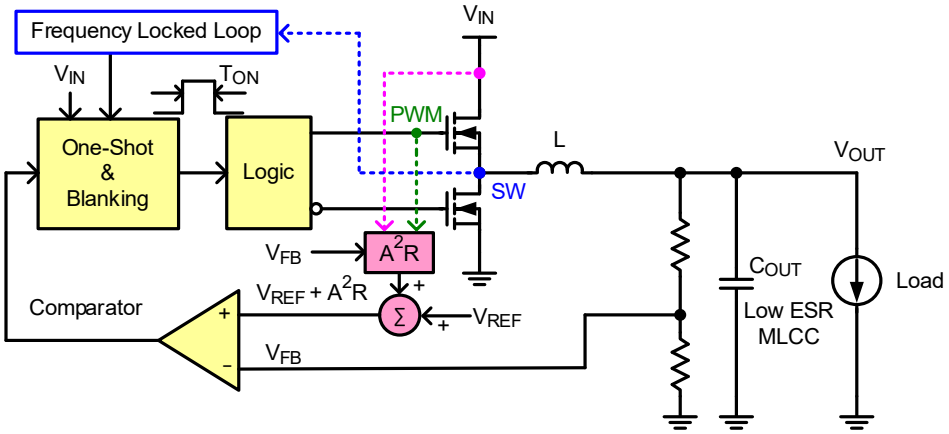


Figure 13. A^{2}RCOT Control Mechanism

Figure 13 illustrates a standard A^{2}RCOT control buck converter. To achieve good stability with low-ESR ceramic capacitors, A^{2}RCOT generates an internal ramp by sensing V_{IN}, V_{FB}, and PWM signal. The internal ramp is in phase with the PWM signal, and its magnitude is proportional to V_{IN}. Moreover, the average of V_{FB} can be well regulated at V_{REF}, which makes good output load and line regulation. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

However, making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for the following reasons. The voltage drops across the MOSFET and inductor make the equivalent conversion ratio smaller than the ideal duty ratio. That is, the switching frequency is not fixed under different output load conditions. The frequency is increasing at higher loading and junction temperature as compared to smaller loading and junction temperature.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. The A^{2}RCOT uses the frequency-locked loop, measuring the actual switching frequency and modifying the on-time with a feedback loop to make the average switching frequency in the desired range.

The RTQ5162 control algorithm is simple to understand, as depicted in Figure 14. The feedback voltage is compared to the reference voltage, VREF, with the accurate adaptive ramp (A2R) added. When the feedback signal is less than the combined reference, the on-time one-shot is triggered as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

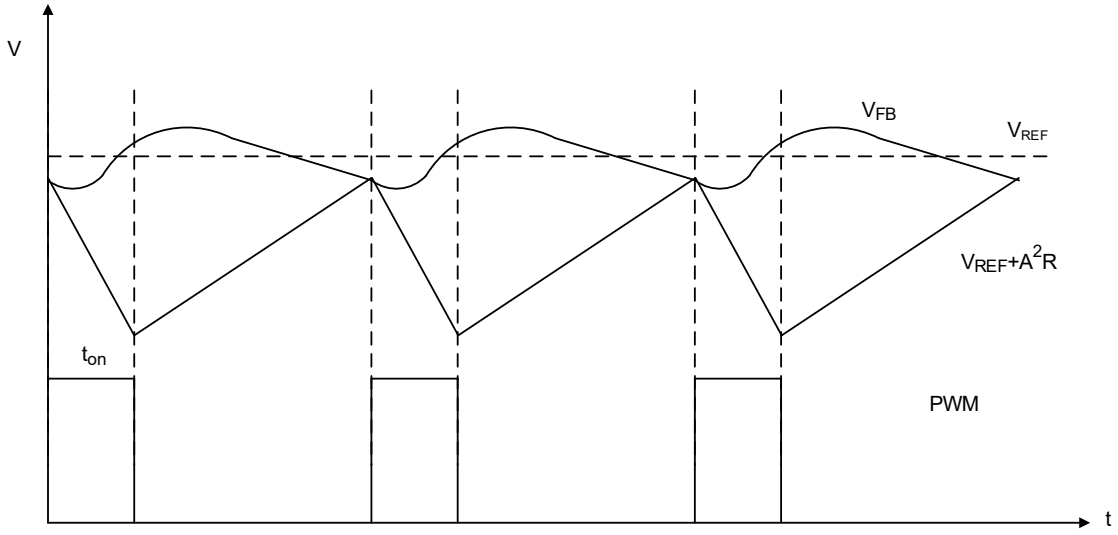


Figure 14. A²RCOT PWM Control Mechanism

15.25 Regulator Operating Mode Selection

The RTQ5162 offers two kinds of PWM operations under the light load: DEM (Diode Emulation Mode) and FCCM (Forced Continuous Conduction Mode). The user can switch between DEM and FCCM by the Register 0x29[7:6], Register 0x2A[7:6], and Register 0x2A[3:2] in programmable mode or in the configuration state of FSM before issuing the VR_EN command.

15.26 DEM (Diode Emulation Mode)

In diode emulation mode, the RTQ5162 automatically reduces the switching frequency under light load conditions to maintain high efficiency. The reduction of frequency is achieved smoothly. As the output current decreases from heavy load conditions, the inductor current also decreases and eventually reaches to the point where its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free-wheeling current becomes negative. As the load current is further decreased, it takes longer to discharge the output capacitor to the level that requires the next “ON” cycle. Contrarily, when the output current increases from light load to heavy load, the switching frequency increases to the pre-set value as the inductor current reaches the continuous conduction. The transition load point between DEM and CCM operation is shown in Figure 15 and can be calculated as follows:

$$I_{LOAD\_BCM} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

, where t_{ON} is the on-time of the high-side MOSFET.

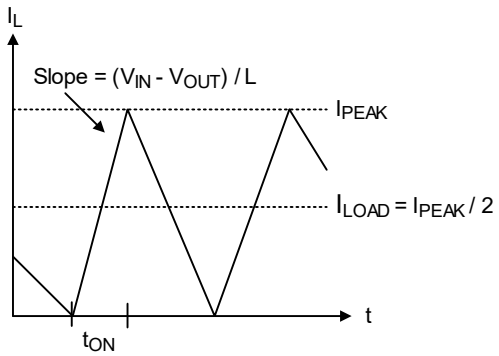


Figure 15. Boundary Condition of DEM/CCM

The switching frequency in DEM can be calculated as follows:

$$f_{SW}(I_{LOAD}) = \frac{2LI_{LOAD}}{V_{IN}t_{ON}^2\left(\frac{V_{IN}}{V_{OUT}}-1\right)}$$

, where I_{LOAD} is smaller than I_{LOAD_BCM}.

As shown in the equation, the switching frequency is a function of the output load current, I_{LOAD}, and it is proportional to I_{LOAD}, which means it becomes higher at heavy load and reduces to almost zero at a very light load. Besides, the inductor selection can also change the switching frequency in DEM. Choosing a large inductance makes more switching loss compared to a small inductance. However, the core loss of the inductor increases with larger inductor current ripple for a given inductor. That is, proper selection of the inductor based on efficiency target is important.

Moreover, to achieve a smooth transition from DEM to CCM or backward, during discontinuous switching, the on-time is immediately increased to add “hysteresis” to discourage the IC from switching back to continuous switching unless the load increases substantially. The RTQ5162 returns to continuous conduction as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for the presetting switching frequency and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

15.27 FCCM (Forced Continuous Conduction Mode)

Unlike diode emulation mode (DEM) that enables zero current detection (ZDC) to reject negative inductor current when the low-side MOSFET turns on, the inductor current can be negative until the next on-time is generated in FCCM. The switching frequency is fixed from no load to full load. Therefore, the results in benefits like better transient response from light load to heavy load and smaller EMI/EMC come along with FCCM. Nevertheless, the poor efficiency at light loads is a trade-off.

16 Application Information

(Note 7)

16.1 Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response; however, they increase the inductor ripple current and output voltage ripple, and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required. Also, transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad \text{and} \quad I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output undervoltage shutdown feature makes this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses, some types of shielded ferrite core are usually better. Although they are possibly larger or more expensive, they will probably give fewer EMI and other noise problems.

Since DDR5 on DIMM has layout space limitation to power management IC on DIMM as well as the surrounding components like inductors and input/output capacitors, a standard inductor mechanical specification is defined in Table 14, Table 15, and Table 16. Moreover, the electrical specification of inductor is also defined in Table 17 and Table 18. The electrical specifications include inductance, maximum DCR, maximum ACR and the minimum inductance requirement after de-rating at a specified operating current. The DIMM vendors can select an inductor based on the Table 17 and Table 18. Because the inductor size is fixed, the tradeoff between efficiency and transient response is the main concern on selection. Generally, for SWA and SWB, which are 1.1V output rails, it is recommended to choose and inductance of 0.47μH. On the other hand, for the output rail with V_{OUT} = 1.8V, which is either the SWC or VPP rail, an inductance of 1μH is suggested.

Table 14. Inductor Mechanical Specifications for SWA and SWB

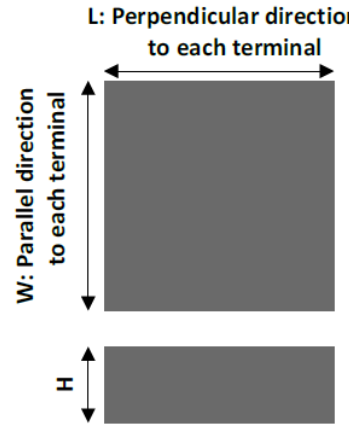
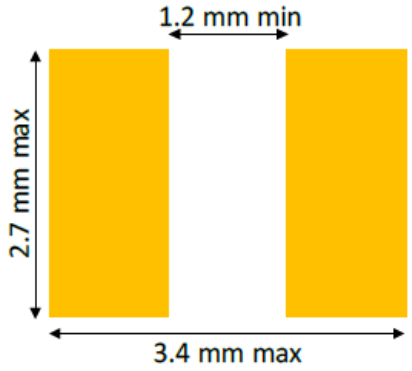
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	3.4 max		
W [mm]	2.7 max		
H [mm]	1.2 max		

Table 15. Selectable Optional Mechanical Specifications for SWA and SWB by the Implemented Acceptable DIMM (in UDIMM and SODIMM) Design

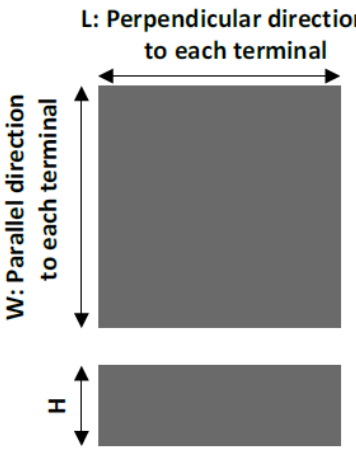
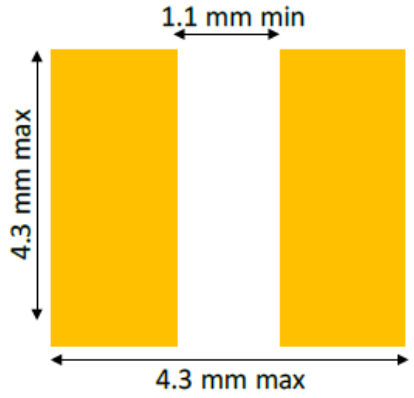
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	4.3 max		
W [mm]	4.3 max		
H [mm]	1.2 max		

Table 16. Inductor Mechanical Specifications for SWC

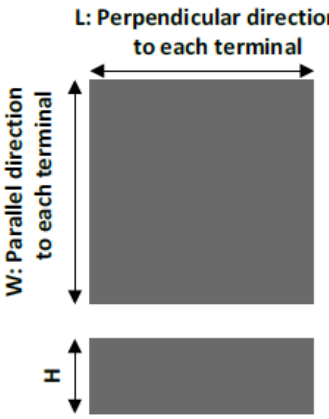
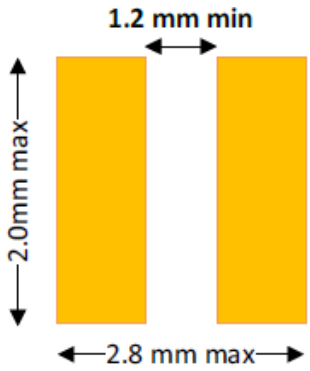
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	2.7 max		
W [mm]	2.2 max		
H [mm]	1.2 max		

Table 17. Inductor Electrical Specifications for SWA and SWB (1.1V)

Package Height	L @ 0.5-1MHz/0bias ± 20% [µH]	Max DCR [mΩ]	Max ACR @ 1MHz [mΩ]	Min. L @ 8.5A [µH]
1.2 Max [mm]	0.47	11	93	0.2

Table 18. Inductor Electrical Specifications for SWC (1.8V)

Package Height	L @ 0.5-1MHz/0bias ± 20% [µH]	Max DCR [mΩ]	Max ACR @ 1MHz [mΩ]	Min. L @ 3A [µH]
1.2 Max [mm]	1	36	182	0.5

16.2 Output Capacitor Selection

The buck output regulators of the RTQ5162 are optimized for ceramic output capacitors, and the best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR, ESL and stored charge. These three ripple components are called ESR ripple, ESL ripple, and capacitive ripple. Since ceramic capacitors have extremely low ESR, ESL and relatively little capacitance, all these components should be considered if ripple is critical. The decomposition of the output ripple is shown in Figure 16. The formulas to describe each component are listed below:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(ESL)} = \frac{d}{dt} I_L \times ESL$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

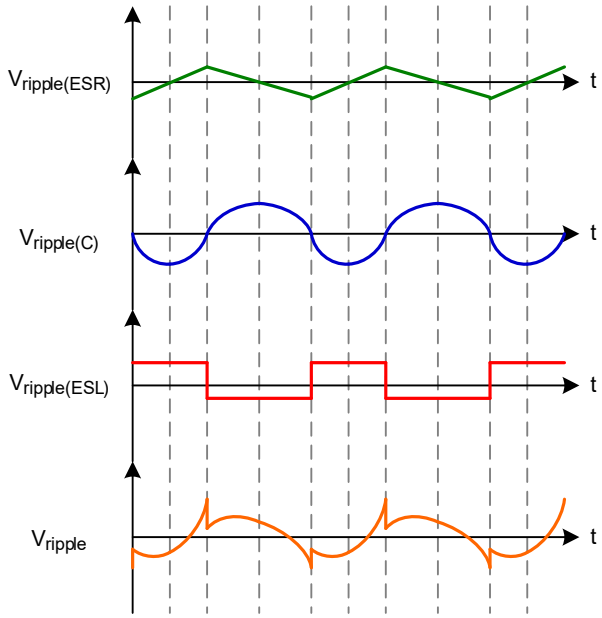


Figure 16. Output Ripple Decomposition

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The A^2RCOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the A^2RCOT control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. The behavior diagram of output voltage drop is depicted as Figure 17. Calculate the approximate on-time (neglecting parasitic) and maximum duty cycle for a given input and output voltage as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ ,and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but it can be neglected both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

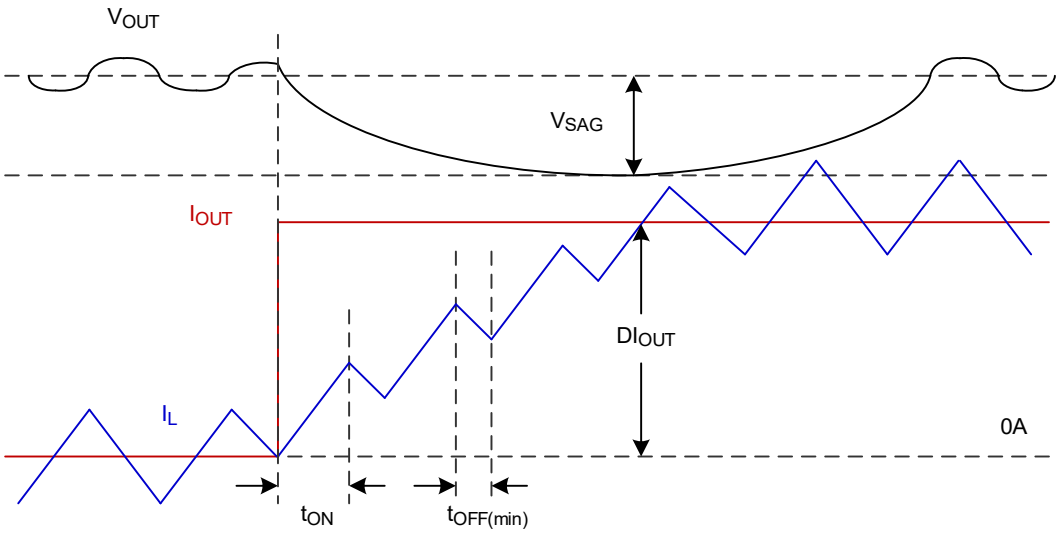


Figure 17. Output Voltage Drop (V_{SAG}) Estimation as Output Load Current Step Up

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

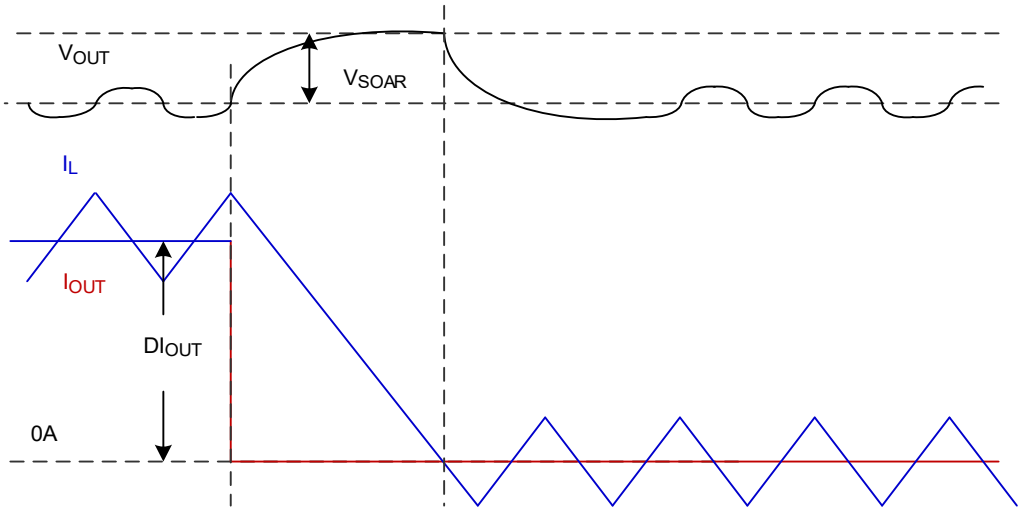


Figure 18. Output Voltage Soar (V_{SOAR}) Estimation as Output Load Current Step Down

Most applications never experience instantaneous full load steps and the RTQ5162's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that overvoltage protection and undervoltage protection will not be triggered.

In addition, the recommended dielectric type of the capacitor is X7R which has the best performance among temperature and DC and AC bias voltage variations. The variation of the capacitance value with temperature, DC

bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage. A standard output capacitors' electrical specification is defined in Table 19. The electrical specifications include capacitance, rated voltage and the size code in inch. The DIMM vendors should select the capacitors based on the Table 19.

Table 19. Output Capacitor Electrical Specifications

Component	Value	Physical Size
C_{OUTA}	47µF (x3)	6.3V; 0603
C_{OUTB}	47µF (x3)	6.3V; 0603
C_{OUTC}	47µF (x3)	6.3V; 0603
$C_{LDO\_1.8V}$	4.7µF	6.3V; 0402
$C_{LDO\_1.0V}$	4.7µF	6.3V; 0402

16.3 Input Capacitor Selection

A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance cause high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

The capacitor voltage rating should meet reliability and safety requirements. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current due to low ESR and ESL. Following equation is used to estimate the required effective capacitance that will meet the ripple requirement.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{\Delta V_{IN\_PP} \times f_{SW}}$$

where D is calculated as below:

$$D = \frac{V_O}{V_{IN} \times \eta}$$

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1-\frac{V_{OUT}}{V_{IN}}) \times {I_{OUT}}^2 + \frac{\Delta {I_L}^2}{12} \right]}$$

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Besides, since the ESL of ceramic capacitors plays a significant role on voltage spikes at both the input and the phase node, it is desirable to add a small capacitor with low ESL near the VIN pin.

While the MLCC is excellent regarding allowable ripple current, it is well-known regarding effective capacitance that is necessary to meet transient response requirements. There can be two VIN spikes during the transient: the first spike is related to the ESR; and the second spike is caused by the difference between the buck-converter input current (i_{IN_B}) and the bus-converter output current (i_{PS}) as depicted in Figure 19. Both spikes should be lower than the VIN undershoot or overshoot requirement (VIN_tran). First, since the MLCCs have very small ESR, the component of ESR drop can almost be ignored. The second spike is related to the response of the bus converter. The converter output-current rise time during a transient event, T_{R_PS}, can be approximated by the following equation:

$$T_{R\_PS} \cong \frac{0.35}{f_{BW\_PS}}$$

, where f_{BW_PS} is the control loop bandwidth of the buck converter.

The equivalent capacitance of the input capacitors should be greater than that calculated with the following equation:

$$C_{IN} \geq \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times T_{R\_PS}}{V_{IN\_Tran}}$$

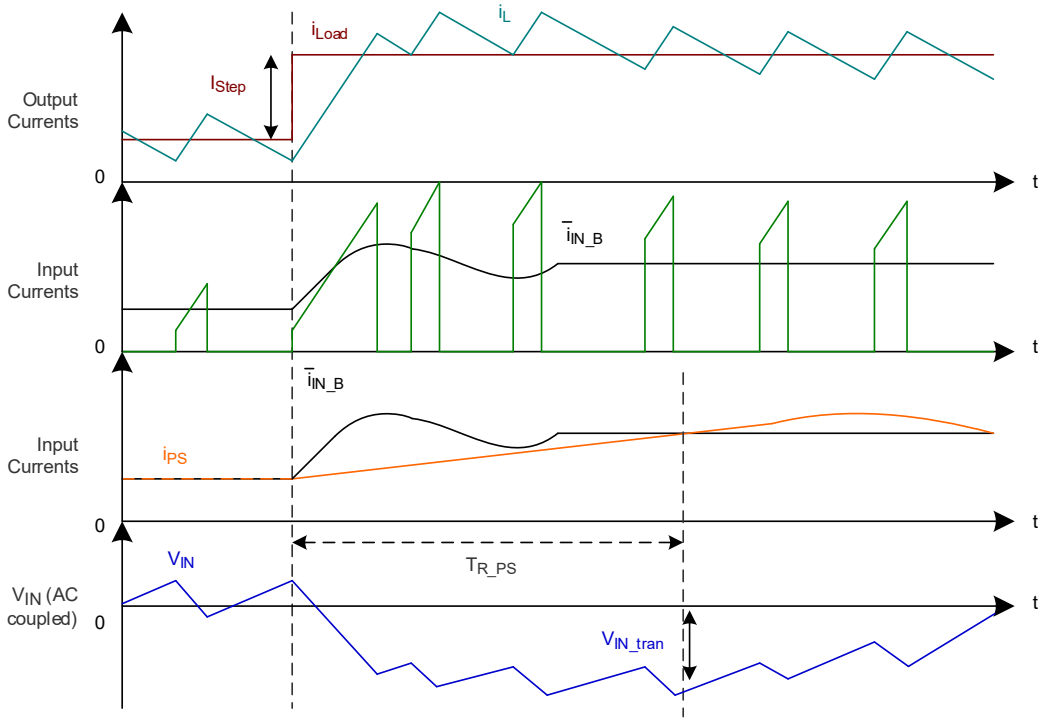


Figure 19. VIN Transient Current Diagram

Either the VIN ripple (ΔV_{IN_PP}) or the Vin transient ripple (V_{IN_Tran}) should meet the design requirements. For the RTQ5162, the input voltage should be always higher than the VIN_UVLO threshold to confirm the PMIC's functionality.

Moreover, it should be noticed that many de-rating factors, including V_{BIAS} dc voltage, ac voltage, and operating temperature, make equivalent capacitance smaller than the capacitance without bias. A standard input capacitors' electrical specification is defined in Table 20. The electrical specifications include capacitance, rated voltage, and the size code in inch. The DIMM vendors should select the input capacitors based on the Table 20.

Table 20. Input Capacitor Electrical Specifications

Component	Value	Physical Size
C_{IN}	4.7µF	10V; 0402
C_{INA}	22µF (x2)	10V; 0603
C_{INB}	22µF (x2)	10V; 0603
C_{INC}	22µF (x2)	10V; 0603
C_{BYP}	0.1µF	10V; 0201
C_{BYPA}	0.1µF	10V; 0201
C_{BYPB}	0.1µF	10V; 0201
C_{BYPC}	0.1µF	10V; 0201

16.4 Bootstrap Circuit

The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. When the SW node goes below the IC supply voltage V_{CC} (V_{DD}) or is pulled down to ground (the low-side MOSFET is turned on and the high-side MOSFET is turned off), the bootstrap capacitor, C_{BOOT}, charges through the bootstrap resistor, R_{BOOT}, and bootstrap diode, D_{BOOT}, from the VCC power supply, as shown in Figure 20. On the other hand, the voltage across V_{BOOT} and SW can supply gate charge to the high-side MOSFET when the low-side MOSFET is turned off and the SW node goes to a higher voltage, VOUT. In the meantime, the bootstrap diode reverses bias and blocks the rail voltage from the IC supply voltage, V_{CC}.

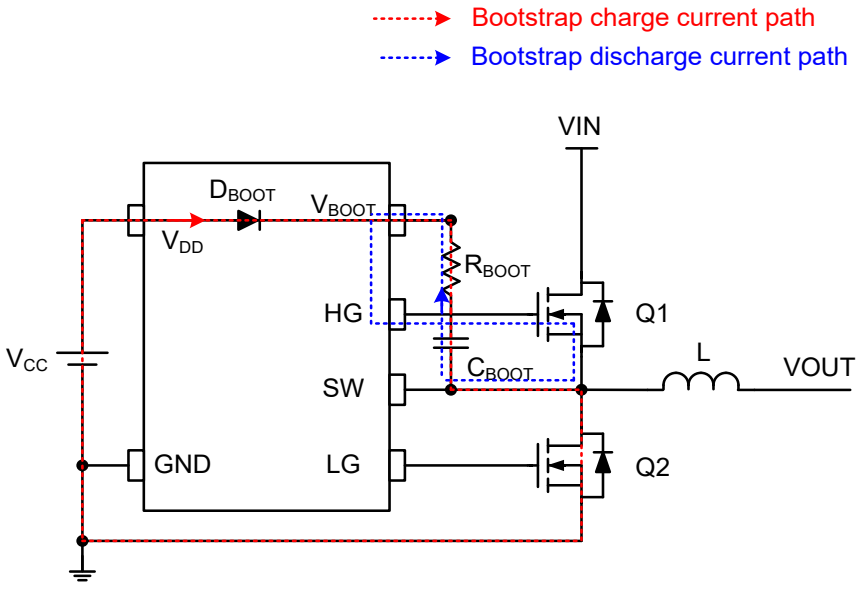


Figure 20. Bootstrap Power Supply Circuit

There are some design considerations for a bootstrap circuit. First, the selection of the bootstrap capacitor (C_{BOOT}) is based on the maximum voltage drop across C_{BOOT} to guarantee the high-side MOSFET has enough charge to turn on periodically. The maximum allowable voltage drop (ΔV_{BOOT}) depends on the minimum gate drive voltage (for the high-side MOSFET) to maintain. If V_{GSMIN} is the minimum gate-source voltage, the capacitor drop must be:

$$\Delta V_{BOOT} = V_{CC} - V_F - V_{GSMIN}$$

where V_{CC} is the supply voltage of the gate driver, and V_F is the forward voltage drop of the bootstrap diode.

Therefore, the value of bootstrap capacitor is calculated as:

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{BOOT}}$$

where Q_{Total} is the total amount of the charge required for driving the high-side MOSFET and some leakage charge in the chip.

Second, when the external bootstrap resistor is used, the resistance, R_{BOOT}, introduces an additional voltage drop:

$$V_{RBOOT} = \frac{Q_{Total}}{t_{Charge}} \times R_{BOOT}$$

where t_{Charge} is the bootstrap charging time (the low-side MOSFET turn-on time).

The power dissipation on R_{BOOT} should be considered when choosing the package size of resistor. When estimating the maximum allowable voltage drop, the value of voltage drop of bootstrap resistor should be taken into account.

For example, assume V_{CC} = 5V, V_F = 0.7V, R_{BOOT} = 1Ω, V_{GSMIN} = 2.5V and Q_{Total} = 5nC. The ΔV_{BOOT} can be calculated as 1.8V. The estimated C_{BOOT} is 2.8nF. Generally, the ΔVBOOT is not suggested to be too large and also need to consider the additional voltage drop on R_{BOOT}. Moreover, the de-rating factors, including V_{BIAS} dc voltage, ac voltage and operating temperature, make equivalent capacitance be smaller. The common selection value of C_{BOOT} is 100nF~220nF, which makes the ΔV_{BOOT} to be 50mV and 25mV, respectively. If choosing the bias capacitor with an 0201 package and 6.3V voltage rating, the de-rating factor is about 0.5. Therefore, ΔV_{BOOT} increases to 100mV and 50mV. In addition, the voltage drop on R_{BOOT} = 1Ω is 25mV as t_{Charge} is 200ns. Adding R_{BOOT} can reduce the EMI noise as well as voltage spikes on the phase node. However, the additional power loss will reduce the system efficiency.

16.5 VLDO_1.8V and VLDO_1.0V Decoupling Capacitor

The RTQ5162 integrates two LDO regulators (VLDO_1.8V and VLDO_1.0V). The VLDO_1.8V and VLDO_1.0V LDOs are supplied by VIN. They provide power to system devices, such as SPD, TS and RCD on the DIMM. Both VLDO_1.8V and VLDO_1.0V need a decoupling capacitor placed near the output pin and the equivalent minimum capacitance should be at least 2.2μF. In many applications, a 4.7μF/6.3V/X5R/0402 capacitor is recommended. When choosing the package size and the voltage rating of a capacitor, the de-rating coefficient versus voltage and temperature is important for taking account of equivalent capacitance under actual operating condition.

16.6 Thermal Consideration

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-28L 3x4 (FC) package, the thermal resistance, θ_{JA}, is 44.13°C/W on a twelve layers DIMM card size PCB. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (44.13°C/W) = 2.27W for a WQFN-28L 3x4 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 21 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

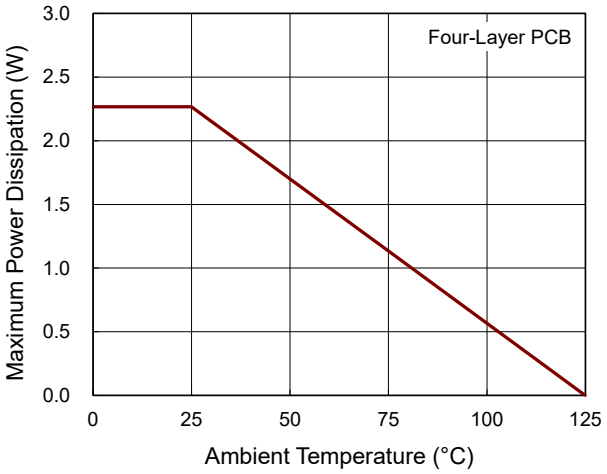


Figure 21. Derating Curve of Maximum Power Dissipation

16.7 Layout Consideration

Layout is crucial in high-frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to converter instability. The following points must be considered before starting a layout for the RTQ5162. Figure 22 and Figure 23 show the recommended layout guide for reference. In Figure 22, the top layer layout of the RTQ5162's EVB is demonstrated. Note that the components' sizes are considered and depicted in their actual relative sizes. In Figure 23, the bottom layer layout of the RTQ5162's EVB is demonstrated. Due to PMIC layout area limitations on the DIMM, the input capacitors and output capacitors are placed on this layer. Furthermore, the input caps have been divided into two parts: a small decoupling capacitor with a smaller package size and capacitance is mounted under one side of the VIN pin for each rail, and two bulk capacitors are placed directly beneath the VIN pin on the other side for each rail. The placement of the small decoupling capacitor helps filter out high-frequency voltage spikes, reducing phase ringing on the phase pin. The bulk capacitors provide prompt energy during output load transients. It is essential to keep noisy signals, such as the switching node and the vias of output capacitors, away from sensitive areas. Below are the key considerations for the RTQ5162's EVB layout:

- Make the traces for high current paths as short and wide as possible to minimize resistance and inductance.
- Place the input capacitors as close to the device pins (VINA, VINB, and VINC) as possible to improve filtering and reduce noise.

- The SW node experiences high-frequency voltage swings, so keep it confined to a small area. Also, keep sensitive components away from the SW node to prevent noise coupling.
- Connect the PGND pin to a robust ground plane for effective heat sinking and noise suppression. For enhanced thermal dissipation, it is advisable to add thermal vias near the PGND pin to link different layers.
- It is recommended to connect the ground of VIN to AGND and then to the PGND layer through a single via to maintain signal integrity.
- Position decoupling capacitors as close to the device pins (VIN and AGND) as possible for optimal noise suppression.
- Differential route the feedback traces for each rail and ensure they are distanced from noisy signals on the EVB to avoid interference.
- The NC pins at the three corners are recommended to connect to PGND for better heat dissipation.

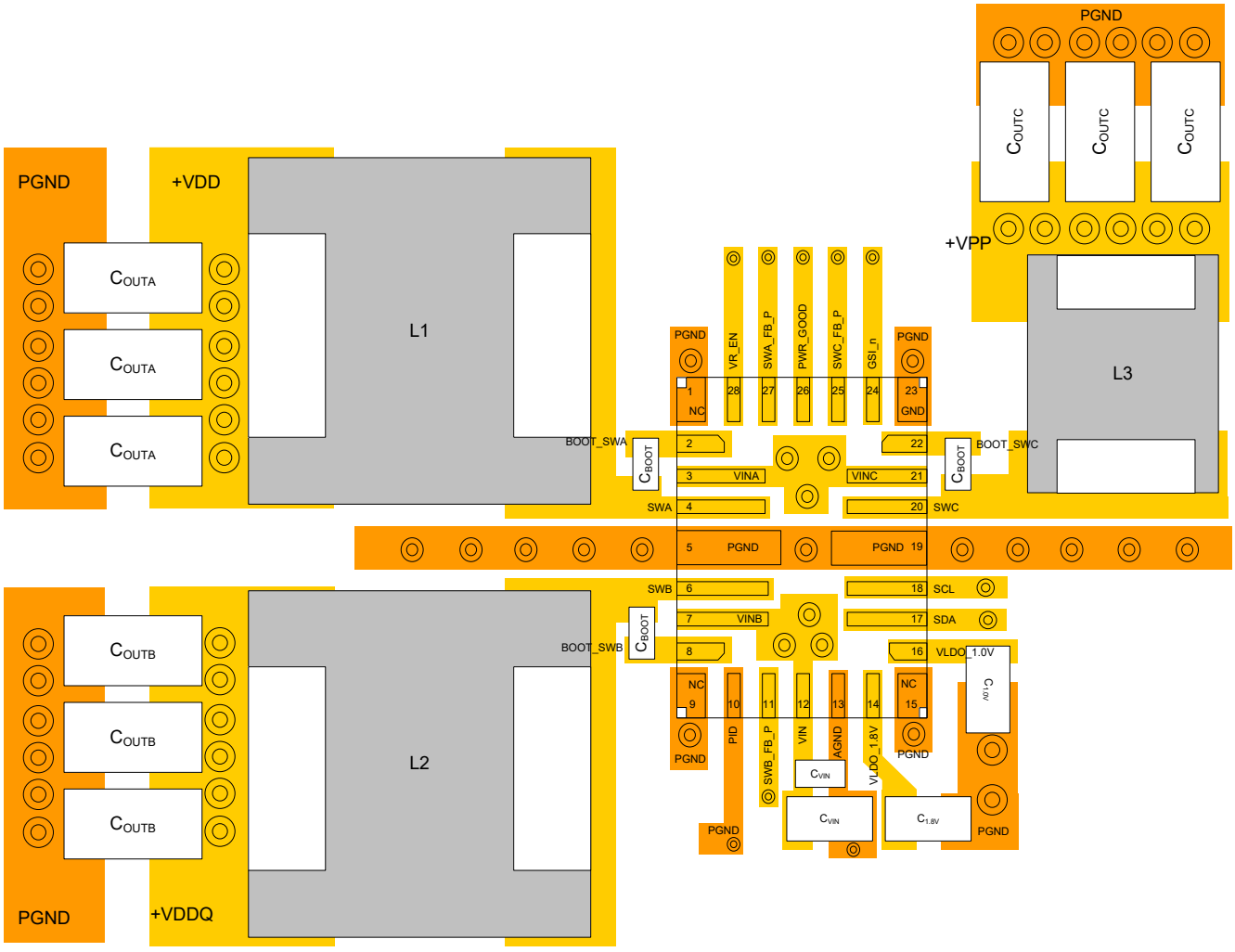


Figure 22. Layout Guide (Top Layer)

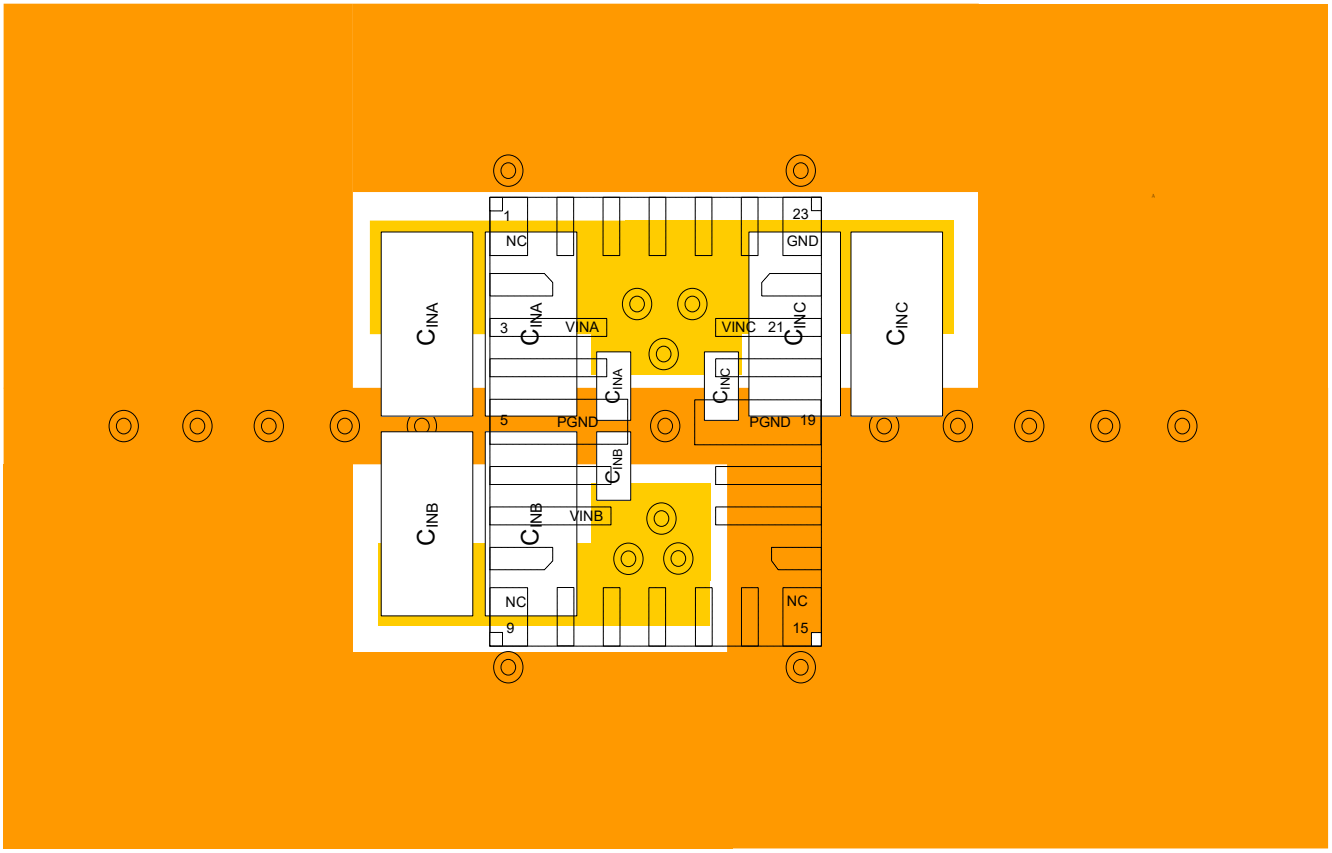


Figure 23. Layout Guide (Bottom Layer)

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Functional Register Description

17.1 Register Attribute Definition

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Write has no effect.
Read/Write	RW	This bit can be read or written by host.
Write Only	WO	This bit can only be written by host. Read from this bit returns ‘0’.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return ‘0’ when read. Write has no effect.
Write ‘1’ Only	1O	This bit can only be set (i.e. write ‘1’) but not reset (i.e. write ‘0’). Write ‘0’ has no effect.
Persistent	E	This bit is persistent during power cycle.
Protected	P	This bit is protected by the password registers. This bit cannot be read to or written unless the password code has been written into the password registers.

17.2 Register Map Breakdown

Region	Register Range	Restriction
Host User (NVM and VM)	R00 – R14, R30 - R31, R33 - R34, R36 – R3F	All non-protect bits are writable in both WP or WE mode.
	R15 - R2F, R32, R35	Restricted access in WP mode
DIMM Vendor (NVM)	R40 - R6F	Restricted access in WP mode
PMIC Vendor (NVM)	R70 - RFF	Restricted access in WP mode

17.3 Register Memory Protection

The PMIC DIMM vendors registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to DIMM vendor registers are blocked unless it is unlocked by providing the correct password. The default password for DIMM vendor registers is (Register_0x37 = 0x73) and (Register_0x38 = 0x94). The PMIC offers DIMM vendors to select their own password for DIMM vendor registers.

17.3.1 Steps to Access DIMM Vendor Region Registers

The steps to access the DIMM vendor registers are as follows:

1. Write to “Register 0x37” = 8 bit password LSB code.
2. Write to “Register 0x38” = 8 bit password MSB code.
3. Write to “Register 0x39” = 0x40.
4. Perform Read operations to DIMM vendor registers as desired.
5. Write to “Register 0x39” = 0x00 (Lock).

17.3.2 Steps to Change DIMM Vendor Region Password

By default, the DIMM vendor region register password is 0x9473. The steps to change the password from default password are as follows:

1. Write to “Register 0x37” = 0x73. (default)
2. Write to “Register 0x38” = 0x94. (default)
3. Write to “Register 0x39” = 0x40.
4. Write to “Register 0x37” = New 8 bit password LSB code as desired by DIMM vendor.
5. Write to “Register 0x38” = New 8 bit password MSB code as desired by DIMM vendor.

6. Write to “Register 0x39” = 0x80.
7. Wait 200ms.
8. Write to “Register 0x39” = 0x00 (Lock).
9. Power cycle the PMIC. Remove VIN_BULK and VIN_MGMT supply from the PMIC. The new password is in effect after the power cycle.

To change the password again from this point on, repeat steps 1 to 8 but note that in steps 1 and 2 current password is required.

17.3.3 Steps to Burn or Program DIMM Vendor Region Registers

The steps to burn or to program the DIMM vendor registers are as follows:

1. Write to “Register 0x37” = 8 bit password LSB code.
2. Write to “Register 0x38” = 8 bit password MSB code.
3. Write to “Register 0x39” = 0x40.
4. Programming DIMM vendor registers are done at block level.

   Block 40 addresses: 0x40 - 0x4F;

   Block 50 addresses: 0x50 - 0x5F;

   Block 60 addresses: 0x60 - 0x6F.

   Perform write operation to each block as desired.
5. Burn each block one at a time:

   Block 40 addresses: Write “Register 0x39” = 0x81.

   Block 50 addresses: Write “Register 0x39” = 0x82.

   Block 60 addresses: Write Register 0x39” = 0x85.
6. Wait time 200ms.
7. To check if programming is complete:

   Perform read from “Register 0x39”. The code 0x5A indicates it is complete. It takes 200ms per page to program.
8. To verify if programming is done correctly:

   Perform read operation from appropriate block addresses.
9. Write to “Register 0x39” = 0x00. (Lock)

17.4 Host and DIMM Region Register Map

Table 21. Host and DIMM Region Register Map

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x00	Serial Number	SERIAL NUMBER – BYTE 0								--	ROE
0x01	Serial Number	SERIAL NUMBER – BYTE 1								--	ROE
0x02	Serial Number	SERIAL NUMBER – BYTE 2								--	ROE
0x03	Serial Number	SERIAL NUMBER – BYTE 3								--	ROE
0x04	Global ERR Log	COUNT	BUCK_OV_OR_UV	VIN_BULK_OV	OTP	RV				0x00	ROE
0x05	PMIC Fault ERR Log	RV	A_NO_PG	RV	B_NO_PG	C_NO_PG	PMIC_ERROR_LOG			0x00	ROE
0x06	UVLO/OV ERR Log	A_UVLO	RV	B_UVLO	C_UVLO	A_OV	RV	B_OV	C_OV	0x00	ROE
0x07	Reserved	RV								0x00	ROE
0x08	PMIC Status_0	RV	OTP	A_PG	RV	B_PG	C_PG	RV	VIN_BULK_OV	0x00	RO
0x09	PMIC Status_1	HTW	RV	LDO_1.8V_PG	RV	A_HCW	RV	B_HCW	C_HCW	0x00	RO
0x0A	PMIC Status_2	A_OV	RV	B_OV	C_OV	PEC_ERR	PARITY_ERR	IBI	RV	0x00	RO
0x0B	PMIC Status_3	A_OC	RV	B_OC	C_OC	A_UVLO	RV	B_UVLO	C_UVLO	0x00	RO
0x0C	SWA Current & Power Measurement	SWA_OUTPUT_CURRENT_POWER_MEASUREMENT								0x00	RO
0x0D	Serial Number	SERIAL NUMBER – BYTE 4								--	ROE
0x0E	SWB Current & Power Measurement	SWB_OUTPUT_CURRENT_POWER_MEASUREMENT								0x00	RO
0x0F	SWC Current & Power Measurement	SWC_OUTPUT_CURRENT_POWER_MEASUREMENT								0x00	RO
0x10	Clear Status Bits_0	RV		A_PG	RV	B_PG	C_PG	RV	VIN_BULK_OV	0x00	W1O
0x11	Clear Status Bits_1	HTW	RV	LDO_1.8V_PG	RV	A_HCW	RV	B_HCW	C_HCW	0x00	W1O
0x12	Clear Status Bits_2	A_OV	RV	B_OV	C_OV	PEC_ERR	PARITY_ERR	RV		0x00	W1O
0x13	Clear Status Bits_3	A_OC	RV	B_OC	C_OC	A_UVLO	RV	B_UVLO	C_UVLO	0x00	W1O
0x14	Clear Status Bits_4	RV				VIN_BULK_UV	LDO_1.0V_PG	RV	GLOBAL_CLR	0x00	W1O
0x15	Mask Status_0	RV		A_PG	RV	B_PG	C_PG	RV	VIN_BULK_OV	0x2C	RW
0x16	Mask Status_1	HTW	RV	LDO_1.8V_PG	RV	A_HCW	RV	B_HCW	C_HCW	0x20	RW
0x17	Mask Status_2	A_OV	RV	B_OV	C_OV	PEC_ERR	PARITY_ERR	RV		0x00	RW
0x18	Mask Status_3	A_OC	RV	B_OC	C_OC	A_UVLO	RV	B_UVLO	C_UVLO	0x00	RW

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x19	Mask Status_4	RV				VIN_BULK_UV	LDO_1.0V_PG	RV		0x04	RW
0x1A	Threshold Settings_1	RV			QUIESCENT_STATE_EN	RV	LDO_1.8V_PG	POWER_MEAS_SEL	LDO_1.0V_PG	0x00	RW
0x1B	Threshold Settings_2	VIN_BULK_OV	CURRENT_OR_POWER_SEL	RV	PWR_GOOD_MASK	GSI_N_EN	HTW			0x05	RW
0x1C	SWA High Current Warning Threshold	SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_TH								0x30	RW
0x1D	Reserved	RV								0x00	RV
0x1E	SWB High Current Warning Threshold	SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_TH								0x30	RW
0x1F	SWC High Current Warning Threshold	SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_TH								0x10	RW
0x20	OC Threshold	A_OC		RV		B_OC		C_OC		0xCF	RW
0x21	SWA Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RW
0x22	SWA Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RW
0x23	Reserved	RV								0x00	RV
0x24	Reserved	RV								0x00	RV
0x25	SWB Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RW
0x26	SWB Threshold	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RW
0x27	SWC Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RW
0x28	SWC Threshold	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RW
0x29	FSW & Mode_1	A_MODE_SEL		A_FSW		RV				0x80	RW
0x2A	FSW & Mode_2	B_MODE_SEL		B_FSW		C_MODE_SEL		C_FSW		0x88	RW
0x2B	LDO Output Voltage Range	LDO_1.8V_VOLTAGE		RV			LDO_1.0V_VOLTAGE		RV	0x42	RW
0x2C	Soft-start Time_1	A_SOFT_START_TIME			RV					0x20	RW
0x2D	Soft-start Time_2	B_SOFT_START_TIME			RV	C_SOFT_START_TIME			RV	0x22	RW
0x2E	OTP Threshold	RV					OTP			0x04	RW
0x2F	PMIC Configuration	RV	A_EN	RV	B_EN	C_EN	WRITE_PROTECTION	MASK_BITS_REGISTER_CONTROL		0x02	RW
0x30	ADC Enable	ADC_EN	ADC_SEL				RV	ADC_UPDATE_FREQ		0x00	RW
0x31	ADC Read	ADC_READ								0x00	RO

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x32	PMIC_EN & Interface Selection	VR_EN	I2C/I3C	PWR_GOOD_IO_TYPE	PMIC_PWR_GOOD_CTRL_OUTPUT_SETTING		RV	ADC_ACCURACY_STEP_SIZE		0x00	RW/RO/RV
0x33	PMIC Status_4	TEMP_MEAS			RV	VIN_BULK_UV_LOCKOUT	LDO_1.0V_PG	RV		0x00	RO
0x34	PEC/IBI/PARITY/HID_CODE	PEC_EN	IBI_EN	PARITY_DIS	RV	HID_CODE			RV	0x0E	RW/RO
0x35	Error Injection	EN	RAIL_SEL			OV_UV_ERR_TYPE	MISC_ERROR_TYPE			0x00	RW
0x36	SOFT_STOP_EXTENSION & ASM	SWA_SOFT_STOP_EXTENSION	RV	SWB_SOFT_STOP_EXTENSION	SWC_SOFT_STOP_EXTENSION	ACOUSTIC_NOISE_PREVENTION_CONTROL			RV	0x02	RV
0x37	DIMM Vendor Region Password Lower Byte	DIMM_VENDOR_PASSWORD_L								0x00	WO
0x38	DIMM Vendor Region Password Upper Byte	DIMM_VENDOR_PASSWORD_H								0x00	WO
0x39	DIMM Vendor Password Control	DIMM_VENDOR_PASSWORD_CONTROL								0x00	RW
0x3A	Default Address Pointer Function	RV	EN	STARTING_ADDRESS		BURST_LENGTH		RV		0x00	RW
0x3B	Revision ID	RV	PMIC_PART_CAPABILITY	MAJREV		MINREV			PMIC_CC_SEL	--	ROE
0x3C	Vendor ID Byte_0	VENDOR_ID_BYTE0								0x8A	ROE
0x3D	Vendor ID Byte_1	VENDOR_ID_BYTE1								0x8C	ROE
0x3E	Reserved	RV								0x00	ROE
0x3F	Reserved	RV								0x00	ROE
0x40	Power-on sequence Configuration 0	SEQ_EN	A_EN	RV	B_EN	C_EN	IDLE_TIME			0x89	RWPE
0x41	Power-on sequence Configuration 1	SEQ_EN	A_EN	RV	B_EN	C_EN	IDLE_TIME			0xD9	RWPE
0x42	Power-on sequence Configuration 2	SEQ_EN	A_EN	RV	B_EN	C_EN	IDLE_TIME			0x00	RWPE
0x43	Reserved	RV								0x00	RV

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x44	SOFT_STOP_EXTENSION	SWA_SOFT_STOP_EXTENSION	RV	SWB_SOFT_STOP_EXTENSION	SWC_SOFT_STOP_EXTENSION	RV				0x00	RW
0x45	DIMM_SWA Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RWPE
0x46	DIMM_SWA Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RWPE
0x47	Reserved	RV								0x00	RV
0x48	Reserved	RV								0x00	RV
0x49	DIMM_SWB Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RWPE
0x4A	DIMM_SWB Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RWPE
0x4B	DIMM_SWC Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RWPE
0x4C	DIMM_SWC Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RWPE
0x4D	DIMM_FSW & Mode_1	A_MODE_SEL		A_FSW		Reserved				0x80	RWPE
0x4E	DIMM_FSW & Mode_2	B_MODE_SEL		B_FSW		C_MODE_SEL		C_FSW		0x88	RWPE
0x4F	Single_Dual Mode	RV							AB_PHASE_MODE	0x00	RWPE
0x50	DIMM_OC Threshold	A_OC		RV		B_OC		C_OC		0xCF	RWPE
0x51	DIMM_LDO Output Voltage Range	LDO_1.8V_VOLTAGE		RV			LDO_1.0V_VOLTAGE		RV	0x42	RWPE
0x52	Reserved	RV								0x00	RV
0x53	Reserved	RV								0x00	RV
0x54	Reserved	RV								0x00	RV
0x55	Reserved	RV								0x00	RV
0x56	Reserved	RV								0x00	RV
0x57	Reserved	RV								0x00	RV
0x58	Power-off sequence Configuration 0	SEQ_EN	A_DIS	RV	B_DIS	C_DIS	IDLE_TIME			0xD1	RWPE
0x59	Power-off sequence Configuration 1	SEQ_EN	A_DIS	RV	B_DIS	C_DIS	IDLE_TIME			0xD9	RWPE

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x5A	Power-off sequence Configuration 2	SEQ_EN	A_DIS	RV	B_DIS	C_DIS	IDLE_TIME			0x00	RWPE
0x5B	Reserved	RV								0x00	RV
0x5C	Reserved	RV								0x00	RV
0x5D	DIMM_Soft-start Time_1	A_SOFT_START_TIME			RV					0x20	RWPE
0x5E	DIMM_Soft-start Time_2	B_SOFT_START_TIME			RV	C_SOFT_START_TIME			RV	0x22	RWPE

17.5 Host Region Registers

Table 22. Serial Number – BYTE 0

Address: 0x00 **Description:** Serial Number – BYTE 0			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	--	R00 [7:0]: SERIAL_NUMBER_BYTE_0 Byte 0 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 23. Serial Number – BYTE 1

Address: 0x01 **Description:** Serial Number – BYTE 1			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	--	R01 [7:0]: SERIAL_NUMBER_BYTE_1 Byte 1 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 24. Serial Number – BYTE 2

Address: 0x02 **Description:** Serial Number – BYTE 2			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	--	R02 [7:0]: SERIAL_NUMBER_BYTE_2 Byte 2 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 25. Serial Number – BYTE 3

Address: 0x03 **Description:** Serial Number – BYTE 3			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	--	R03 [7:0]: SERIAL_NUMBER_BYTE_3 Byte 3 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 26. Global Error Log

Address: 0x04 **Description:** Global Error Log			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation 0 = No Error or Only 1 Error Since Last Erase Operation 1 = > 1 Error Count since last Erase Operation
6	ROE	0	R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Buck Regulator Output Overvoltage or Undervoltage 0 = No Error 1 = Error
5	ROE	0	R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOTLAGE Global Error VIN_BULK Overvoltage 0 = No Error 1 = Error
4	ROE	0	R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Critical Temperature 0 = No Error 1 = Error
3:0	RV	0	R04 [3:0]: Reserved

Table 27. PG-On-Reset ERR Log

Address: 0x05 **Description:** PG-on-Reset ERR Log			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R05 [7]: Reserved
6	ROE	0	R05 [6]: SWA_Power_Good PMIC Power On - SWA Power Not Good 0 = Normal Power On 1 = SWA Power Not Good
5	RV	0	R05 [5]: Reserved
4	ROE	0	R05 [4]: SWB_Power_Good PMIC Power On - SWB Power Not Good 0 = Normal Power On 1 = SWB Power Not Good
3	ROE	0	R05 [3]: SWC_Power_Good PMIC Power On - SWC Power Not Good 0 = Normal Power On 1 = SWC Power Not Good
2:0	ROE	0	R05 [2:0]: PMIC_ERROR_LOG PMIC Power On - High Level Status Bit to Indicate previous power down cycle 000 = Normal Power On 001 = Reserved 010 = Buck Regulator Output Overvoltage or Undervoltage 011 = Critical Temperature 100 = VIN_BULK Input Overvoltage 101 = Reserved 110 = Reserved 111 = VIN_Bulk Undervoltage

Table 28. UVLO/OV ERR Log

Address: 0x06 **Description:** UVLO/OV ERR Log			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R06 [7]: SWA_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWA Undervoltage-Lockout 0 = Normal Power On 1 = Power On - SWA Undervoltage-Lockout
6	RV	0	R06 [6]: Reserved
5	ROE	0	R06 [5]: SWB_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWB Undervoltage-Lockout 0 = Normal Power On 1 = Power On - SWB Undervoltage-Lockout
4	ROE	0	R06 [4]: SWC_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWC Undervoltage-Lockout 0 = Normal Power On 1 = Power On - SWC Undervoltage-Lockout
3	ROE	0	R06 [3]: SWA_OVER_VOLTAGE PMIC Power On – SWA Overvoltage 0 = Normal Power On 1 = Power On - SWA Overvoltage
2	RV	0	R06 [2]: Reserved
1	ROE	0	R06 [1]: SWB_OVER_VOLTAGE PMIC Power On – SWB Overvoltage 0 = Normal Power On 1 = Power On - SWB Overvoltage
0	ROE	0	R06 [0]: SWC_OVER_VOLTAGE PMIC Power On – SWC Overvoltage 0 = Normal Power On 1 = Power On - SWC Overvoltage

Table 29. Reserved R07

Address: 0x07 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	0	R07 [7:0]: Reserved

Table 30. Power-Good Status

Address: 0x08 **Description:** Power-Good Status			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R08 [7]: Reserved
6	RO	0	R08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown
5	RO	0	R08 [5]: SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power-Good Status 0 = Power-Good 1 = Not Good
4	RV	0	R08 [4]: Reserved
3	RO	0	R08 [3]: SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power-Good Status 0 = Power-Good 1 = Not Good
2	RO	0	R08 [2]: SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power-Good Status 0 = Power-Good 1 = Not Good
1	RV	0	R08 [1]: Reserved
0	RO	0	R08 [0]: VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_BULK Input Supply Overvoltage Status 0 = No Overvoltage 1 = Overvoltage

Table 31. HT, PG, Switch Over, High Current Warning

Address: 0x09 **Description:** HT, PG, Switch Over, High Current Warning			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R09 [7]: PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold
6	RV	0	R09 [6]: Reserved
5	RO	0	R09 [5]: VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS VLDO_1.8V Output Power-Good Status 0 = Power-Good 1 = Power Not Good
4	RV	0	R09 [4]: Reserved
3	RO	0	R09[3]: SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node A High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
2	RV	0	R09 [2]: Reserved
1	RO	0	R09 [1]: SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node B High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
0	RO	0	R09 [0]: SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node C High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning

Table 32. SW[A:D] OV Status & PEC/Parity/IBI Status

Address: 0x0A **Description:** SW[A:D] OV Status & PEC/Parity/IBI Status			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0A [7]: SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
6	RV	0	R0A [6]: Reserved
5	RO	0	R0A [5]: SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
4	RO	0	R0A [4]: SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
3	RO	0	R0A [3]: PEC_ERROR_STATUS Packet Error Code Status 0 = No PEC Error 1 = PEC Error
2	RO	0	R0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status 0 = No Parity Error 1 = Parity Error
1	RO	0	R0A [1]: IBI_AND_GLOBAL_STATUS In Band Interrupt and Global Status 0 = No Pending IBI or Outstanding Status 1 = Pending IBI or Outstanding Status
0	RV	0	R0A [0]: Reserved

Table 33. SW[A:D] Current Limited and UVLO

Address: 0x0B **Description:** SW[A:D] Current Limited and UVLO			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0B [7]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
6	RV	0	R0B [6]: Reserved
5	RO	0	R0B [5]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
4	RO	0	R0B [4]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
3	RO	0	R0B [3]: SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Undervoltage-Lockout Status 0 = No Undervoltage-Lockout 1 = Undervoltage-Lockout
2	RV	0	R0B [2]: Reserved
1	RO	0	R0B [1]: SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Undervoltage-Lockout Status 0 = No Undervoltage-Lockout 1 = Undervoltage-Lockout
0	RO	0	R0B [0]: SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Undervoltage-Lockout Status 0 = No Undervoltage-Lockout 1 = Undervoltage-Lockout

Table 34. SWA Current and Power Measurement

Address: 0x0C **Description:** SWA Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R0C [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT If Register R1A [1] = 0, Switch Node A Output Current or Output Power Measurement 0000 0000 = Un-defined 0000 0001 = 125 or 31.25 mA/mW 0000 0010 = 250 or 62.5 mA/mW 0000 0011 = 375 or 93.75 mA/mW 0000 0100 = 500 or 125 mA/Mw … 1111 1111 ≥ 31.875 or 7.968 A/W If Register 0x1A[1] = 1: Sum of SWA, SWB and SWC Output Power 0000 0000 = Undefined 0000 0001 = 125 mW 0000 0010 = 250 mW 0000 0011 = 375 mW 0000 0100 = 500 mW ... 1111 1100 = 31500 mW 1111 1101 = 31625 mW 1111 1110 = 31750 mW 1111 1111 ≥ 31875 mW

Table 35. Serial Number – BYTE 4

Address: 0x0D **Description:** Serial Number – BYTE 4			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	0	R0D [7:0]: SERIAL_NUMBER_BYTE_4 Byte 4 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 36. SWB Current and Power Measurement

Address: 0x0E **Description:** SWB Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R0E [7:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power Measuremen 000000 = Un-defined 0000 0001 = 125 or 31.25 mA/mW 0000 0010 = 250 or 62.5 mA/mW 0000 0011 = 375 or 93.75 mA/mW 0000 0100 = 500 or 125 mA/mW ... 1111 1111 ≥ 31.875 or 7.968 A/W

Table 37. SWC Current and Power Measurement

Address: 0x0F **Description:** SWC Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R0F [7:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power Measurement 0000 0001 = 125 or 31.25 mA/mW 0000 0010 = 250 or 62.5 mA/mW 0000 0011 = 375 or 93.75 mA/mW 0000 0100 = 500 or 125 mA/mW ... 1111 1111 ≥ 31.875 or 7.968 A/W

Table 38. Clear Status Bits_0

Address: 0x10 **Description:** Clear Status Bits_0			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R10 [7:6]: Reserved
5	1O	0	R10 [5]: CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power-Good Status. 1 = Clear “Register R08” [5]
4	RV	0	R10 [4]: Reserved
3	1O	0	R10 [3]: CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS Clear SWB Output Power-Good Status. 1 = Clear “Register R08” [4]
2	1O	0	R10 [2]: CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power-Good Status. 1 = Clear “Register R08” [3]
1	RV	0	R10 [1]: Reserved
0	1O	0	R10 [0]: CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear 12V Input Supply Overvoltage Status. 1 = Clear “Register R08” [0]

Table 39. Clear Status Bits_1

Address: 0x11 **Description:** Clear Status Bits_1			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R11 [7]: CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS Clear PMIC High Temperature Warning Status 1 = Clear “Register R09” [7]
6	RV	0	R11 [6]: Reserved
5	1O	0	R11 [5]: CLEAR_VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS Clear VLDO_1.8V Output Power-Good Status 1 = Clear “Register R09” [5]
4	RV	0	R11 [4]: Reserved
3	1O	0	R11 [3]: CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node A High Output Current Consumption Warning Status. 1 = Clear “Register R09” [3]
2	RV	0	R11 [2]: Reserved
1	1O	0	R11 [1]: CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node B High Output Current Consumption Warning Status. 1 = Clear “Register R09” [1]
0	1O	0	R11 [0]: CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node C High Output Current Consumption Warning Status. 1 = Clear “Register R09” [0]

Table 40. Clear Status Bits_2

Address: 0x12 **Description:** Clear Status Bits_2			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R12 [7]: CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Overvoltage Status. 1 = Clear “Register R0A” [7]
6	RV	0	R12 [6]: Reserved
5	1O	0	R12 [5]: CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node B Output Overvoltage Status. 1 = Clear “Register R0A” [5]
4	1O	0	R12 [4]: CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Overvoltage Status. 1 = Clear “Register R0A” [4]
3	1O	0	R12 [3]: CLEAR_PEC_ERROR_STATUS Clear PEC Error Status. 1 = Clear “Register R0A” [3]
2	1O	0	R12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear “Register R0A” [2]
1:0	RV	0	R12 [1:0]: Reserved

Table 41. Clear Status Bits_3

Address: 0x13 **Description:** Clear Status Bits_3			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node A Output Current Limiter Warning Status. 1 = Clear “Register R0B” [7]
6	RV	0	R13 [6]: Reserved
5	1O	0	R13 [5]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node B Output Current Limiter Warning Status. 1 = Clear “Register R0B” [5]
4	1O	0	R13 [4]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node C Output Current Limiter Warning Status. 1 = Clear “Register R0B” [4]
3	1O	0	R13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node A Output Undervoltage Lockout Status. 1 = Clear “Register R0B” [3]
2	RV	0	R13 [2]: Reserved
1	1O	0	R13 [1]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node B Output Undervoltage Lockout Status. 1 = Clear “Register R0B” [1]
0	1O	0	R13 [0]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node C Output Undervoltage Lockout Status. 1 = Clear “Register R0B” [0]

Table 42. Clear Status Bits_4

Address: 0x14 **Description:** Clear Status Bits_4			
Bits	**Attribute**	**Default**	**Description**
7:4	RV	0	R14 [7:4]: Reserved
3	1O	0	R14 [3]: CLEAR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Clear VIN_Bulk Input UnderVoltage-Lockout Status 1 = Clear ”Register 0x33” [3]
2	1O	0	R14 [2]: CLEAR_VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS Clear VLDO_1.0V Output Power-Good Status 1 = Clear “Register R33” [2]
1	RV	0	R14 [1]: Reserved
0	1O	0	R14 [0]: GLOBAL_CLEAR_STATUS Clear all status bits. 1 = Clear all status bits

Table 43. Mask Status_0

Address: 0x15 **Description:** Mask Status_0			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R15 [7:6]: Reserved
5	RW	1	R15 [5]: MASK_SWA_OUTPUT_POWER_GOOD_STATUS Mask SWA Output Power-Good Status Event 0 = Do Not Mask SWA Output Power-Good Status Event 1 = Mask SWA Output Power-Good Status Event
4	RV	0	R15 [4]: Reserved
3	RW	1	R15 [3]: MASK_SWB_OUTPUT_POWER_GOOD_STATUS Mask SWB Output Power-Good Status Event 0 = Do Not Mask SWB Output Power-Good Status Event 1 = Mask SWB Output Power-Good Status Event
2	RW	1	R15 [2]: MASK_SWC_OUTPUT_POWER_GOOD_STATUS Mask SWC Output Power-Good Status Event 0 = Do Not Mask SWC Output Power-Good Status Event 1 = Mask SWC Output Power-Good Status Event
1	RV	0	R15 [1]: Reserved
0	RW	0	R15 [0]: MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Bulk Input Supply Overvoltage Status Event 0 = Do Not Mask VIN_Bulk Input Supply Overvoltage Status Event 1 = Mask VIN_Bulk Input Supply Overvoltage Status Event

Table 44. Mask Status_1

Address: 0x16 **Description:** Mask Status_1			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R16 [7]: MASK_PMIC_HIGH_TEMP_WARNING_STATUS Mask PMIC High Temperature Warning Status Event 0 = Do Not Mask PMIC High Temperature Warning Status Event 1 = Mask PMIC High Temperature Warning Status Event
6	RV	0	R16 [6]: Reserved
5	RW	1	R16 [5]: MASK_VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS Mask VLDO_1.8V Output Power-Good Status Event 0 = Do Not Mask VLDO_1.8V Output Power-Good Status Event 1 = Mask VLDO_1.8V Output Power-Good Status Event
4	RV	0	R16 [4]: Reserved
3	RW	0	R16 [3]: MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node A High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Consumption Warning Status Event 1 = Mask Switch Node A Output Current Consumption Warning Status Event
2	RV	0	R16 [2]: Reserved
1	RW	0	R16 [1]: MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node B High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node B Output Current Consumption Warning Status Event 1 = Mask Switch Node B Output Current Consumption Warning Status Event
0	RW	0	R16 [0]: MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node C High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Consumption Warning Status Event 1 = Mask Switch Node C Output Current Consumption Warning Status Event

Table 45. Mask Status_2

Address: 0x17 **Description:** Mask Status_2			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R17 [7]: MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS Mask SWA Output Overvoltage Status Event 0 = Do Not Mask SWA Output Overvoltage Status Event 1 = Mask SWA Output Overvoltage Status Event
6	RV	0	R17 [6]: Reserved
5	RW	0	R17 [5]: MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS Mask SWB Output Overvoltage Status Event 0 = Do Not Mask SWB Output Overvoltage Status Event 1 = Mask SWB Output Overvoltage Status Event
4	RW	0	R17 [4]: MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS Mask SWC Output Overvoltage Status Event 0 = Do Not Mask SWC Output Overvoltage Status Event 1 = Mask SWC Output Overvoltage Status Event
3	RW	0	R17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n output Only 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status
2	RW	0	R17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n output Only 0 = Do Not Mask Parity Error Status Event 1 = Mask Parity Error Status
1:0	RV	0	R17 [1:0]: Reserved

Table 46. Mask Status_3

Address: 0x18 **Description:** Mask Status_3			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R18 [7]: MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node A Output Current Limiter Warning Status Event 0 = Do Not Mask Switch Node A Output Current Limiter Warning Status Event 1 = Mask Switch Node A Output Current Limiter Warning Status Event
6	RV	0	R18 [6]: Reserved
5	RW	0	R18 [5]: MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node B Output Current Limiter Warning Status Event 0 = Do Not Mask Switch Node B Output Current Limiter Warning Status Event 1 = Mask Switch Node B Output Current Limiter Warning Status Event
4	RW	0	R18 [4]: MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node C Output Current Limiter Warning Status Event 0 = Do Not Mask Switch Node C Output Current Limiter Warning Status Event 1 = Mask Switch Node C Output Current Limiter Warning Status Event
3	RW	0	R18 [3]: MASK_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node A Output Undervoltage Lockout Status Event 0 = Do Not Mask Switch Node A Output Undervoltage Lockout Status Event 1 = Mask Switch Node A Output Undervoltage Lockout Status Event
2	RV	0	R18 [2]: Reserved
1	RW	0	R18 [1]: MASK_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node B Output Undervoltage Lockout Status Event 0 = Do Not Mask Switch Node B Output Undervoltage Lockout Status Event 1 = Mask Switch Node B Output Undervoltage Lockout Status Event
0	RW	0	R18 [0]: MASK_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node C Output Undervoltage Lockout Status Event 0 = Do Not Mask Switch Node C Output Undervoltage Lockout Status Event 1 = Mask Switch Node C Output Undervoltage Lockout Status Event

Table 47. Mask Status_4

Address: 0x19 **Description:** Mask Status_4			
Bits	**Attribute**	**Default**	**Description**
7:4	RV	0	R19 [7:4]: Reserved
3	RW	0	R19 [3]: MASK_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Mask VIN_Bulk Input Under Voltage Lockout Event 0 = Do Not Mask VIN_Bulk Input Under Voltage Lockout 1 = Mask VIN_Bulk Input Under Voltage Lockout
2	RW	1	R19 [2]: MASK_VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS Mask VLDO_1.0V Output Power-Good Status Event 0 = Do Not Mask VLDO_1.0V Output Power-Good Status Event 1 = Mask VLDO_1.0V Output Power-Good Status Event
1:0	RV	0	R19 [1:0]: Reserved

Table 48. IN/OUT PG/UVLO TH

Address: 0x1A **Description:** IN/OUT PG/UVLO TH			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	110	VIN_BULK_POWER_GOOD_THRESHOLD_VOLTAGE VIN Bulk Input Threshold Voltage for Input Power-Good Status for input s upply 000 = Reserved (9.5V) 001 = 9.5V 010 = 8.5V 011 = 7.5V 100 = 6.5V 101 = 5.5V 110 = 4.25V 111 = Reserved (4.25V)
4	RW	0	R1A [4]: QUIESCENT_STATE_EN 0 = Disable 1 = Enable
3	RV	0	R1A [3]: Reserved
2	RW	0	R1A [2]: VLDO_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VLDO_1.8V LDO Output Threshold Voltage for Power-Good Status 0 = 1.6V 1 = Reserved
1	RW	0	R1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select 0 = Report Power Measurement for Each Rail in R0C, R0E & R0F 1 = Report Total Power Measurement of Each Rail in R0C
0	RW	0	R1A [0]: VLDO_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VLDO_1.0V LDO Output Threshold Voltage for Power-Good Status 0 = –10% from the setting in “Register R51” [2:1] 1 = –15% from the setting in “Register R51” [2:1]

Table 49. OV/OT_TH; GSI EN; Global PG MASK

Address: 0x1B **Description:** OV/OT_TH; GSI EN; Global PG MASK			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_BULK Input Overvoltage Threshold Setting For GSI_n Assertion 0 = 5.8V to 6V (Varies across vendors) 1 = Reserved
6	RW	0	R1B [6]: CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter 0 = Report Current Measurements in registers 1 = Report Power Measurements in registers
5	RV	0	R1B [5]: Reserved
4	RW	0	R1B [4]: GLOBAL_PWR_GOOD_PIN_STATUS_MASK Global Mask PWR_GOOD Output Pin 0 = Not Masked 1 = Masked
3	RW	0	R1B [3]: GSI_N_OUTPUT_PIN_ENABLE Enable GSI_n Output Pin 0 = Disable GSI_n Output Pin 1 = Enable GSI_n Output Pin
2:0	RW	101	R1B [2:0]: PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold 000 = Reserved 001 = PMIC temperature > 85°C 010 = PMIC temperature > 95°C 011 = PMIC temperature > 105°C 100 = PMIC temperature > 115°C 101 = PMIC temperature > 125°C 110 = PMIC temperature > 135°C 111 = Reserved

Table 50. SWA High Current Warning Threshold

Address: 0x1C **Description:** SWA High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	00110000	R1C [7:0]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold If 0x32 [1:0] = 01: 0000 0000 = Undefined 0000 0001 = 31.25mA 0000 0010 = 62.5mA 0000 0011 = 93.75mA 0000 0100 = 125mA ... 1100 0000 = 6.0A ... 1111 1111 = 7.968A If Register 0x32[1:0] = 00: 0000 0000 = Undefined 0000 0001 = 0.125A 0000 0010 = 0.250A ... 0011 0000 = 6.0A (Default) ... 1111 1111 = 31.875A

Table 51. Reserved

Address: 0x1D **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R1D [7:0]: Reserved

Table 52. SWB High Current Warning Threshold

Address: 0x1E **Description:** SWB High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0011 0000	R1E [7:0]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node B Output High Current Consumption Warning Threshold If Register 0x32[1:0] = 01: 0000 0000 = Undefined 0000 0001 = 31.25 mA 0000 0010 = 62.5 mA 0000 0011 = 93.75 mA 0000 0100 = 125mA ... 1100 0000 = 6.0 A ... 1111 1111 = 7.968 A If Register 0x32[1:0] = 00: 0000 0000 = Undefined 0000 0001 = 0.125 A 0000 0010 = 0.250 A ... 0011 0000 = 6.0 A (Default) ... 1111 1111 = 31.875A

Table 53. SWC High Current Warning Threshold

Address: 0x1F **Description:** SWC High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0001 0000	R1F [7:0]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold If Register 0x32[1:0] = 01: 0000 0000 = Undefined 0000 0001 = 31.25 mA 0000 0010 = 62.5 mA 0000 0011 = 93.75 mA 0000 0100 = 125mA ... 0100 0000 = 2.0 A ... 1111 1111 = 7.968 A If Register 0x32[1:0] = 00: 0000 0000 = Undefined 0000 0001 = 0.125 A 0000 0010 = 0.250 A ... 0001 0000 = 2.0A (Default) ... 1111 1111 = 31.875A

Table 54. SW[A:D] Current Limited Warning TH

Address: 0x20 **Description:** SW[A:D] Current Limited Warning TH			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	11	R20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING High Current PMIC Encoding Definition For Constant On Time (COT) Mode, Ivalley_limit: 00 = 4.5A 01 = 5.5A 10 = 6.5A 11 = 8.0A
5:4	RV	0	R20 [5:4]: Reserved
3:2	RW	11	R20 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING High Current PMIC Encoding Definition For Constant On Time (COT) Mode, Ivalley_limit: 00 = 4.5A 01 = 5.5A 10 = 6.5A 11 = 8.0A
1:0	RW	11	R20 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING High Current PMIC Encoding Definition For Constant On Time (COT) Mode, Ivalley_limit: 00 = 1.5A 01 = 2.0A 10 = 2.5A 11 = 3A

Table 55. SWA Voltage Setting

Address: 0x21 **Description:** SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R21 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800 mV 000 0001 = 805 mV 000 0010 = 810 mV ... 011 1100 = 1100 mV ... 111 1101 = 1425 mV 111 1110 = 1430 mV 111 1111 = 1435 mV
0	RW	0	R21 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power-Good Status 0 = –5% from the setting in “Register R21,” [7:1] 1 = –7.5% from the setting in “Register R21,” [7:1]

Table 56. SWA Threshold

Address: 0x22 **Description:** SWA Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R22 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound level” For Power-Good Status 00 = +5% from the setting in “Register R21,” [7:1] 01 = +7.5% from the setting in “Register R21,” [7:1] 10 = +10% from the setting in “Register R21,” [7:1] 11 = +2.5% from the setting in “Register R21,” [7:1]
5:4	RW	10	R22 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R21,” [7:1] 01 = +10% from the setting in “Register R21,” [7:1] 10 = +12.5% from the setting in “Register R21,” [7:1] 11 = +20% from the setting in “Register R21,” [7:1]
3:2	RW	00	R22 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Undervoltage-Lockout Status 00 = –10% from the setting in “Register R21,” [7:1] 01 = –12.5% from the setting in “Register R21,” [7:1] 10 = –7.5% from the setting in “Register R21,” [7:1] 11 = –20% from the setting in “Register R21,” [7:1]
1:0	RW	11	R22 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 57. Reserved

Address: 0x23 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R23 [7:0]: Reserved

Table 58. Reserved

Address: 0x24 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R24 [7:0]: Reserved

Table 59. SWB Voltage Setting

Address: 0x25 **Description:** SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R25 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800 mV 000 0001 = 805 mV 000 0010 = 810 mV ... 011 1100 = 1100 mV ... 111 1101 = 1425 mV 111 1110 = 1430 mV 111 1111 = 1435 mV
0	RW	0	R25 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power-Good Status 0 = –5% from the setting in “Register R25,” [7:1] 1 = –7.5% from the setting in “Register R25,” [7:1]

Table 60. SWB Threshold

Address: 0x26 **Description:** SWB Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R26 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power-Good Status 00 = +5% from the setting in “Register R25” [7:1] 01 = +7.5% from the setting in “Register R25” [7:1] 10 = +10% from the setting in “Register R25” [7:1] 11 = +2.5% from the setting in “Register R25” [7:1]
5:4	RW	10	R26 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R25” [7:1] 01 = +10% from the setting in “Register R25” [7:1] 10 = +12.5% from the setting in “Register R25” [7:1] 11 = +20% from the setting in “Register R25” [7:1]
3:2	RW	00	R26 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Undervoltage-Lockout Status 00 = –10% from the setting in “Register R25” [7:1] 01 = –12.5% from the setting in “Register R25” [7:1] 10 = –7.5% from the setting in “Register R25” [7:1] 11 = –20% from the setting in “Register R25” [7:1]
1:0	RW	11	R26 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 61. SWC Voltage Setting

Address: 0x27 **Description:** SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R27 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting 000 0000 = 1500 mV 000 0001 = 1505 mV 000 0010 = 1510 mV ... 011 1100 = 1800 mV ... 111 1101 = 2125 mV 111 1110 = 2130 mV 111 1111 = 2135 mV
0	RW	0	R27 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power-Good Status 0 = –5% from the setting in “Register R27” [7:1] 1 = –7.5% from the setting in “Register R27” [7:1]

Table 62. SWC Threshold

Address: 0x28 **Description:** SWC Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R28 [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R27” [7:1] 01 = +7.5% from the setting in “Register R27” [7:1] 10 = +10% from the setting in “Register R27” [7:1] 11 = +2.5% from the setting in “Register R27” [7:1]
5:4	RW	10	R28 [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R27” [7:1] 01 = +10% from the setting in “Register R27” [7:1] 10 = +12.5% from the setting in “Register R27” [7:1] 11 = +20% from the setting in “Register R27” [7:1]
3:2	RW	00	R28 [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register R27” [7:1] 01 = –12.5% from the setting in “Register R27” [7:1] 10 = –7.5% from the setting in “Register R27” [7:1] 11 = –20% from the setting in “Register R27” [7:1]
1:0	RW	11	R28 [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

Table 63. SW[A] FSW and Mode

Address: 0x29 **Description:** SW[A] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R29 [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R29 [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:0	RV	0	R29 [3:0]: Reserved

Table 64. SW[B:C] FSW and Mode

Address: 0x2A **Description:** SW[B:C] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R2A [7:6]: SWB_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R2A [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RW	10	R2A [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	00	R2A [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

Table 65. Voltage Setting for VLDO_1.8V & VLDO_1.0V & SW[A:D] Output Voltage Range

Address: 0x2B **Description:** Voltage Setting for VLDO_1.8V & VLDO_1.0V & SW[A:D] Output Voltage Range			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R2B [7:6]: VLDO_1.8V_VOLTAGE_SETTING VLDO_1.8V LDO Output Voltage Setting 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5:3	RV	0	R2B [5:3]: Reserved
2:1	RW	01	R2B [2:1]: VLDO_1.0V_VOLTAGE_SETTING VLDO_1.0V LDO Voltage Setting 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	R2B [0]: Reserved

Table 66. SW[A] Soft-Start

Address: 0x2C **Description:** SW[A] Soft-Start			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2C [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4:0	RV	0	R2C [4:0]: Reserved

Table 67. SW[B] Soft-Start

Address: 0x2D **Description:** SW[B] Soft-Start			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2D [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4	RV	0	R2D [4]: Reserved
3:1	RW	001	R2D [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	R2D [0]: Reserved

Table 68. Shutdown Temperature Threshold

Address: 0x2E **Description:** Shutdown Temperature Threshold			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R2E [7:3]: Reserved
2:0	RW	100	R2E [2:0]: PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature > 105°C 001 = PMIC Temperature > 115°C 010 = PMIC Temperature > 125°C 011 = PMIC Temperature > 135°C 100 = PMIC Temperature > 145°C 101 = Reserved 110 = Reserved 111 = Reserved

Table 69. PMIC Configuration

Address: 0x2F **Description:** PMIC Configuration			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R2F [7]: Reserved
6	RW	0	R2F [6]: SWA_REGULATOR_CONTROL Disable SWA Regulator Output 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R2F [5]: Reserved
4	RW	0	R2F [4]: SWB_REGULATOR_CONTROL Disable SWB Regulator Output 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RW	0	R2F [3]: SWC_REGULATOR_CONTROL Disable SWC Regulator Output 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2	RW	0	R2F [2]: SECURE_MODE PMIC Mode Operation 0 = Secure Mode Operation 1 = Programmable Mode Operation
1:0	RW	10	R2F [1:0]: MASK_BITS_REGISTER_CONTROL Mask Bits Register Control 00 = Mask GSI_n Signal Only (PWR_GOOD Signal will assert) 01 = Mask PWR_GOOD Only (GSI_n signal will assert) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD assert or GSI_n signal will assert) 11 = Reserved

Table 70. ADC Enable

Address: 0x30 **Description:** ADC Enable			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R30 [7]: ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable 1 = Enable
6:3	RW	0	R30 [6:3]: ADC_SELECT Input Selection for ADC Readout 0000 = SWA Output Voltage 0001 = Reserved 0010 = SWB Output Voltage 0011 = SWC Output Voltage 0100 = Reserved 0101 = VIN_BULK Input Voltage 0110 = Reserved 0111 = Reserved 1000 = VLDO_1.8V Output Voltage 1001 = VLDO_1.0V Output Voltage All other encodings are reserved.
2	RV	0	R30[2]: Reserved
1:0	RW	0	R30 [1:0]: ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

Table 71. ADC Read

Address: 0x31 **Description:** ADC Read			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R31 [7:0]: ADC_READ ADC Output Voltage Reading (Applies to SW[A:D], VLDO_1.8V, VLDO_1.0V, VIN_MGMT) 0000 0000 = Undefined 0000 0001 = 15 mV 0000 0010 = 30 mV ... 1111 1111 ≥ 3825 mV ADC Output Voltage Reading (Applies to VIN_Bulk Input Voltage) 0000 0000 = Undefined 0000 0001 = 70 mV 0000 0010 = 140 mV ... 1111 1111 ≥ 17850 mV

Table 72. PMIC_EN and MGMT Interface Selection

Address: 0x32 **Description:** PMIC_EN & MGMT Interface Selection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R32 [7]: VR_ENABLE PMIC Enable 0 = PMIC Disable 1 = PMIC Enable
6	RO	0	R32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection 0 = I^2C Interface (Max speed 1MHz) 1 = I3C Basic Protocol
5	RW	1	R32 [5]: PWR_GOOD_IO_TYPE PMIC PWR_GOOD Output Signal Type 0 = Output Only 1 = Input and Output
4:3	RW	0	R32 [4]: PWR_GOOD_OUTPUT_SIGNAL_CONTROL PMIC PWR_GOOD Output Signal Control 0x = PMIC controls PWR_GOOD on its own based on internal status 10 = PWR_GOOD Output Low 11 = PWR_GOOD Output Floats
2	RV	0	R32 [2]: Reserved
1:0	RW	00	R32 [2:1]: ADC_ACCURACY_STEP_SIZE ADC Accuracy Step Size 00 = 125 mA or 125 mW 01 = 31.25 mA or 31.25 mW All other encodings are reserved

Table 73. Temp_Meas and LDO Status

Address: 0x33 **Description:** Temp_Meas and LDO Status			
Bits	**Attribute**	**Default**	**Description**
7:5	RO	000	R33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature 000 = ≤ 80°C (± 5°C) 001 = 85°C (± 5°C) 010 = 95°C (± 5°C) 011 = 105°C (± 5°C) 100 = 115°C (± 5°C) 101 = 125°C (± 5°C) 110 = 135°C (± 5°C) 111 = ≥140°C (± 5°C)
4	RV	0	R33 [4]: Reserved
3	RO	0	R33 [3]: VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS VIN_Bulk Undervoltage-Lockout Status 0 = No Undervoltage-Lockout 1 = Undervoltage-Lockout
2	RO	0	R33 [2]: VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS VLDO_1.0V LDO Output Power-Good Status 0 = Power-Good 1 = Power Not Good
1:0	RV	0	R33 [1:0]: Reserved

Table 74. PEC/IBI/PARITY/HID_CODE

Address: 0x34 **Description:** PEC/IBI/PARITY/HID_CODE			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R34 [7]: PEC_ENABLE Packet Error Code Enable (Applicable Only if R32 [6] = '1') 0 = Disable 1 = Enable
6	RO	0	R34 [6]: IBI_ENABLE In Band Interrupt Enable (Applicable Only if R32 [6] = '1') 0 = Disable 1 = Enable
5	RO	0	R34 [5]: PARITY_DISABLE T Bit Parity Code Disable (Applicable Only if R32 [6] = '1'.) 0 = Enable 1 = Disable
4	RV	0	R34 [4]: Reserved
3:1	RO	111	R34 [3:1]: HID_CODE PMIC's 3-bit HID Code 000 001 010 011 100 101 110 111
0	RV	0	R34 [0]: Reserved

Table 75. Error Injection

Address: 0x35 **Description:** Error Injection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R35 [7]: Error_Injection_Enable 0 = Disable 1 = Enable
6:4	RW	0	R35 [6:4]: Error_Injection_Rail_Selection 000 = Undefined 001 = SWA Output Only 010 = Reserved 011 = SWB Output Only 100 = SWC Output Only 101 = VIN_BULK Input Only 110 = Reserved 111 = Do Not Use.
3	RW	0	R35 [3]: OVER_VOLTAGE_UNDER_VOLTAGE_SELECT Overvoltage or Undervoltage Selection for Bits [6:4] 0 = Overvoltage 1 = Undervoltage
2:0	RW	0	R35 [2:0]: Misc_Error_Injection_Type 000 = Undefined 001 = Reserved 010 = Critical Temperature Shutdown 011 = High Temperature Warning 100 = VLDO_1.8V LDO Power-Good 101 = High Current Consumption Warning 110 = Reserved 111 = Current Limiter Warning

Table 76. SOFT_STOP_EXTENSION & ASM

Address: 0x36 **Description:** Soft_Stop_Extension & ASM			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R36 [7]: SWA_OUTPUT_SOFT_STOP_TIME_EXTENSION SWA Output Regulator Soft Stop Time After VR Disable 3-bit encoding with {R36[7],R22[1:0]}: 0xx = Encoding determined by R22[1:0] (Default) 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms
6	RV	0	R36 [6]: Reserved
5	RW	0	R36 [5]: SWB_OUTPUT_SOFT_STOP_TIME_EXTENSION SWB Output Regulator Soft Stop Time After VR Disable 3-bit encoding with {R36[5],R26[1:0]}: 0xx = Encoding determined by R26[1:0] (Default) 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms
4	RW	0	R36 [4]: SWC_OUTPUT_SOFT_STOP_TIME_EXTENSION SWC Output Regulator Soft Stop Time After VR Disable 3-bit encoding with {R36[4],R28[1:0]}: 0xx = Encoding determined by R28[1:0] (Default) 100 = 16 ms 101 = 32 ms 110 = 64 ms 111 = 128 ms
3:1	RW	001	R36 [3:1]: ACOUSTIC_NOISE_PREVENTION_CONTROL Acoustic Noise Prevention Control Feature 000 = Feature is disabled 001 = Enable; Switching frequency threshold = 50 kHz 010 = Enable; Switching frequency threshold = 40 kHz 011 = Enable; Switching frequency threshold = 30 kHz 100 = Enable; Switching frequency threshold = 20 kHz
0	RV	0	R36 [0]: Reserved

Table 77. DIMM Vendor Region Password Lower Byte

Address: 0x37 **Description:** DIMM Vendor Region Password Lower Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	0	R37 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE DIMM Vendor Memory Region (R40 to R6F) Password – Lower Byte [7:0] = Code

Table 78. DIMM Vendor Region Password Upper Byte

Address: 0x35 **Description:** DIMM Vendor Region Password Upper Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	0	R38 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE DIMM Vendor Memory Region (R40 to R6F) Password – Upper Byte [7:0] = Code

Table 79. DIMM Vendor Password Control

Address: 0x39 **Description:** DIMM Vendor Password Control			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0	R39 Codes: Host Region Codes: 0x74: Clear Registers R04 to R07, Erase MTP memory for R04 to R07 Registers. DIMM Vendor Region (0x40 to 0x6F) Write Codes: 0x40: Unlock DIMM Vendor Region. Password needs to be present in R37 and R38 registers. 0x00: Lock DIMM Vendor Region. 0x80: Burn DIMM Vendor Region Password. New password needs to be present in R37 and R38. 0x81: Burn DIMM Vendor Region - 0x40 to 0x4F 0x82: Burn DIMM Vendor Region - 0x50 to 0x5F 0x85: Burn DIMM Vendor Region - 0x60 to 0x6F DIMM Vendor Region (0x40 to 0x6F) Read Codes: 0x5A: Burning is complete in DIMM Vendor region.

Table 80. Default Address Pointer

Address: 0x3A **Description:** Default Address Pointer			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R3A [7]: Reserved
6	RW	0	R3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE Enable Default Address Read Pointer when PMIC sees STOP operation 0 = Disable Default Address Pointer (address pointer is set by Host) 1 = Enable Default Address Pointer; Address selected by register bits [5:4]
5:4	RW	0	R3A [5:4]: DEFAULT_READ_STARTING_ADDRESS Default Read Address Pointer Selection when PMIC sees STOP operation 00 = R08 01 = R0C 10 = Reserved 11 = Reserved
3:2	RW	0	R3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode 00 = 2 Bytes 01 = 4 Bytes 10 = Reserved 11 = 16 Bytes
1:0	RV	0	R3A [1:0]: Reserved

Table 81. Revision ID, PMIC Current Capability Selection

Address: 0x3B **Description:** Revision ID, PMIC Current Capability Selection			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R3B [7]: Reserved
6	ROE	--	R3B [6]: PMIC_PART_CAPABILITY PMIC Current Capability 0 = PMIC5100 (Low Current) 1 = PMIC5120 (High Current)
5:4	ROE	--	R3B [5:4]: REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	--	R3B [3:1]: REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 All other encodings are reserved.
0	RV	--	R3B [0]: Reserved

Table 82. Vendor ID Byte 0

Address: 0x3C **Description:** Vendor ID Byte 0			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001010	R3C [7:0]: VENDOR_ID_BYTE0 Vendor Identification Register Byte 0.

Table 83. Vendor ID Byte 1

Address: 0x3D **Description:** Vendor ID Byte 1			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001100	R3D [7:0]: VENDOR_ID_BYTE1 Vendor Identification Register Byte 1.

Table 84. Reserved

Address: 0x3E **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R3E [7:0]: Reserved

Table 85. Reserved

Address: 0x3F **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R3F [7:0]: Reserved

17.6 DIMM Vendor Region Registers

Table 86. Power-On Sequence Configuration 0

Address: 0x40 **Description:** Power-On Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R40 [7]: POWER_ON_SEQUENCE_CONFIG0 PMIC Power-On Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	0	R40 [6]: POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable SWA Output 1 = Enable SWA Output
5	RV	0	R40 [5]: Reserved
4	RWPE	0	R40 [4]: POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable SWB Output 1 = Enable SWB Output
3	RWPE	1	R40 [3]: POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable SWC Output 1 = Enable SWC Output
2:0	RWPE	001	R40 [2:0]: POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power-On Sequence Config0 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

Table 87. Power-On Sequence Configuration 1

Address: 0x41
Description: Power-On Sequence Configuration 1

Bits	Attribute	Default	Description
7	RWPE	1	R41 [7]: POWER_ON_SEQUENCE_CONFIG1 PMIC Power-On Sequence Config1 0 = Do Not Execute Config1 1 = Execute Command
6	RWPE	1	R41 [6]: POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable SWA Output 1 = Enable SWA Output
5	RV	0	R41 [5]: Reserved
4	RWPE	1	R41 [4]: POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable SWB Output 1 = Enable SWB Output
3	RWPE	1	R41 [3]: POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable SWC Output 1 = Enable SWC Output
2:0	RWPE	001	R41 [2:0]: POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power-On Sequence Config1 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

Table 88. Power-On Sequence Configuration 2

Address: 0x42 **Description:** Power-On Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R42 [7]: POWER_ON_SEQUENCE_CONFIG2 PMIC Power-On Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	R42 [6]: POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable SWA Output 1 = Enable SWA Output
5	RV	0	R42 [5]: Reserved
4	RWPE	0	R42 [4]: POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable SWB Output 1 = Enable SWB Output
3	RWPE	0	R42 [3]: POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable SWC Output 1 = Enable SWC Output
2:0	RWPE	000	R42 [2:0]: POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power-On Sequence Config2 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

Table 89. Reserved

Address: 0x43 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R43 [7:0]: Reserved

Table 90. Soft Stop Extension

Address: 0x44 **Description:** Soft Stop Extension			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R44 [7]: SWA_OUTPUT_SOFT_STOP_TIME_EXTENSION SWA Output Regulator Soft Stop Time After VR Disable 3-bit encoding with {R44[7],R46[1:0]}: 0xx = Encoding determined by R46[1:0] (Default) 100 = 8ms 101 = 16ms 110 = 32ms 111 = 64ms
6	RV	0	R44 [6]: Reserved
5	RW	0	R44 [5]: SWB_OUTPUT_SOFT_STOP_TIME_EXTENSION SWB Output Regulator Soft Stop Time After VR Disable 3-bit encoding with {R44[5],R4A[1:0]}: 0xx = Encoding determined by R4A[1:0] (Default) 100 = 8ms 101 = 16ms 110 = 32ms 111 = 64ms
4	RW	0	R44 [4]: SWC_OUTPUT_SOFT_STOP_TIME_EXTENSION SWC Output Regulator Soft Stop Time After VR Disable 3-bit encoding with {R44[4],R4C[1:0]}: 0xx = Encoding determined by R4C[1:0] (Default) 100 = 16ms 101 = 32ms 110 = 64ms 111 = 128ms
3:0	RV	0	R44 [3:0]: Reserved

Table 91. SWA Voltage Setting

Address: 0x45 **Description:** SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R45 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RWPE	0	R45 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power-Good Status 0 = –5% from the setting in “Register R45” [7:1] 1 = –7.5% from the setting in “Register R45” [7:1]

Table 92. SWA Threshold, Soft-Stop Time

Address: 0x46 **Description:** SWA Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R46 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound” For Power-Good Status 00 = +5% from the setting in “Register R45” [7:1] 01 = +7.5% from the setting in “Register R45” [7:1] 10 = +10% from the setting in “Register R45” [7:1] 11 = +2.5% from the setting in “Register R45” [7:1]
5:4	RWPE	10	R46 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R45” [7:1] 01 = +10% from the setting in “Register R45” [7:1] 10 = +12.5% from the setting in “Register R45” [7:1] 11 = +20% from the setting in “Register R45” [7:1]
3:2	RWPE	00	R46 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Undervoltage Lockout Status 00 = −10% from the setting in “Register R45” [7:1] 01 = −12.5% from the setting in “Register R45” [7:1] 10 = −7.5% from the setting in “Register R45” [7:1] 11 = −20% from the setting in “Register R45” [7:1]
1:0	RWPE	11	R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 93. Reserved

Address: 0x47 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R47 [7:0]: Reserved

Table 94. Reserved

Address: 0x48 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R48 [7:0]: Reserved

Table 95. SWB Voltage Setting

Address: 0x49 **Description:** SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R49 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800 mV 000 0001 = 805 mV 000 0010 = 810 mV ... 011 1100 = 1100 mV ... 111 1101 = 1425 mV 111 1110 = 1430 mV 111 1111 = 1435 mV
0	RWPE	0	R49 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power-Good Status 0 = –5% from the setting in “Register R49” [7:1] 1 = –7.5% from the setting in “Register R49” [7:1]

Table 96. SWB Threshold, Soft-Stop Time

Address: 0x4A **Description:** SWB Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4A [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power-Good Status 00 = +5% from the setting in “Register R49” [7:1] 01 = +7.5% from the setting in “Register R49” [7:1] 10 = +10% from the setting in “Register R49” [7:1] 11 = +2.5% from the setting in “Register R49” [7:1]
5:4	RWPE	10	R4A [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R49” [7:2] 01 = +10% from the setting in “Register R49” [7:1] 10 = +12.5% from the setting in “Register R49” [7:1] 11 = +20% from the setting in “Register R49” [7:1]
3:2	RWPE	00	R4A [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Undervoltage-Lockout Status 00 = –10% from the setting in “Register R49” [7:1] 01 = –12.5% from the setting in “Register R49” [7:1] 10 = –7.5% from the setting in “Register R49” [7:1] 11 = –20% from the setting in “Register R49” [7:1]
1:0	RWPE	11	R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 97. SWC Voltage Setting

Address: 0x4B **Description:** SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R4B [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting 000 0000 = 1500 mV 000 0001 = 1505 mV 000 0010 = 1510 mV ... 011 1100 = 1800 mV ... 111 1101 = 2125 mV 111 1110 = 2130 mV 111 1111 = 2135 mV
0	RWPE	0	R4B [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power-Good Status 0 = –5% from the setting in “Register R4B” [7:1] 1 = –7.5% from the setting in “Register R4B” [7:1]

Table 98. SWC Threshold, Soft-stop Time

Address: 0x4C **Description:** SWC Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4C [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power-Good Status 00 = +5% from the setting in “Register R4B” [7:1] 01 = +7.5% from the setting in “Register R4B” [7:1] 10 = +10% from the setting in “Register R4B” [7:1] 11 = +2.5% from the setting in “Register R4B” [7:1]
5:4	RWPE	10	R4C [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Overvoltage Status 00 =+7.5% from the setting in “Register R4B” [7:1] 01 = +10% from the setting in “Register R4B” [7:1] 10 = +12.5% from the setting in “Register R4B” [7:1] 11 = +20% from the setting in “Register R4B” [7:1]
3:2	RWPE	00	R4C [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register R4B” [7:1] 01 = –12.5% from the setting in “Register R4B” [7:1] 10 = –7.5% from the setting in “Register R4B” [7:1] 11 = –20% from the setting in “Register R4B” [7:1]
1:0	RWPE	11	R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

Table 99. SW[A] FSW and Mode

Address: 0x4D **Description:** SW[A] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4D [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4D [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:0	RV	0	R4D [3:0]: Reserved

Table 100. SW[B:C] FSW and Mode

Address: 0x4E **Description:** SW[B:C] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4E [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4E [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RWPE	10	R4E [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	00	R4E [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

Table 101. Single_Dual Mode

Address: 0x4F **Description:** Single_Dual Mode			
Bits	**Attribute**	**Default**	**Description**
7:1	RV	0	R4F [7:1]: Reserved
0	RWPE	0	R4F [0]: SWA_SWB_PHASE_MODE_SELECT Switch Node A and Switch Node B Phase Regulator Mode Selection. 0 = Single Phase Regulator Mode 1 = Dual Phase Regulator Mode

Table 102. SW[A:C] Current Limited Warning Threshold

Address: 0x50 **Description:** SW[A:C] Current Limited Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	11	R50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_THRESHOLD_SETTING Switch Node A Output Current Limiter Threshold Setting High Current PMIC Encoding Definition For COT Mode, Ivalley_limit: 00 = 4.5A 01 = 5.5A 10 = 6.5A 11 = 8.0A
5:4	RV	0	R50 [5:4]: Reserved
3:2	RWPE	11	R50 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_THRESHOLD_SETTING Switch Node B Output Current Limiter Threshold Setting High Current PMIC Encoding Definition For COT Mode, Ivalley_limit: 00 = 4.5A 01 = 5.5A 10 = 6.5A 11 = 8.0A
1:0	RWPE	11	R50 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_THRESHOLD_SETTING Switch Node C Output Current Limiter Threshold Setting High Current PMIC Encoding Definition For COT Mode, Ivalley_limit: 00 = 1.5A 01 = 2.0A 10 = 2.5A 11 = 3A

Table 103. Voltage Setting for VLDO_1.8V & VLDO_1.0V

Address: 0x51 **Description:** Voltage Setting for VLDO_1.8V & VLDO_1.0V			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R51 [7:6]: VLDO_1.8V_VOLTAGE_SETTING VLDO_1.8V LDO Output Voltage Setting 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5:3	RV	0	R51 [5:3]: Reserved
2:1	RWPE	01	R51 [2:1]: VLDO_1.0V_VOLTAGE_SETTING VLDO_1.0V LDO Voltage Setting 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	R51 [0]: Reserved

Table 104. Reserved R52 – R57

Address: 0x52 – 0x57 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R52 [7:0] – R57 [7:0]: Reserved

Table 105. Power-Off Sequence Configuration 0

Address: 0x58 **Description:** Power-Off Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R58 [7]: POWER_OFF_SEQUENCE_CONFIG0 PMIC Power-Off Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	1	R58 [6]: POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R58 [5]: Reserved
4	RWPE	1	R58 [4]: POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R58 [3]: POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	R58 [2:0]: POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power-Off Sequence Config0 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

Table 106. Power-Off Sequence Configuration 1

Address: 0x59 **Description:** Power-Off Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R59 [7]: POWER_OFF_SEQUENCE_CONFIG1 PMIC Power-Off Sequence Config1 0 = Do Not Execute Config1 1 = Execute Config1
6	RWPE	1	R59 [6]: POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R59 [5]: Reserved
4	RWPE	1	R59 [4]: POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	1	R59 [3]: POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	R59 [2:0]: POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power-Off Sequence Config1 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

Table 107. Power-Off Sequence Configuration 2

Address: 0x5A **Description:** Power-Off Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R5A [7]: POWER_OFF_SEQUENCE_CONFIG2 PMIC Power-Off Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	R5A [6]: POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R5A [5]: Reserved
4	RWPE	0	R5A [4]: POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R5A [3]: POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R5A [2:0]: POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power-Off Sequence Config2 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

Table 108. Reserved

Address: 0x5B **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5B [7:0]: Reserved

Table 109. Reserved

Address: 0x5C **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5C [7:0]: Reserved

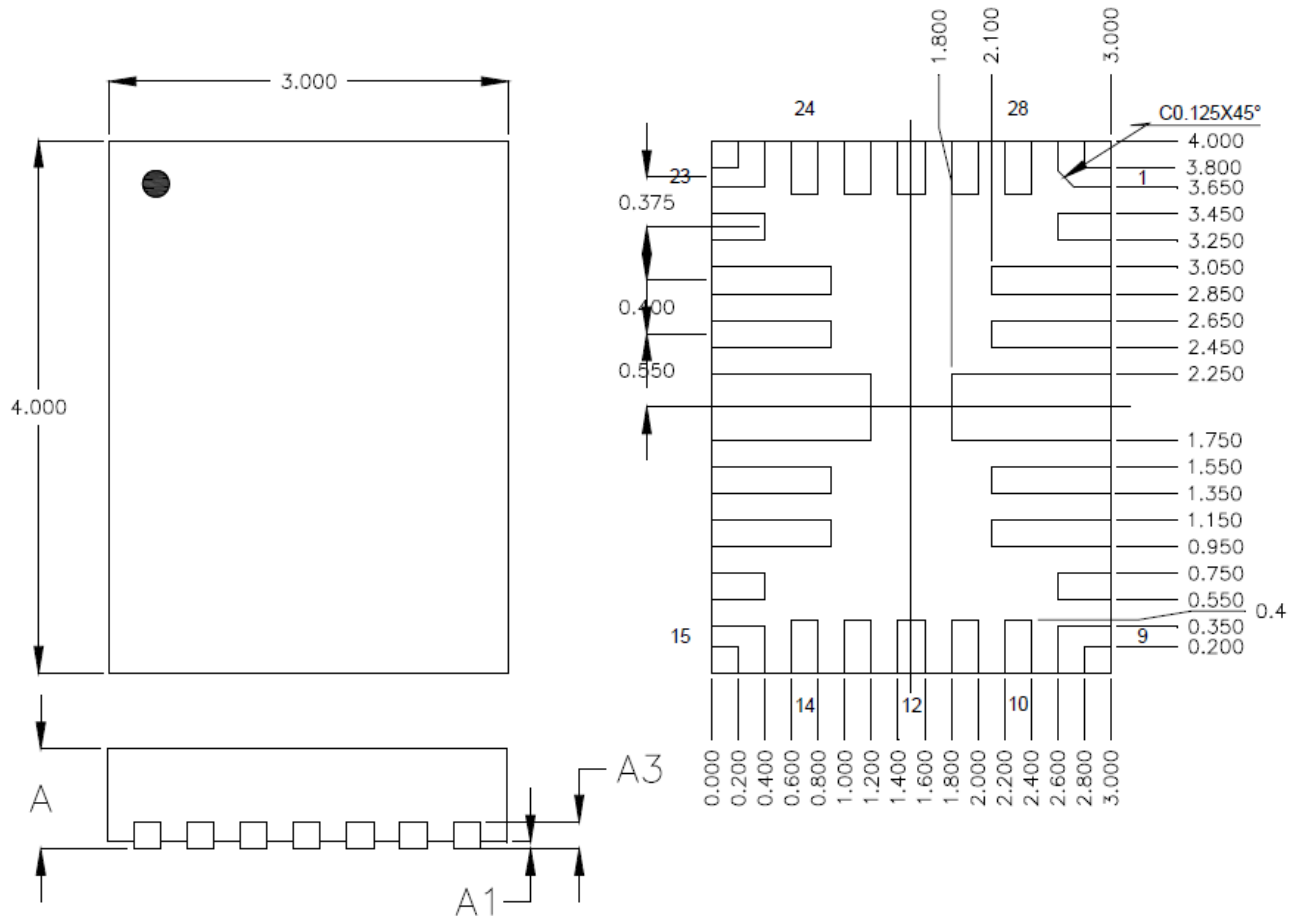
Table 110. SW[A] Soft-Start Time

Address: 0x5D **Description:** SW[A] Soft-Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5D [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
4:0	RV	0	R5D [4:0]: Reserved

Table 111. SW[B:C] Soft-Start Time

Address: 0x5E **Description:** SW[B:C] Soft-Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5E [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
4	RV	0	R5E [4]: Reserved
3:1	RWPE	001	R5E [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
0	RV	0	R5E [0]: Reserved

18 Outline Dimension

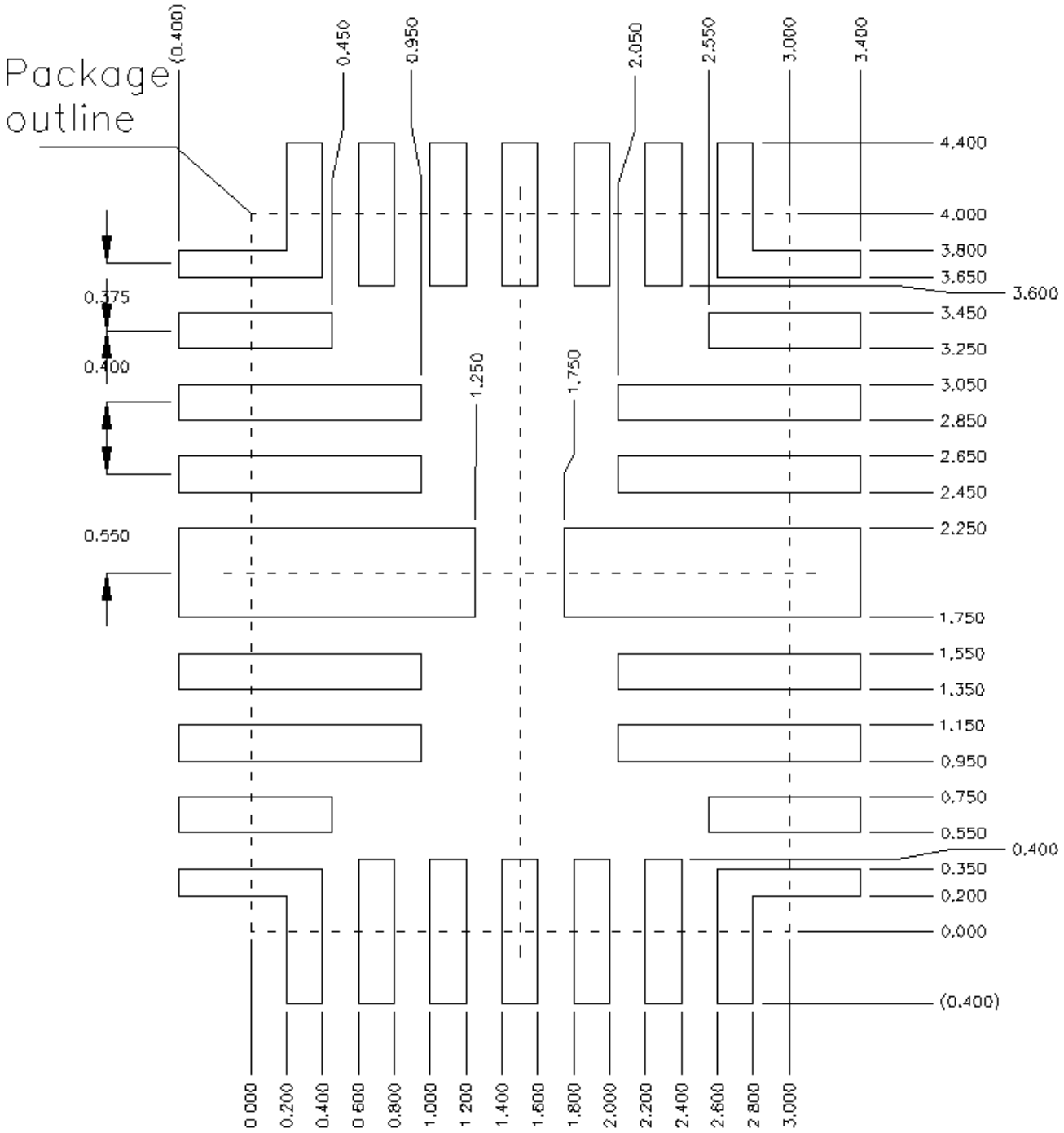


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

W-Type 28L QFN 3x4 (FC) Package

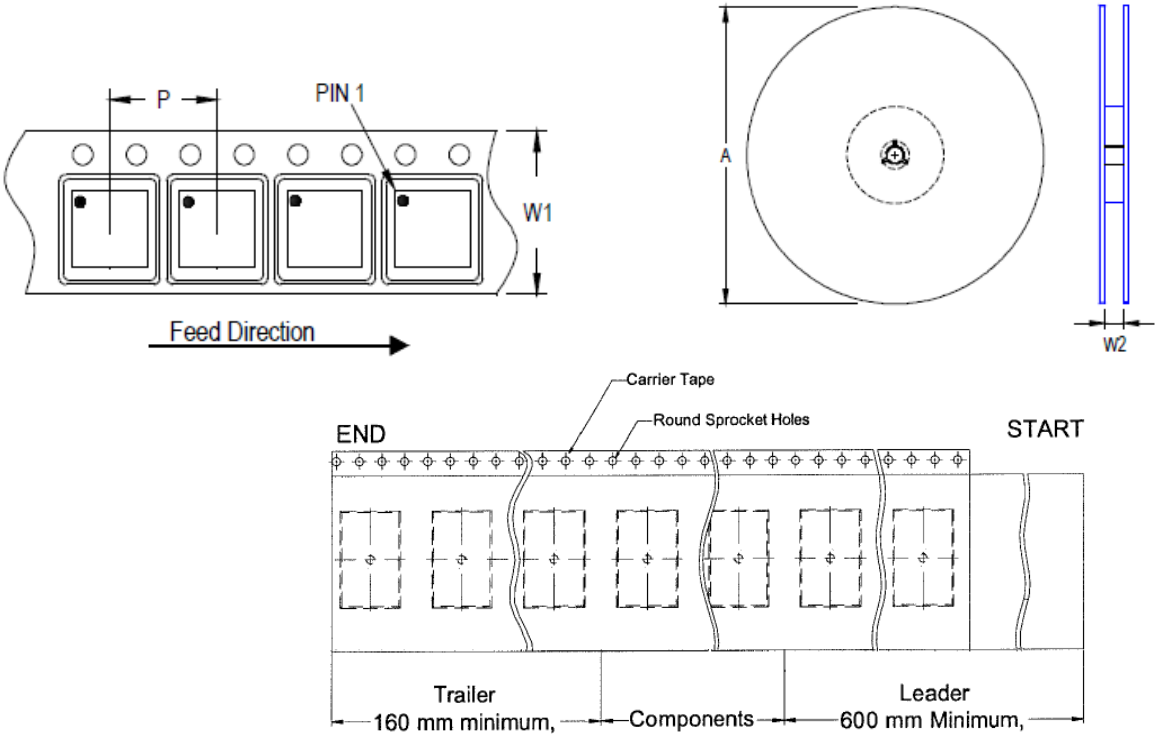
19 Footprint Information



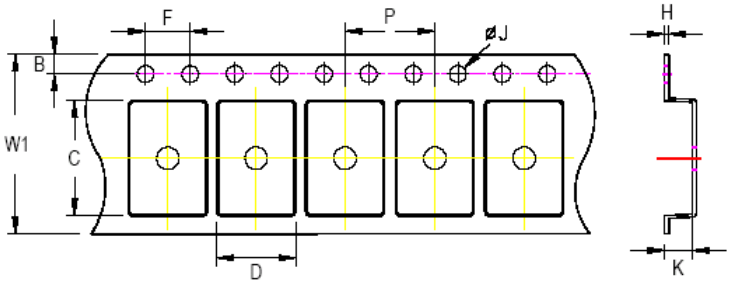
Package	Number of Pin	Tolerance
V/W/U/XQFN3x4-28(FC)	28	±0.05

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
00	2026/3/13	First Edition