RICHTEK® **RTQ5760T**

6V, 1A, ACOT® Buck Converter

1 General Description

The RTQ5760T is a simple, easy-to-use, 1A synchronous step-down converter with an input supply voltage range from 2.5V to 6V. The device builds in an accurate 0.6V reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in a SOT-563 (FC) package.

The RTQ5760T adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate with nearly constant switching frequency over the line, load, and output voltage range. The RTQ5760T operates in automatic PSM that maintains high efficiency during light load operation.

The RTQ5760T senses both MOSFETs current for a robust overcurrent protection. The device features cycle-by-cycle current-limit protection and prevents the device from the catastrophic damage in output short circuit, overcurrent, or inductor saturation. A built-in soft-start function prevents inrush current during start-up. The device also includes input undervoltage-lockout, output undervoltage protection, and over-temperature protection to provide safe and smooth operation in all operating conditions. The recommended junction temperature range is –40°C to 125°C.

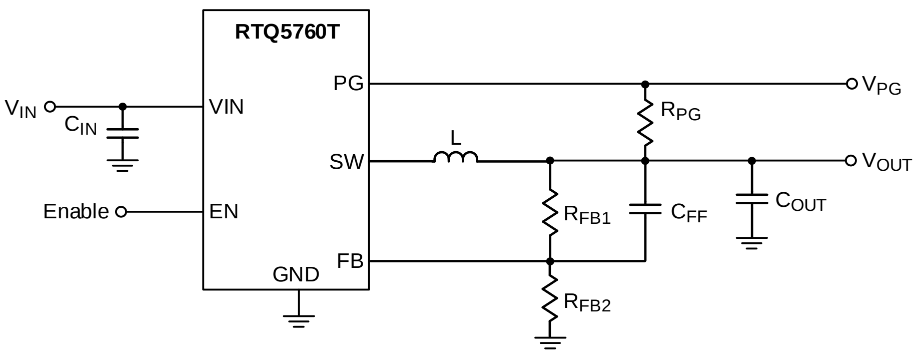
2 Features

- **Input Voltage Range from 2.5V to 6V**
- **Integrated 120mΩ and 80mΩ MOSFETs**
- **1A Output Current, up to 95% Efficiency**
- **100% Duty Cycle for Lowest Dropout**
- **1% Internal Reference Voltage**
- **2.2MHz Typical Switching Frequency**
- **Power Saving Mode for Light Loads**
- **Low Quiescent Current: 25μA (Typical)**
- **Fast Advanced Constant On-Time (ACOT®) Control**
- **Internal Soft Startup (0.6ms)**
- **Enable Control Input**
- **Power-Good Indicator**
- **Both MOSFETs Overcurrent Protection**
- **Input Undervoltage-Lockout Protection**
- **Hiccup-Mode Output Undervoltage Protection**
- **Over-Temperature Protection**

3 Applications

- Mobile Phones and Handheld Devices
- Set-Top Boxes, Cable Modems, and xDSL Platforms
- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converters

4 Simplified Application Circuit



5 Ordering Information

RTQ5760T □-□□

Packing
A: Standard

Product Grade
T: Industrial

Package Type(1)
D: SOT-563 (FC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

0SW

0S: Product Code
W: Date Code

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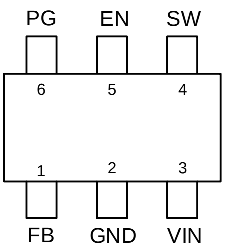
RICHTEK

7 Pin Configuration

(TOP VIEW)

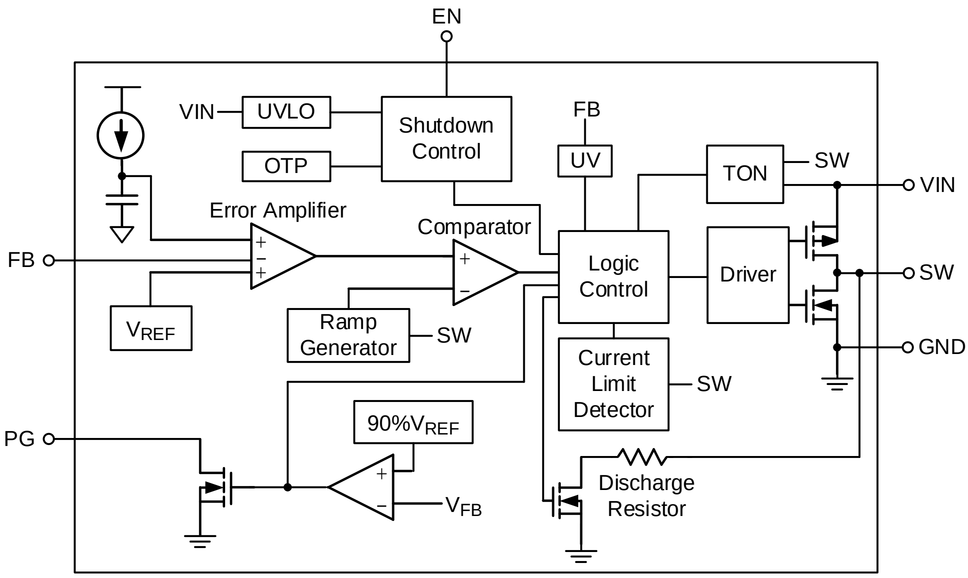


SOT-563 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at the Feedback Reference Voltage, typically 0.6V.
2	GND	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
3	VIN	Power input. The input voltage range is from 2.5V to 6V. Connect input capacitors directly to this pin and GND pins. MLCC with capacitance higher than 10μF is recommended.
4	SW	This pin is the switch node connected to the internal switch. Connect this pin to the inductor.
5	EN	Enable control input. Connecting this pin to logic high enables the device, and connecting this pin to GND disables the device. Do not leave this pin floating.
6	PG	Power-good indicator. The output of this pin is an open-drain with external pull-up resistor. After soft-startup, PG is pulled up when the FB voltage is within 90% (typical). The PG status is low while EN is disabled.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN -- –0.3V to 6.5V
- Switch Voltage, SW -- –0.3V to 6.5V
  < 50ns -- –2.5V to 9V
- Other Pins -- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-563 (FC) --- 1W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature --- 150°C
- Storage Temperature Range --- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
- HBM (Human Body Model) -- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage --- 2.5V to 6V
- Output Voltage -- 0.6V to V_{IN}
- Junction Temperature Range -- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		SOT-563 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	109.4	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	7.3	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	18.1	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	100	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	13	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$ and $\Psi_{JC(TOP)}$ are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 3.6V. T_J = T_A = –40°C to 85°C. Typical value is tested at T_A = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Voltage	V_{IN}		2.5	--	6	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	2.15	2.3	2.47	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}		160	300	440	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_A = 25°C	--	0.3	1	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.63V	--	25	35	μA
Soft-Start						
Soft-Start Time	t_{SS}	10%V_{OUT} to 90%V_{OUT}	--	0.6	--	ms
Enable Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}	EN high-level input voltage	0.6	0.82	0.95	V
EN Input Voltage Falling Threshold	V_{EN_F}	EN low-level input voltage	0.5	0.76	0.9	V
Feedback Voltage and Discharge Resistance						
Feedback Voltage	V_{FB}		594	600	606	mV
FB Pin Current	I_{FB}	V_{FB} = 0.6V, T_A = 25°C	–0.1	0	0.1	μA
Internal MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	120	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	80	--	mΩ
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	V_{IN} = 3.6V, V_{OUT} = 1.2V L = 1μH, T_A = 25°C	1.85	2.65	3.45	A
Low-Side Switch Current Limit	I_{LIM_L}	V_{IN} = 3.6V, V_{OUT} = 1.2V L = 1μH, T_A = 25°C	1.05	1.55	2.05	A
Switching Frequency						
Switching Frequency	f_{SW}		1.76	2.2	2.64	MHz
On-Time Timer Control						
Minimum Off-Time	t_{OFF_MIN}		50	80	110	ns
Hiccup-Mode Output Undervoltage Protection						
UVP Trip Threshold	V_{UVP}	Hiccup detect	43	50	57	%
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	30	--	°C
Power-Good Function						
Power-Good High Threshold	V_{TH_PGLH}	V_{FB} rising, PG goes high	80	90	94	%
Power-Good High Hysteresis	ΔV_{TH_PGLH}	V_{FB} falling, PG goes low	1	5	10	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good Falling Delay Time			36	60	96	μs
Output Discharge Resistor						
Discharge Resistor	R_{DISCHG}		100	150	200	Ω

15 Typical Application Circuit

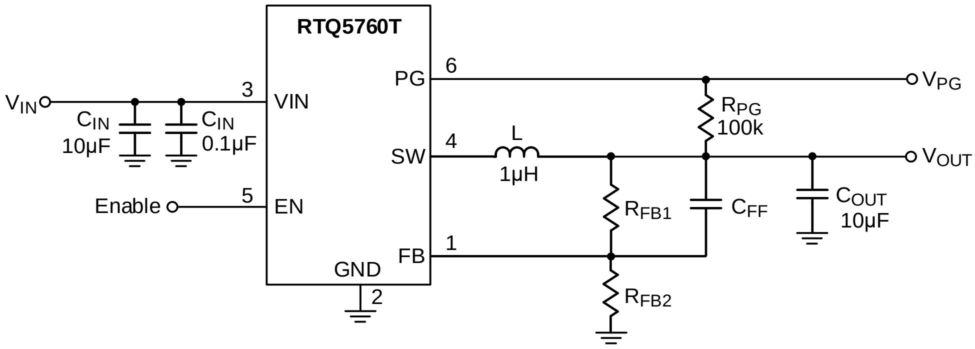


Table 1. Suggested Component Values

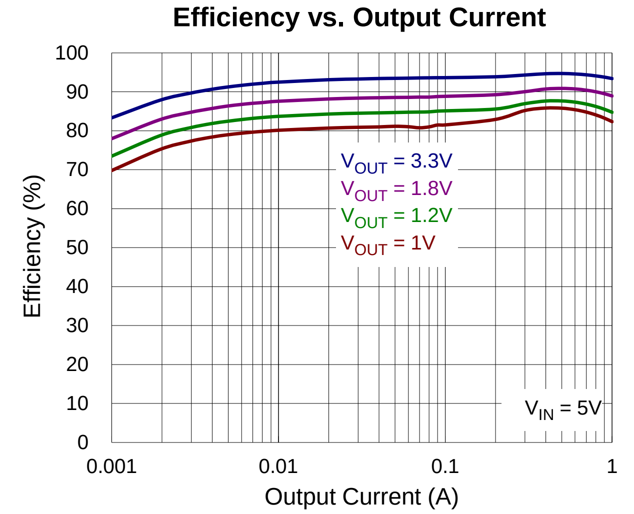
V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	L (µH)	C_{FF} (pF)
3.3	45	10	1	--
1.8	20	10	1	--
1.5	15	10	1	--
1.2	10	10	1	--
1.05	7.5	10	1	--
1	6.65	10	1	--

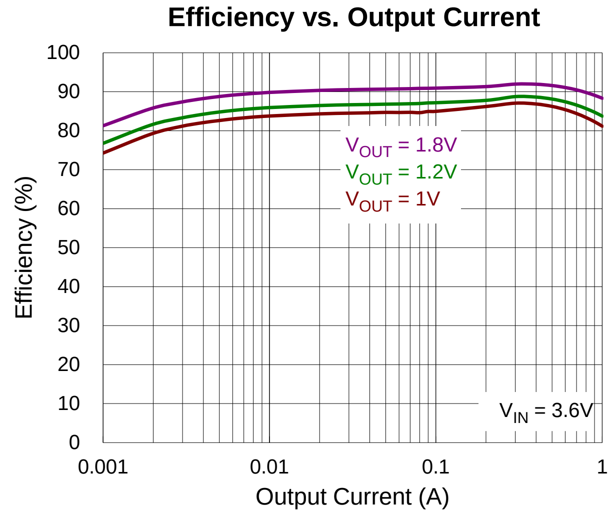
Table 2. Recommended External Components

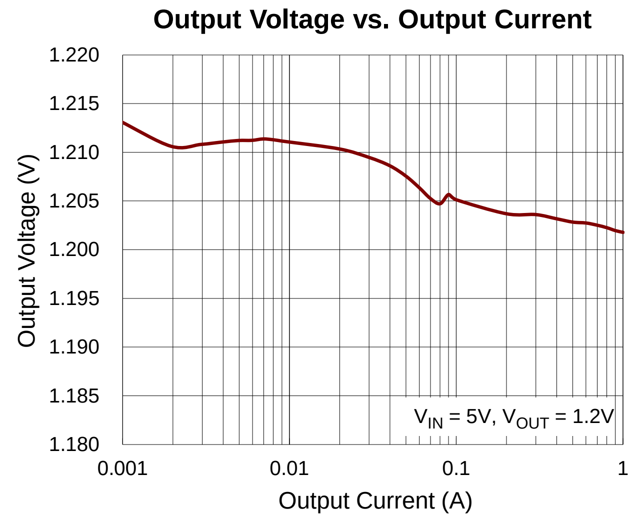
Component	Description	Vendor P/N
C_{IN}	10µF, 6.3V, X5R, 0603	0603X106M6R3 (WALSIN) GRM188R60J106ME84 (MURATA)
C_{OUT} (Note 7)	10µF, 6.3V, X5R, 0603	0603X106M6R3 (WALSIN) GRM188R60J106ME84 (MURATA)
L	1µH	DFE252010F-1R0M (MURATA) HMLQ25201T-1R0MSR (CYNTEC)

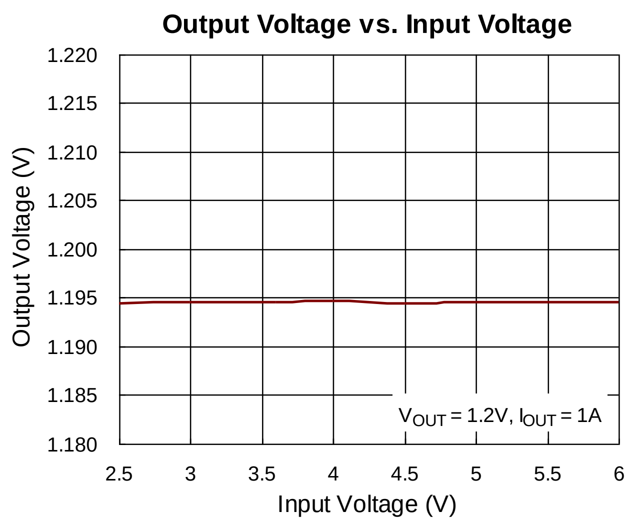
Note 7. Considering the effective capacitance de-rated with biased voltage level and size, the C_{OUT} component needs to satisfy the effective capacitance at least 4µF for V_{OUT} = 3.3V and 7µF for V_{OUT} < 3.3V for stable and normal operation.

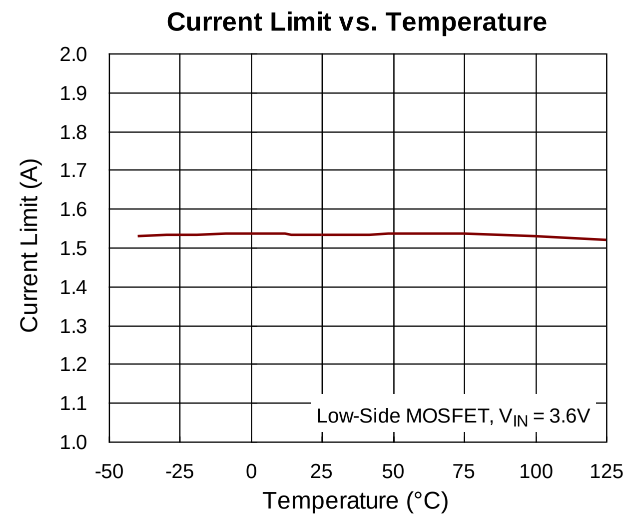
16 Typical Operating Characteristic

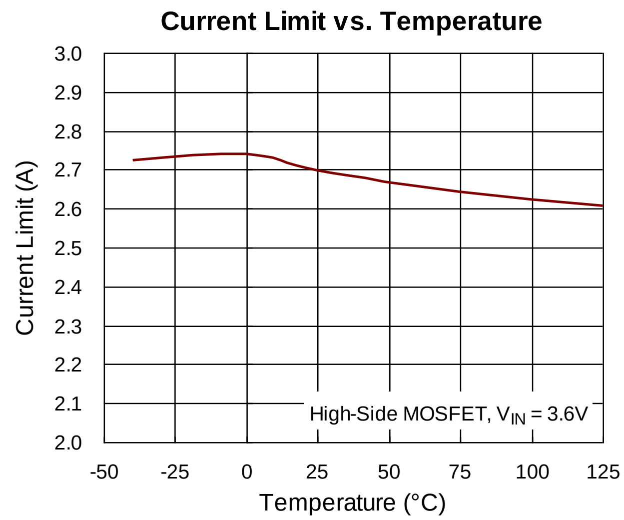


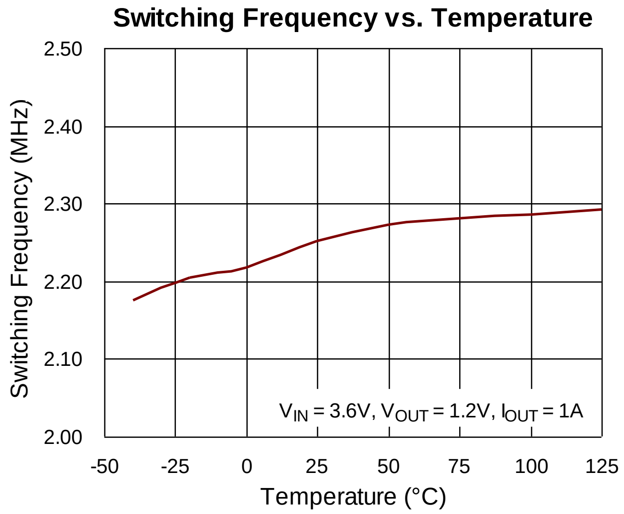


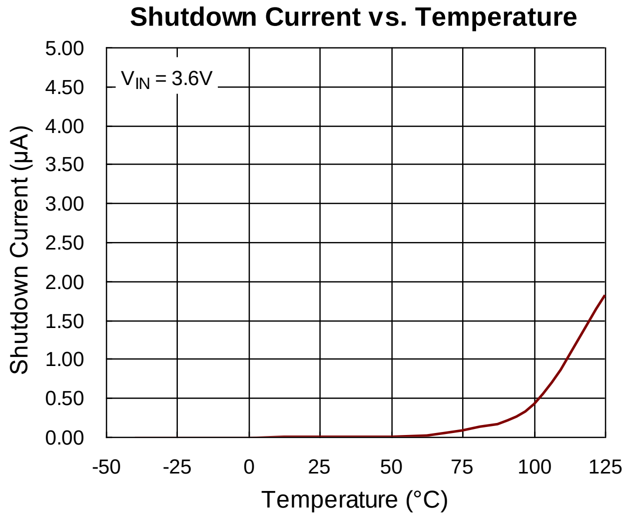


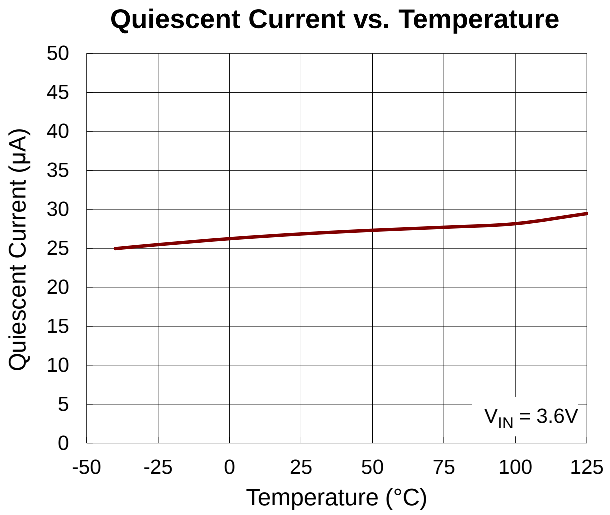


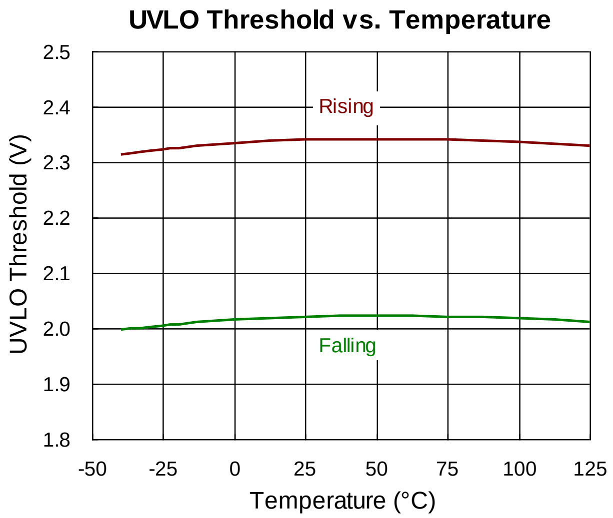


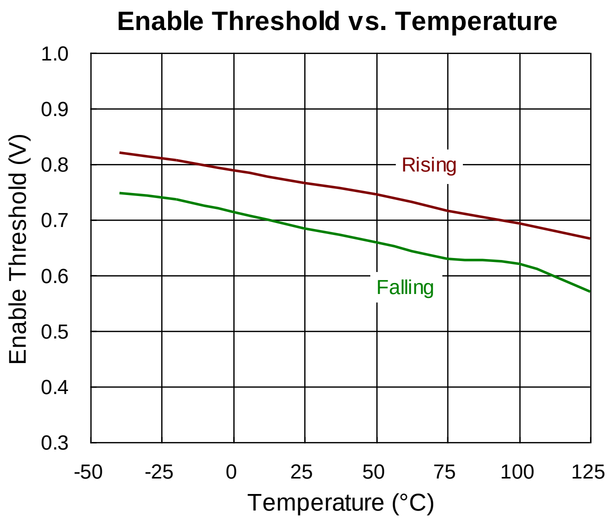


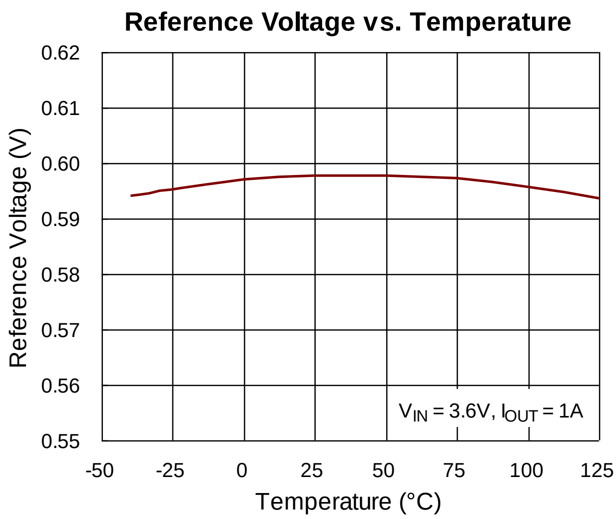

Switching Frequency vs. Temperature
Switching Frequency (MHz)
Temperature (°C)
VIN = 3.6V, VOUT = 1.2V, IOUT = 1A


Shutdown Current vs. Temperature
Shutdown Current (μA)
Temperature (°C)
VIN = 3.6V

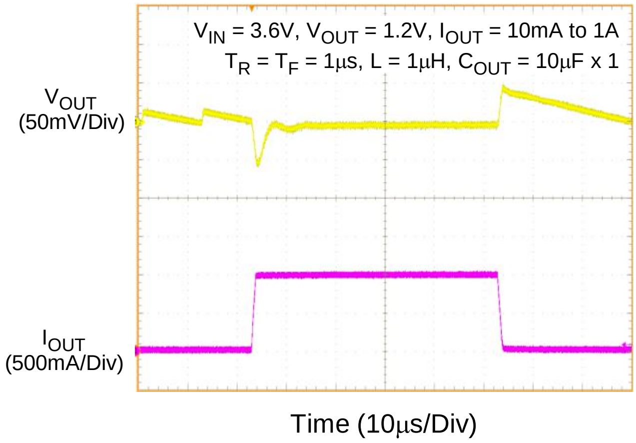

Quiescent Current vs. Temperature
Quiescent Current (μA)
Temperature (°C)
VIN = 3.6V


UVLO Threshold vs. Temperature
UVLO Threshold (V)
Temperature (°C)
Rising
Falling


Enable Threshold vs. Temperature
Enable Threshold (V)
Temperature (°C)
Rising
Falling


Reference Voltage vs. Temperature
Reference Voltage (V)
Temperature (°C)
VIN = 3.6V, IOUT = 1A

Load Transient Response



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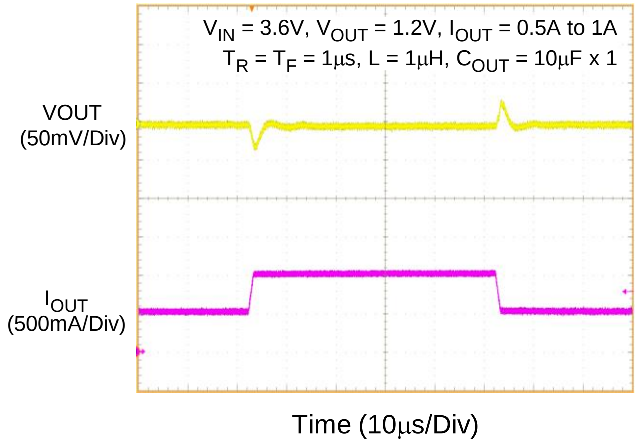
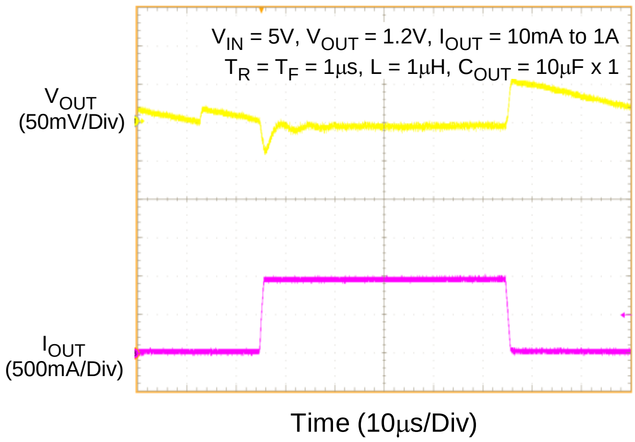
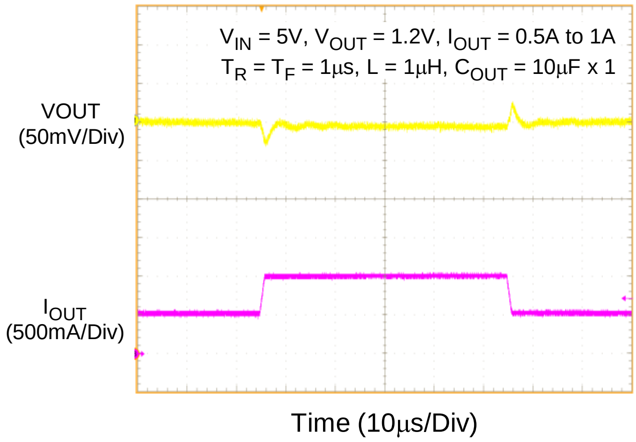


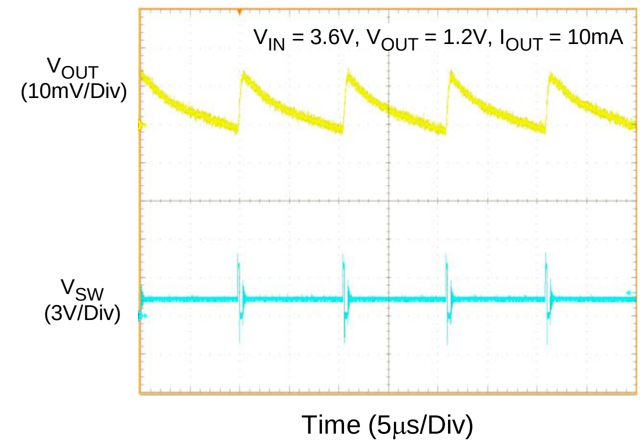
Load Transient Response



Load Transient Response



Output Ripple Voltage



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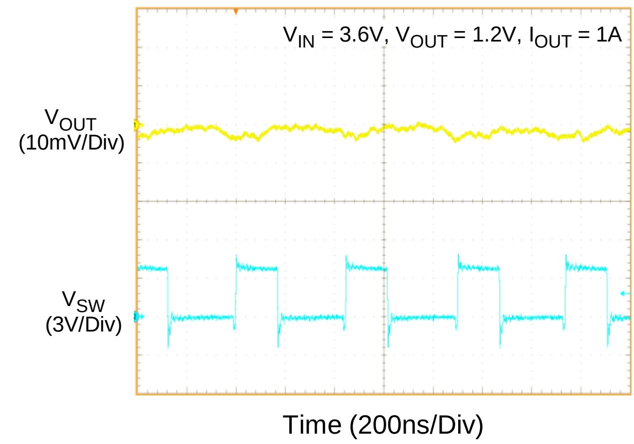

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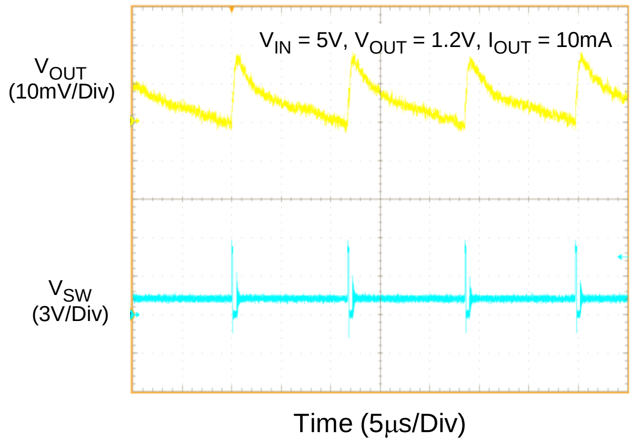
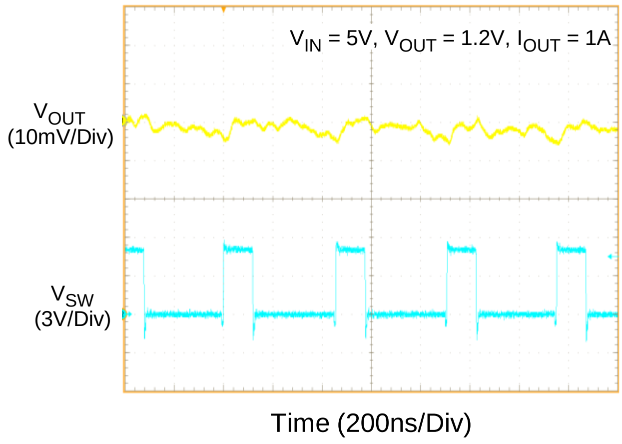
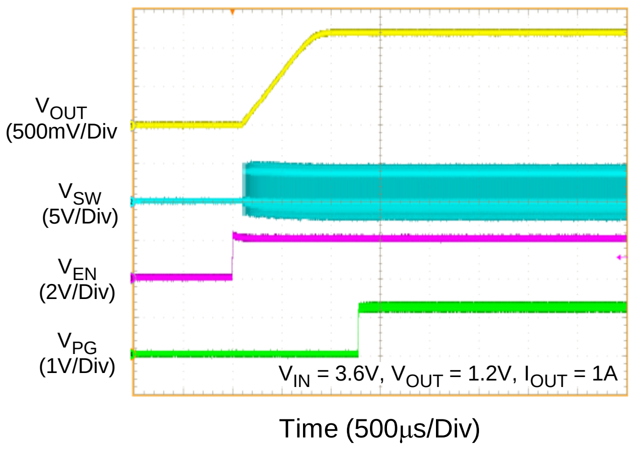


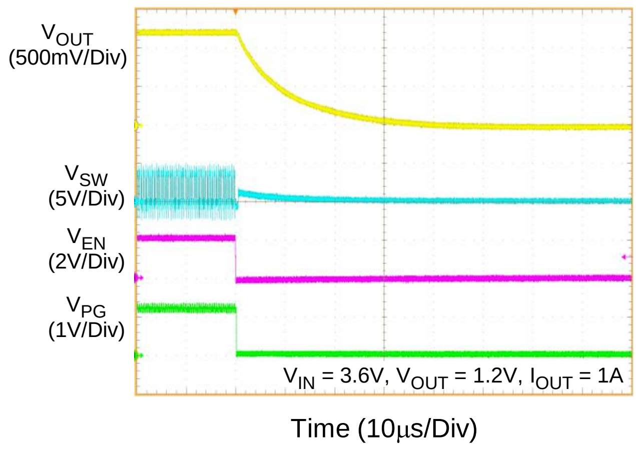
Output Ripple Voltage



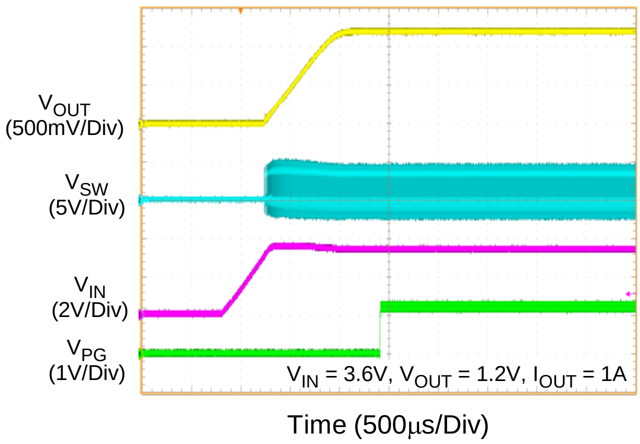
Power On from EN



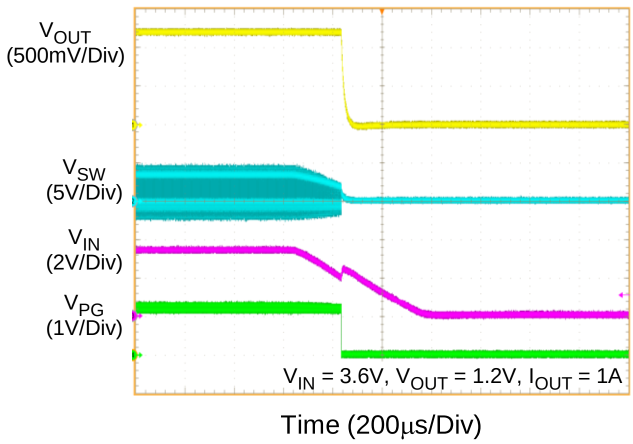
Power Off from EN



Power On from VIN



Power Off from VIN



17 Operation

The RTQ5760T is a high-efficiency, synchronous step-down converter that can deliver up to 1A output current from a 2.5V to 6V input supply.

17.1 Advanced Constant On-Time Control and PWM Operation

The RTQ5760T adopts ACOT® control for its ultrafast transient response, low external component count and stability with low ESR MLCC output capacitors. When the feedback voltage falls below the feedback reference voltage, the minimum off-time one-shot (80ns, typical) has timed out and the inductor current is below the current-limit threshold, then the internal on-time one-shot circuitry is triggered, and the high-side switch is turned on. Since the minimum off-time is short, the device exhibits an ultrafast transient response and enables the use of smaller output capacitance.

The on-time is inversely proportional to input voltage and directly proportional to output voltage to achieve pseudo-fixed frequency over the input voltage range. After the on-time one-shot timer expires, the high-side switch is turned off, and the low-side switch is turned on until the on-time one-shot is triggered again. In the steady state, the error amplifier compares the feedback voltage V_{FB} and an internal reference voltage. If the virtual inductor current ramp voltage is lower than the output of the error amplifier, a new pre-determined fixed on-time will be triggered by the on-time one-shot generator.

17.2 Power Saving Mode

The RTQ5760T automatically enters power-saving mode (PSM) at light load to maintain high efficiency. As the load current decreases and eventually the inductor current ripple valley touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side switch is turned off when the zero inductor current is detected. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level that requires the next on-time. The switching frequency decreases and is proportional to the load current to maintain high efficiency at light load.

17.3 Enable Control

The RTQ5760T provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{EN_F}) of the enable input (EN), the converter will disable output voltage, that is, the converter is disabled, and switching is inhibited even if the VIN voltage is above VIN undervoltage-lockout rising threshold (V_{UVLO_R}). During shutdown mode, the supply current can be reduced to I_{SHDN} (1μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{EN_R}) while the VIN voltage is higher than the UVLO threshold, the device will be turned on, that is, the switching is enabled and the soft-start sequence is initiated. Do not leave this pin floating.

17.4 Soft-Start (SS)

The RTQ5760T provides an internal soft-start feature for inrush control. At power-up, the internal capacitor is charged by an internal current source to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth start-up from a pre-biased output. The output voltage starts to rise in 0.1ms from EN rising, and the soft-start ramp-up time (10%V_{OUT} to 90%V_{OUT}) is 0.6ms.

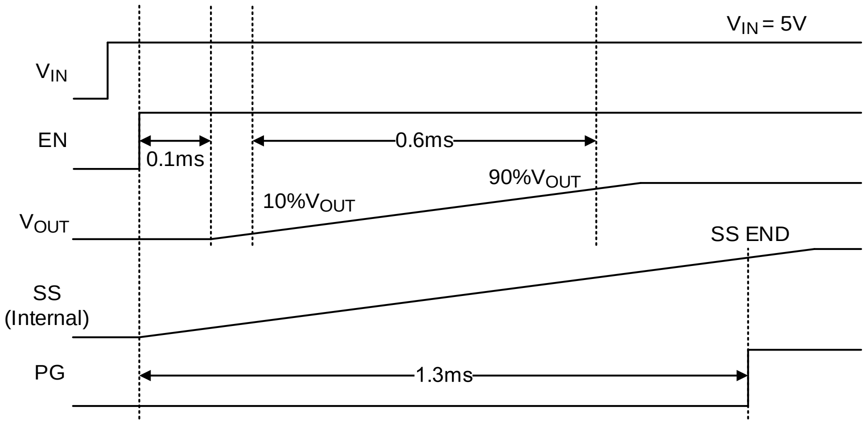


Figure 1. Start-Up Sequence

17.5 Maximum Duty Cycle Operation

The RTQ5760T is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off time becomes smaller than minimum off time, the RTQ5760T starts to enable the skip off time function and keeps the high-side MOSFET switch on continuously. The RTQ5760T implements the skip off time function to achieve a high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

17.6 Power-Good Indication

The RTQ5760T features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of the comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to VOUT or an external voltage below 6V. When VIN voltage rises above V_{UVLO_R}, the power-good function is activated. After soft-start is finished, the PG pin is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (V_{TH_PGLH}) (typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high. When V_{FB} falls short of the power-good low threshold (V_{TH_PGHL}) (typically 85% of the reference voltage), the PG pin will be pulled low after a certain delay (typically 60μs) elapsed. Once started up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull-down device (typically 10Ω) will pull the PG pin low. The power-good indication profile is shown below.

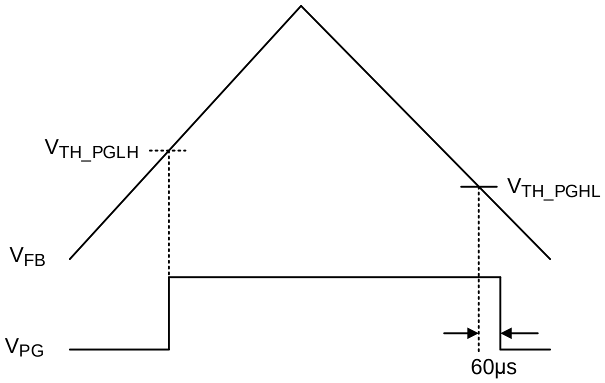


Figure 2. The Logic of PG

Table 3. PG Pin Status

Conditions		PG Pin
Enable	$V_{EN} > V_{EN\_R}$, $V_{FB} > V_{TH\_PGLH}$	High Impedance
	$V_{EN} > V_{EN\_R}$, $V_{FB} < V_{TH\_PGHL}$	Low
Shutdown	$V_{EN} < V_{EN\_F}$	Low
OTP	$T_J > T_{OTP}$	Low

17.7 Input Undervoltage-Lockout

In addition to the EN pin, the RTQ5760T also provides enable control through the VIN pin. If V_{EN} rises above V_{EN_R} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO_R}. This is to ensure that the internal regulator is ready, preventing operation with not-fully-enhanced internal MOSFET switches. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage (V_{UVLO_R} – V_{UVLO_HYS}), the switching will be inhibited. If VIN rises above the UVLO rising threshold (V_{UVLO_R}), the device will resume normal operation with a complete soft-start.

17.8 Overcurrent Protection

The RTQ5760T features cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs and prevents catastrophic damage in output short circuit, overcurrent, or inductor saturation.

The high-side MOSFET overcurrent protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch peak-current limit (I_{LIM_H}) after a certain delay when the high-side switch is turned on each cycle. If an overcurrent condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current exceeding the high-side current limit.

The low-side MOSFET overcurrent protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output undervoltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Overcurrent Protection

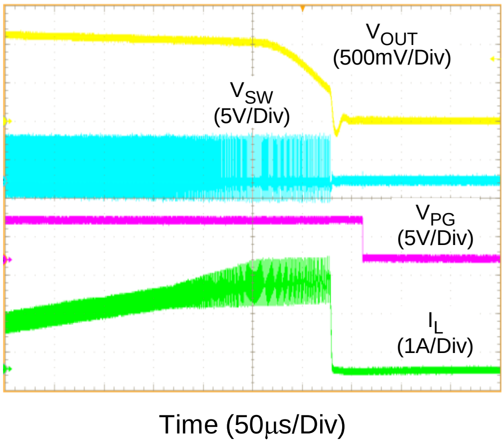


Figure 3. Overcurrent Protection

17.9 Output Active Discharge

When the RTQ5760T is disabled by the EN pin, UVLO or OTP, the device discharges the output capacitors (via SW pins) through an internal discharge resistor (150Ω) connected to ground. This function prevents the reverse current flow from the output capacitors to the input capacitors once the input voltage collapses. It does not need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is removed.

17.10 Hiccup-Mode Output Undervoltage Protection

The RTQ5760T includes output undervoltage protection (UVP) against over-load or short-circuited conditions by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold (typically 50% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches. The RTQ5760T will enter output undervoltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF} (2.4ms), and then attempt to recover automatically for t_{HICCUP_ON} (1.2ms). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such a cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the overload or short-circuit condition is removed. A short-circuit protection and recovery profile is shown below.

Short-Circuit Protection and Recovery

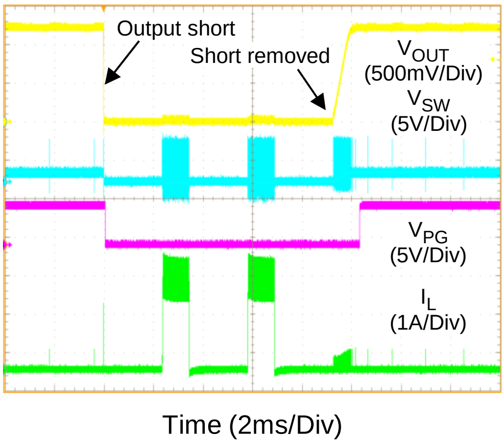


Figure 4. Short-Circuit Protection and Recovery

17.11 Over-Temperature Protection

The RTQ5760T includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds an over-temperature protection threshold (T_{OTP}). Once the junction temperature cools down by an over-temperature protection hysteresis (T_{OTP_HYS}), the IC will resume normal operation with a complete soft-start.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18 Application Information

(Note 8)

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which store and deliver energy to the load, and form a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

18.1 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is to choose the peak-to-peak ripple current to be equal to 20% to 50% of the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

$I_{L(PEAK)}$ should not exceed the minimum value of the high-side switch current limit. Besides, the current flowing through the inductor is the inductor ripple current plus the output current. During power-up, fault conditions, or transient load changes, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Considering Typical Application Circuit for 1.2V output at 1A and an input voltage of 5V, using an inductor ripple of 0.4A (40% of the IC rated current), the calculated inductance value is:

$$L = \frac{1.2 \times (5 - 1.2)}{5 \times 2.2\text{MHz} \times 0.4\text{A}} = 1\mu\text{H}$$

For typical applications, a standard inductance value of 1μH can be selected.

$$\Delta I_L = \frac{1.2 \times (5 - 1.2)}{5 \times 2.2\text{MHz} \times 1\mu\text{H}} = 0.41\text{A (41\% of the IC rated current)}$$

$$\text{and } I_{L(PEAK)} = 1\text{A} + \frac{0.41\text{A}}{2} = 1.205\text{A}$$

For the 1μH value, the inductor's saturation and thermal rating should exceed at least 1.205A. For more conservative, the rating for the inductor saturation current must be equal to or greater than the switch current limit of the device rather than the peak inductor current.

For EMI-sensitive applications, choosing a shielded type inductor is preferred.

18.2 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to prevent large variations in the input voltage. The waveform of the C_{IN} ripple voltage and ripple current is shown in Figure 5. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \left(\frac{1-D}{C_{IN} \times f_{SW}} \right) + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, which have a very low the equivalent series resistance (ESR), the ripple caused by ESR can be ignored, and the minimum input capacitance can be estimated as equation below:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \leq 100mV$

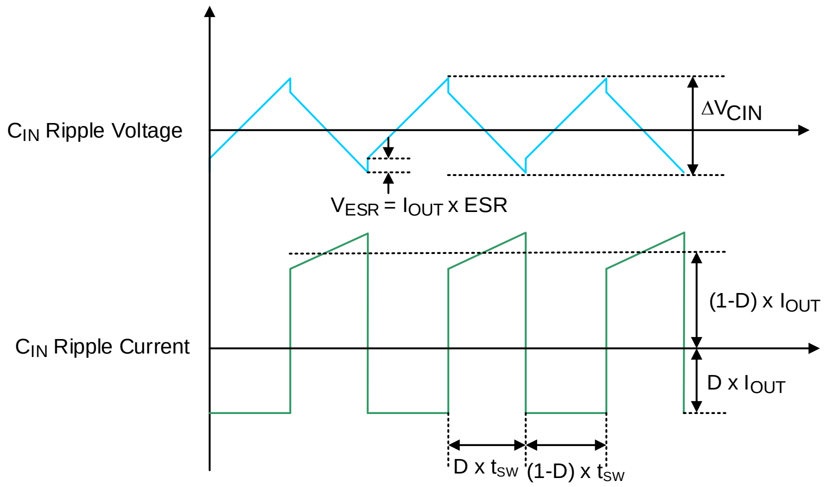


Figure 5. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worst-case $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be connected in parallel to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the RTQ5760T circuit is connected to an active supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by connecting the low ESR ceramic input capacitor in parallel with a bulk capacitor that has a higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitor of 0.1μF should be placed close to the VIN and GND pins. This capacitor should be 0402 or 0603 in size.

18.3 Output Capacitor Selection

The RTQ5760T are optimized for use with ceramic output capacitors and the best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on load apply) and soar (overshoot on load release).

18.4 Output Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple passing through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor, C_{OUT}, and its equivalent series resistance, R_{ESR}, must be taken into consideration. The output peak-to-peak ripple voltage V_{RIPPLE}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple $V_{RIPPLE(ESR)}$ and capacitive ripple $V_{RIPPLE(C)}$, can be expressed as follows:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

For the RTQ5760T's Typical Application Circuit for 1.2V output voltage, with an actual inductor current ripple (ΔI_L) of 0.41A. Taking the 10μF ceramic capacitors of GRM188R60J106ME84 from Murata as an example, the output ripple of the output capacitor is as follows:

The ripple caused by the ESR of about 5mΩ can be calculated as:

$$V_{RIPPLE(ESR)} = 0.41A \times 5m\Omega = 2.05mV$$

Due to DC bias capacitance degrading, the effective capacitance at the output voltage of 1.2V is reduced from 10μF to about 8μF.

$$V_{RIPPLE(C)} = \frac{0.41A}{8 \times 8\mu F \times 2.2MHz} = 2.91mV$$

$$V_{RIPPLE} = 2.05mV + 2.91mV = 4.96mV$$

18.5 Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick and output transients are usually small. The following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components: the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasites) and maximum duty cycle for a given input and output voltage as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Due to some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR step up or down should be taken into consideration.

18.6 Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB, as shown in Figure 6. The output voltage is set according to the following equation:

$V_{OUT} = 0.6V \times (1 + R_{FB1} / R_{FB2})$

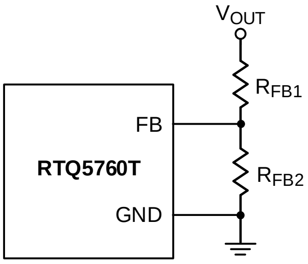


Figure 6. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. For output voltage accuracy, use divider resistors with 1% or better tolerance.

18.7 EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 7, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 0.82V).

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 8. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when VIN is smaller than the VOUT target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage-lockout threshold, as shown in Figure 9.

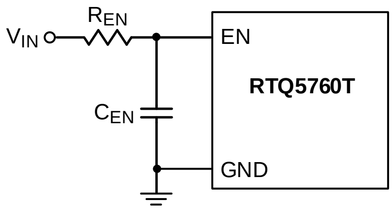


Figure 7. Enable Timing Control

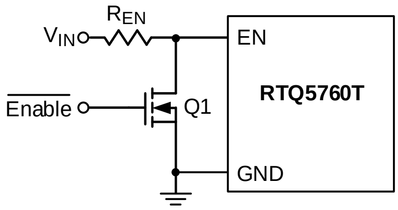


Figure 8. Logic Control for the EN Pin

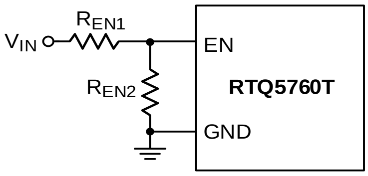


Figure 9. Resistive Divider for Undervoltage-Lockout Threshold Setting

18.8 Power-Good Output

The PG pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 6V, V_{CC}, or the output of the RTQ5760T if the output voltage is regulated under 6V. It is recommended to connect a 100kΩ between external voltage source to PG pin.

18.9 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-563 (FC) package, the thermal resistance, θ_{JA}, is 100°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (100°C/W) = 1W for a SOT-563 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

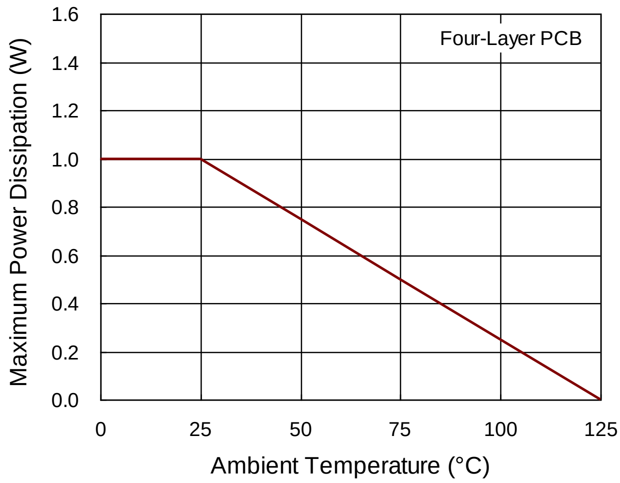


Figure 10. Derating Curve of Maximum Power Dissipation

18.10 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path comprising of the input capacitor, high-side FET, inductor, and output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RTQ5760T.
- The SW node is with high-frequency voltage swings and should be kept at a small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect the feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, design a wide and thick plane for the GND pin, or add many vias to the GND plane.

An example of a PCB layout guide is shown in Figure 11.

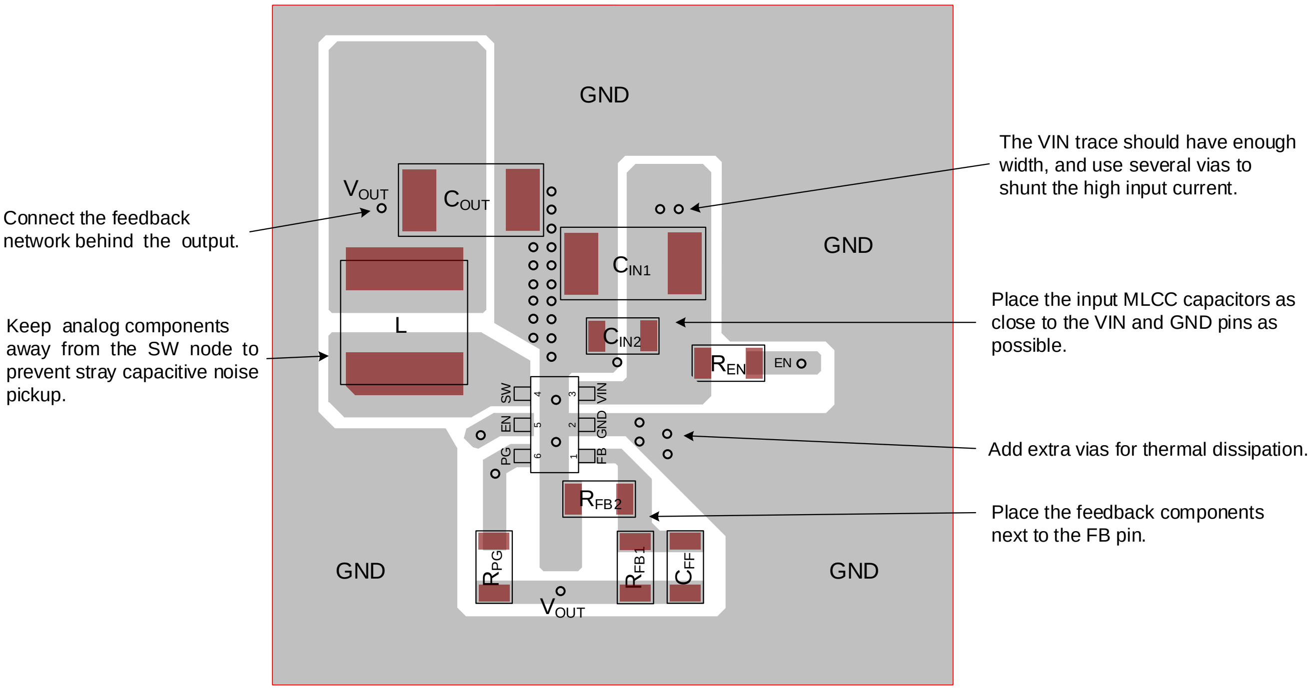
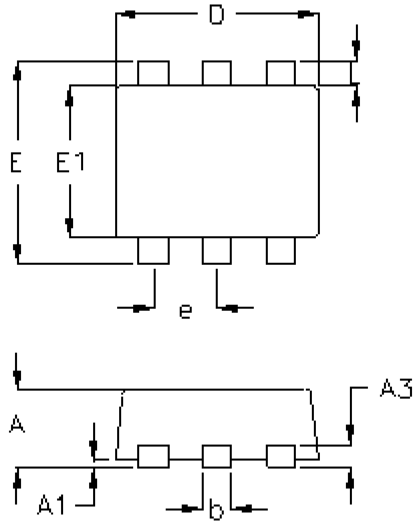


Figure 11. Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

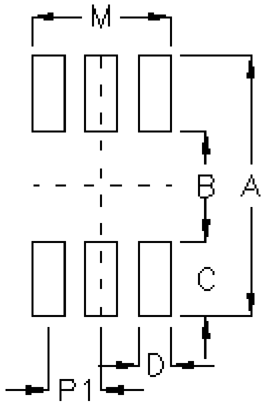
19 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.080	0.180	0.003	0.007
b	0.150	0.300	0.006	0.012
D	1.500	1.700	0.059	0.067
E	1.500	1.700	0.059	0.067
E1	1.100	1.300	0.043	0.051
e	0.500		0.020	
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016

SOT-563 (FC) Surface Mount Package

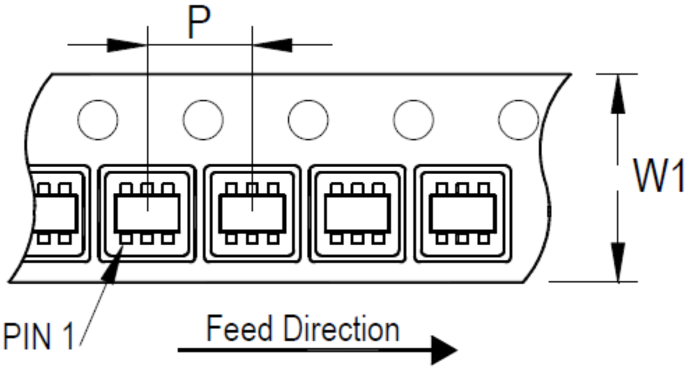
20 Footprint Information

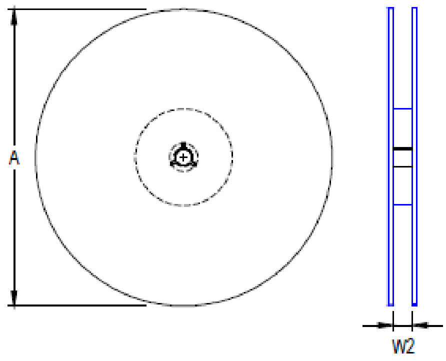


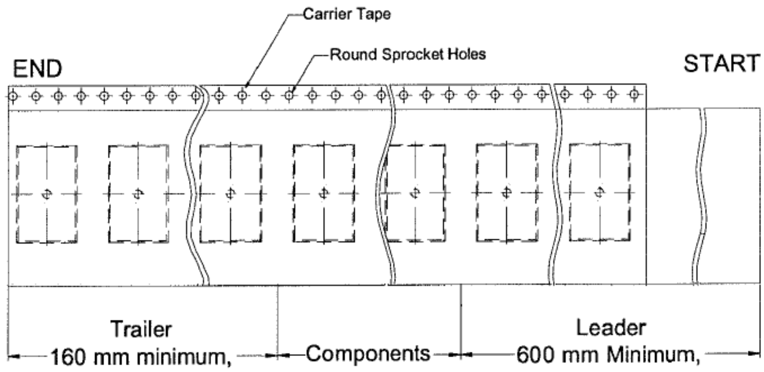
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
SOT-563(FC)	6	0.50	2.42	1.02	0.70	0.30	1.30	±0.10

21 Packing Information

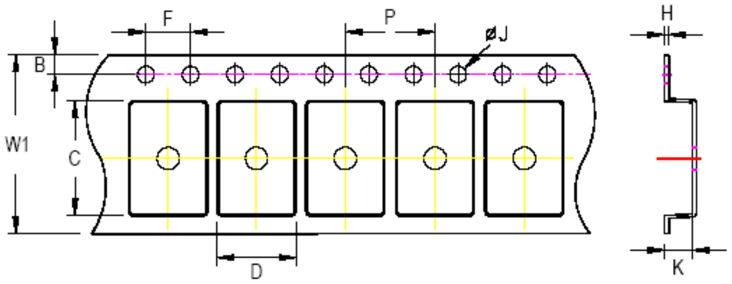
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-563	8	4	180	7	5,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.65mm	0.85mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-563	7”	5,000	Box A	3	15,000	Carton A	12	180,000
			Box E	1	5,000	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
P00	2024/10/23	First Edition	