

5.5V, 3A, 1.2MHz Synchronous Buck Converter with Soft Start and Power-Good

1 General Description

The RTQ5765A/RTQ5765B are a synchronous buck switching voltage regulator designed to operate within an input voltage range of 2.5V to 5.5V. It is capable of delivering up to 3A of output current and provides an adjustable output voltage greater than 0.6V.

The RTQ5765A/RTQ5765B utilizes the Advanced Constant On-Time (ACOT[®]) control architecture, which provides fast and stable regulation of the output voltage, making the RTQ5765A/RTQ5765B well-suited for applications with dynamic load requirements. By minimizing the external component count, the ACOT architecture simplifies the design process and reduces overall system cost, making the RTQ5765A/RTQ5765B an efficient and cost-effective solution for power management needs.

The RTQ5765A/RTQ5765B are designed to be user-friendly and suitable for a wide range of applications. It features an independent enable control input pin and a power-good indicator, allowing for easy sequence control. Additionally, to manage inrush current during start-up, the device offers a programmable soft-start feature through an external capacitor connected to the SS pin, ensuring a smooth and controlled power-up process.

Furthermore, the RTQ5765A/RTQ5765B provide comprehensive protection functions, including input undervoltage lockout, output undervoltage protection, output overvoltage protection, overcurrent protection, and over-temperature protection, enhancing system reliability and safeguarding against potential fault conditions. It incorporates cycle-by-cycle current-limit protection to safeguard against shorted outputs. The RTQ5765A/RTQ5765B are available in a compact SOT-583 (FC) package, offering flexibility in integration and space-saving advantages for various system designs.

The recommended junction temperature range and ambient temperature range are -40°C to 125°C .

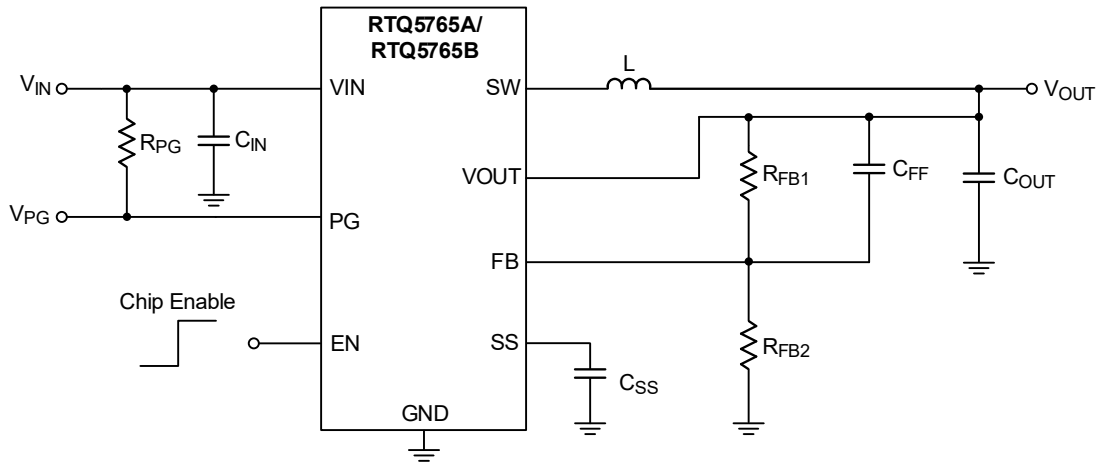
2 Features

- $\pm 1.5\%$ Output Accuracy from -40°C to 125°C Junction Temperature Range
- Soft-Start Control with External C_{ss}
- 21 μA Quiescent Current in Auto PSM/PWM Mode
- Input Voltage Range from 2.5V to 5.5V
- 65m Ω and 35m Ω Integrated Power MOSFETs
- Steady 1.2MHz Switching Frequency
- Fast Load Transient with ACOT Control Topology
- Enable and Power-Good Indicator for Sequence Control
- Operates Up to 100% Duty Cycle
- Fixed Discharge Resistor
 - RTQ5765A: 150 Ω
 - RTQ5765B: 5 Ω
- Input Undervoltage Lockout Protection (UVLO)
- Input Overvoltage Lockout Protection (OVLO)
- Output Overvoltage Protection (OVP)
- Output Undervoltage Protection (UVP)
- Short Circuit Protection with Hiccup Mode
- Over-Temperature Protection

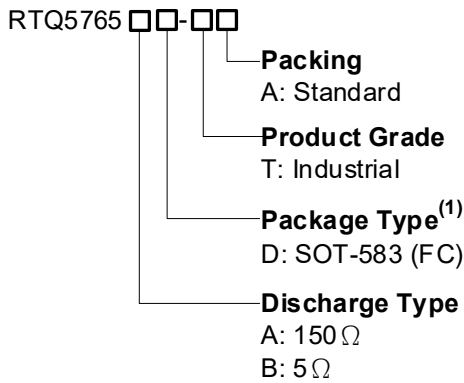
3 Application

- Wearable and Portable Electronic Devices
- DDR Memories and Solid-State Drives
- Tablets, Netbooks, Ultra-Mobile PCs
- Low-Voltage I/O System Power
- TV Stick, OTT, and Home Entertainment Devices

4 Simplified Application Circuit



5 Ordering Information

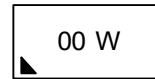


Note 1.

Richtek products are Richtek Green Policy compliant and marked with ⁽¹⁾ indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

RTQ5765AD-TA

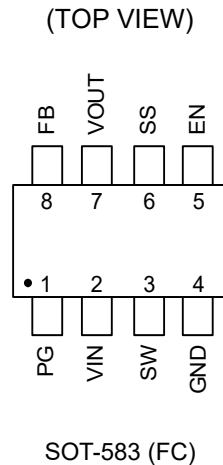


00: Product Code
W: Date Code

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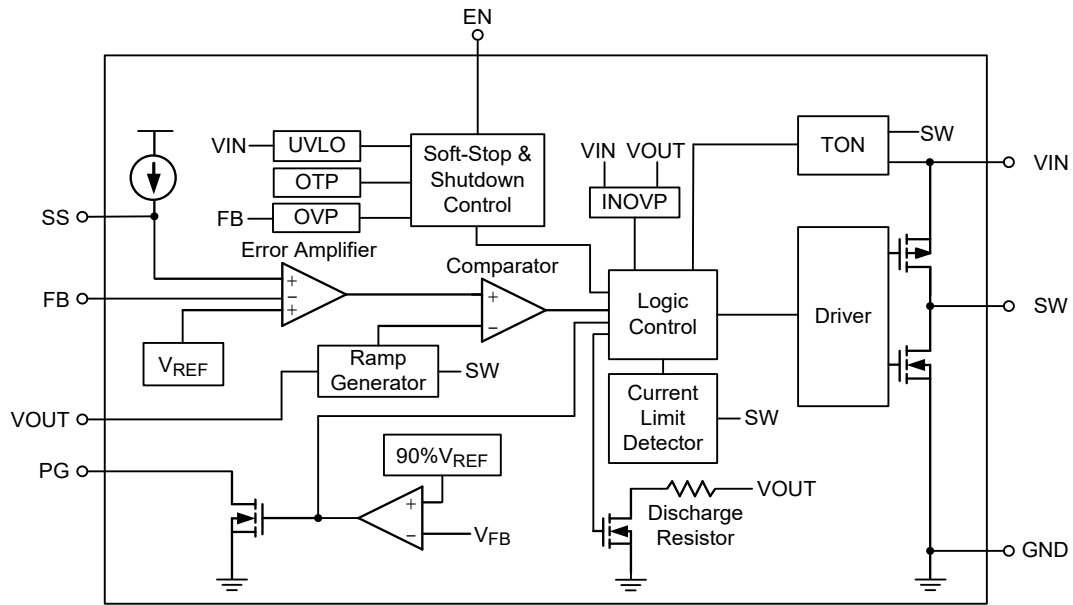
7 Pin Configuration



8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PG	Open-drain power-good indicator pin for the device output status. To enable normal operation, pull-up this pin using a 100kΩ resistor to the I/O reference power source. The PG output will set to logic-high once device output settle within the target range, and will be pulled low to ground if any internal protection is triggered. If unused, leave it floating.
2	VIN	Power input. The input voltage range is from 2.5V to 5.5V. Connect an input capacitor of 10μF, X7R or larger ceramic capacitor (with an effective capacitance >2.53μF at TA = 125°C and a 5.5V _{DCbias} condition) between this pin and the GND pins.
3	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to an inductor between SW and the output capacitor.
4	GND	Power ground. Connect this pin to the PCB ground planes with multiple vias for thermal performance consideration.
5	EN	Enable control input. Connecting this pin to a logic high enables the device, and connecting this pin to ground disables the device.
6	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and ground to set the soft-start time.
7	VOUT	Output voltage sense input. Connect this pin to the external output capacitors located near the critical load to maintain the desired output level.
8	FB	Feedback sense input pin. Connect this pin to the midpoint of the external feedback resistive divider, which is between the sensing point of the VOUT pin and the FB pin to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.6V.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ----- -0.3V to 6.5V
- VIN to SW ----- -0.3V to 6.5V
- VIN to SW (t≤10ns) ----- -2.5V to 9V
- Switch Node Voltage, SW ----- -0.3V to 6.5V
 <10ns ----- -5V to 8V
- Other I/O Pins Voltages ----- -0.3V to 6.5V
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
- HBM (Human Body Model) ----- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ----- 2.5V to 5.5V
- Output Voltage, VOUT ----- 0.6V to 3.3
- Junction Temperature Range ----- -40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		SOT583	Unit
θJA	Junction-to-ambient thermal resistance (JEDEC standard)	113.41	°C/W
θJC(Top)	Junction-to-case (top) thermal resistance	83.6	°C/W
θJC(Bottom)	Junction-to-case (bottom) thermal resistance	9.7	°C/W
θJA(EVB)	Junction-to-ambient thermal resistance (specific EVB)	66	°C/W
ΨJC(Top)	Junction-to-top characterization parameter	2.2	°C/W
ΨJB	Junction-to-board characterization parameter	48.9	°C/W

Note 5. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. θJA(EVB), ΨJC(TOP), and ΨJB are measured on a high effective-thermal-conductivity four-layer test board which is in size of 180mm x 90mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

($V_{IN} = 3.6V$, $T_A = T_J = -40$ to $125^\circ C$, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	VIN	VEN = 2V	2.5	--	5.5	V
Undervoltage Lockout Threshold	VUVLO_H	VIN rising, TJ = -40 to 125°C	--	2.3	2.45	V
	VUVLO_L	VIN falling, TJ = -40 to 125°C	--	2.1	--	
Supply Current (Shutdown)	ISHDN	VIN = 3.6V, VEN = 0V, TJ = 25°C	--	0	1	μA
Supply Current (Quiescent)	IQ	VIN = 3.6V, VFB = 0.63V, no switching, TJ = 25°C	--	21	26	μA
Soft-Start						
Soft-Start Charge Current	ISS	0%VFB to 95%VFB	2.4	3	3.6	μA
Enable Voltage						
EN Input Voltage Rising threshold	VEN_R	EN high-level input voltage	1	--	--	V
EN Input Voltage Falling threshold	VEN_F	EN low-level input voltage	--	--	0.4	
Feedback Voltage						
Feedback Threshold Voltage	VFB	VIN = 3.6V, TJ = 25°C	0.594	0.6	0.606	V
		VIN = 3.6V, TJ = -40°C to 125°C	0.591	0.6	0.609	
Internal MOSFET						
High-Side On-Resistance	RDS(ON)_H	VIN = 5V	--	65	--	mΩ
Low-Side On-Resistance	RDS(ON)_L	VIN = 5V	--	35	--	
Switching Frequency and Minimum Off Timer						
Switching Frequency	fsw	VIN = 5V, VOUT = 1.2V, FCCM	--	1.2	--	MHz
Minimum Off-Time	toff_MIN		--	80	--	ns
Protection						
Input Overvoltage Protection Threshold	VIN_OVP	After VOUT_OVP enable	--	6.1	--	V
Input Overvoltage Protection Hysteresis	ΔVIN_OVP		--	160	--	mV
Output Overvoltage Protection Threshold	VOUT_OVP		110	115	120	%
Output Overvoltage Protection Hysteresis	ΔVOUT_OVP	Overvoltage protection release	--	10	--	%
Output Undervoltage Protection Threshold	VUVP		--	50	--	%
Output Undervoltage Protection Hysteresis	ΔVUVP	Undervoltage protection release	--	10	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good						
Power-Good Threshold	V _{TH_PGLH}	V _{OUT} rising, PG from low to high	87	90	93	%
	V _{TH_PGHL}	V _{OUT} falling, PG from high to low	82	85	88	%
Power-Good Rising/Falling, Delay Time	t _{PG_DLY}		--	80	--	μs
Output Discharge Resistor						
Output Discharge Switch On-Resistor	R _{DISCHG}	RTQ5765A, V _{EN} = 0V	--	150	--	Ω
		RTQ5765B, V _{EN} = 0V	--	5	--	Ω

14.1 System Characteristics

(The following specifications are guaranteed by design and are not performed in production testing. (T_A = T_J = -40°C to 125°C, V_{IN} = 3.6V, L = 0.47μH, C_{OUT} = 22μFx2, unless otherwise specified.))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit						
High-Side Switch Peak Current Limit	I _{LIM_H}		4	5	6.2	A
Low-Side Switch Valley Current Limit	I _{LIM_L}		--	3	--	A
Low-Side Switch Negative Current Limit	I _{LIM_N}		--	1.5	--	A
Over-Temperature Protection						
Over-Temperature Protection Threshold	T _{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T _{OTP_HYS}		--	30	--	°C
Power-Good						
Self-Bias PG		When V _{IN} = 0V & EN = 0V, PG pull-up voltage = 3.6V, pull-up resistor = 300kΩ	--	--	0.7	V

15 Typical Application Circuit

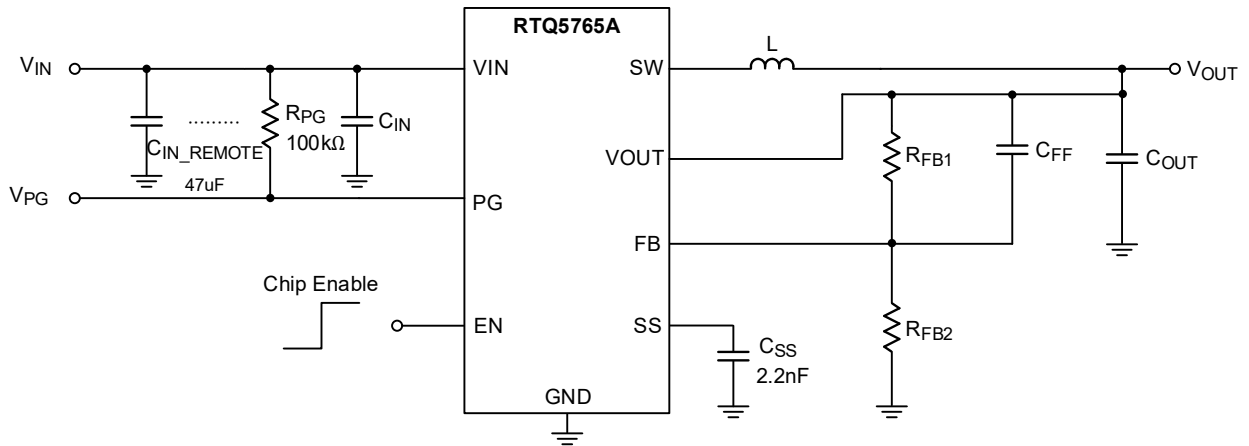


Table 1. Suggested Component Values

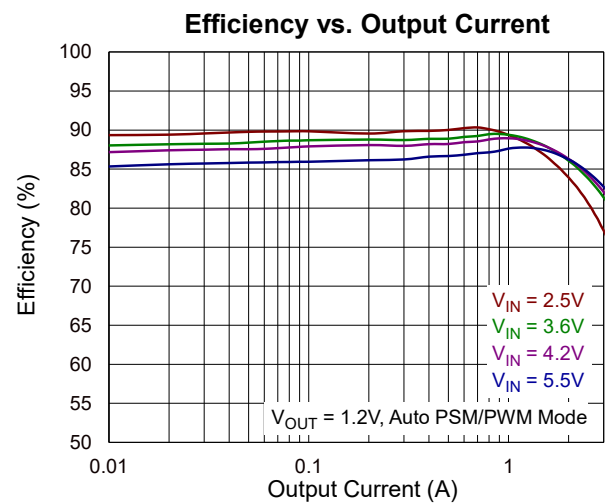
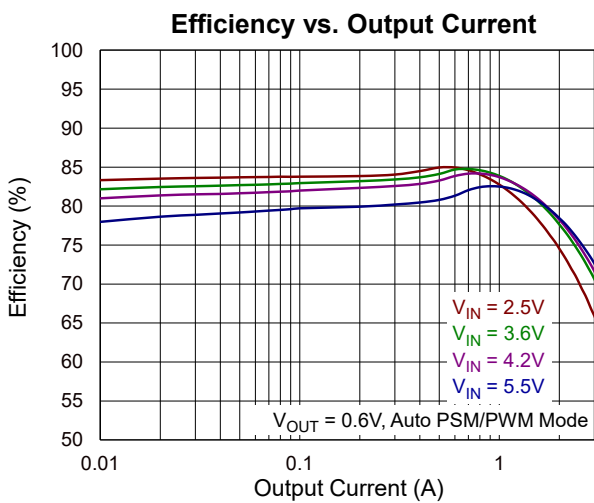
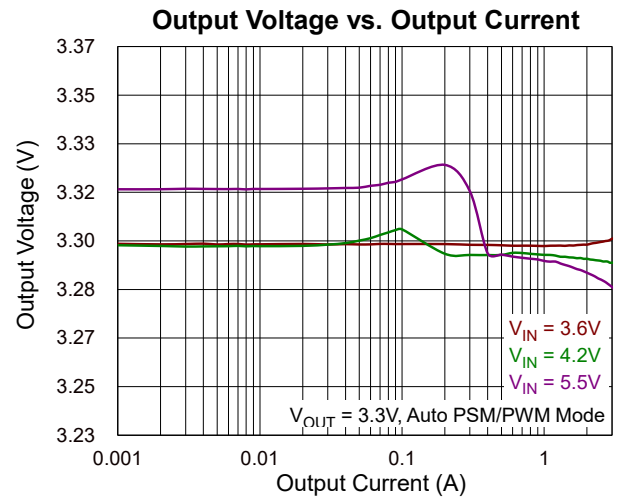
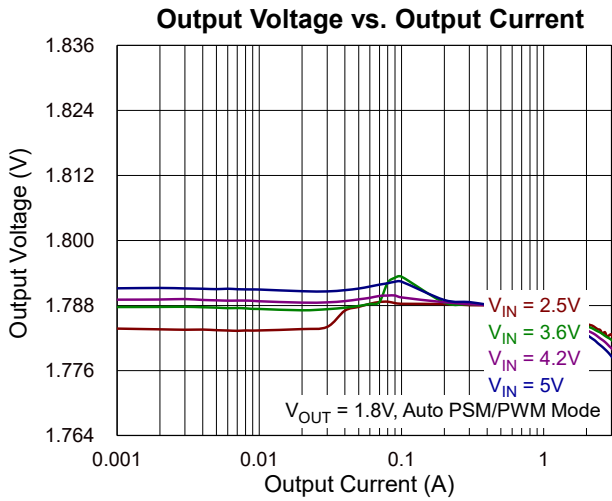
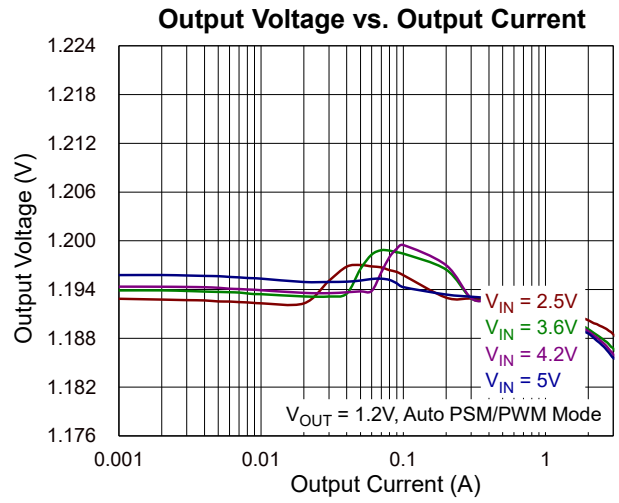
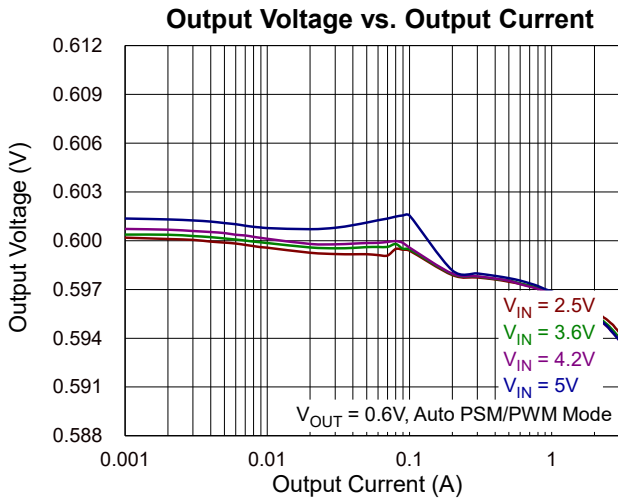
V _{OUT} (V)	R _{FB1} (kΩ)	R _{FB2} (kΩ)	C _{IN} (µF)	L (µH)	C _{OUT} (µF)	C _{FF} (pF)
3.3	499	110	10	0.47	22 x 2	22
2.5	124	39	10	0.47	22 x 2	22
1.8	200	100	10	0.47	22 x 2	22
1.2	200	200	10	0.47	22 x 2	22
0.85	150	360	10	0.47	22 x 2	22
0.6	0	--	10	0.47	22 x 3	--

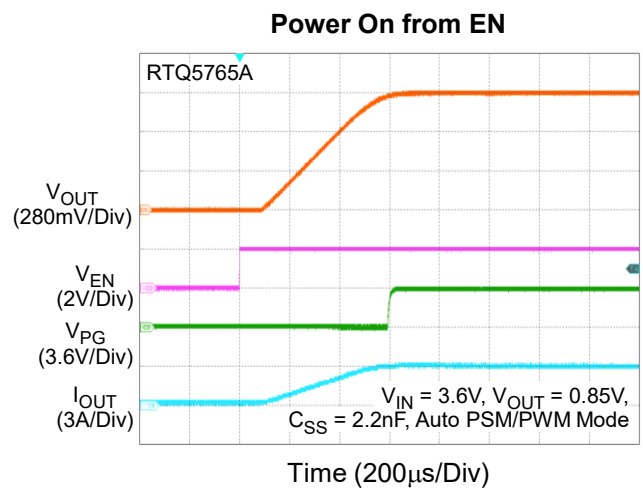
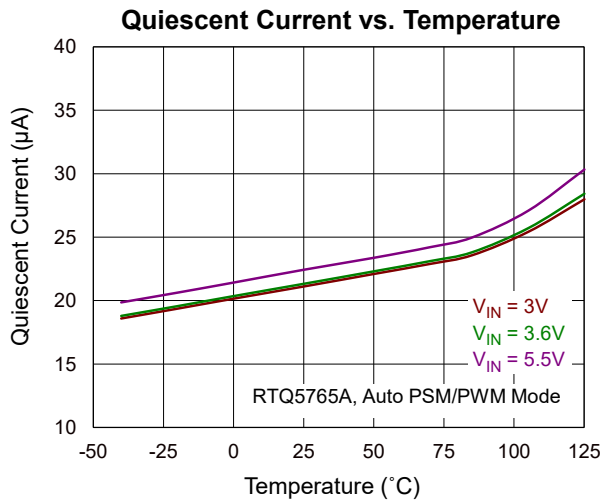
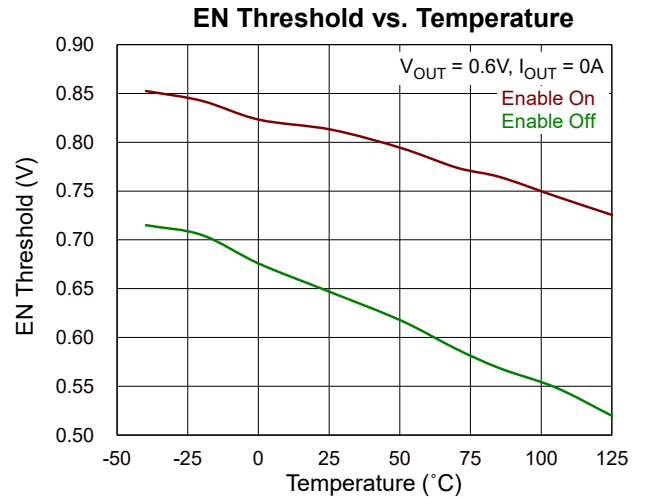
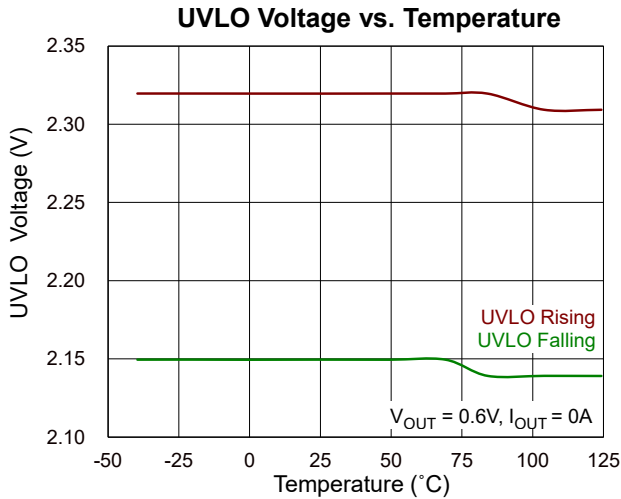
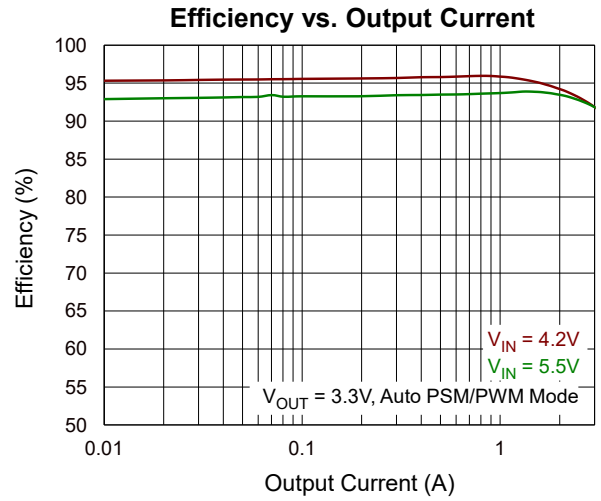
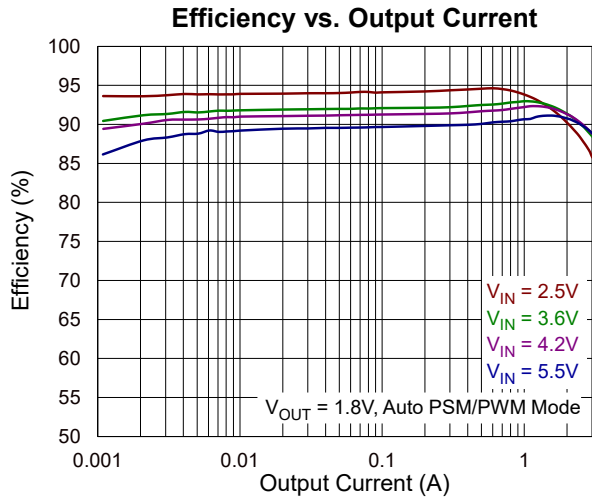
Table 2. Recommended External Components for 3A Maximum Load Current

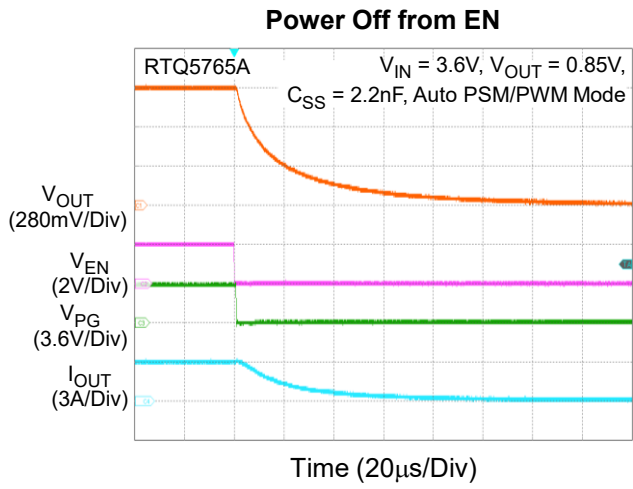
Component	Description	Vendor P/N	Manufacture
C _{IN}	10µF, 6.3V, X7R, 0603	GCM188D70J106ME36	Murata
	10µF, 10V, X5R, 0402	CL05A106MP68UN8	Samsung
C _{OUT}	22µF, 6.3V, X7T, 0603	GRM188D70J226ME01D	Murata
	22µF, 6.3V, X7T, 0805	MAASJ21GBD7226MTCA01	Taiyo Yuden
L	0.47µH	DFE252012F-R47M=P2	Murata
		CIGW252010GLR47MNE	Samsung

Note 7. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

16 Typical Operating Characteristics







17 Operation

The RTQ5765A/RTQ5765B is a synchronous buck DC-DC converter that delivers up to 3A output current from a 2.5V to 5.5V input supply.

17.1 Advanced Constant On-Time Control and Switching Node Operation

The RTQ5765A/RTQ5765B adopts ACOT[®] control for its ultrafast transient response, low external component counts, and stable with low ESR MLCC output capacitors. When the feedback voltage falls below the feedback reference voltage, the minimum off-time one-shot (80ns, typical) has timed out, and the inductor current is below the current-limit threshold, then the internal on-time one-shot circuitry is triggered, and the high-side switch is turned on. Since the minimum off-time is short, the device exhibits ultrafast transient response and enables the use of smaller output capacitance.

The on-time is inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. After the on-time one-shot timer expires, the high-side switch is turned off, and the low-side switch is turned on until the on-time one-shot is triggered again. In steady state, the error amplifier compares the feedback voltage VFB with an internal reference voltage. If the virtual inductor current ramp voltage is lower than the output of the error amplifier, a new pre-determined fixed on-time will be triggered by the on-time one-shot generator.

17.2 Power Saving Mode

The RTQ5765A/RTQ5765B automatically enters power saving mode (Auto PSM/PWM mode) at light loads to maintain high efficiency. As the load current decreases, and eventually the inductor current ripple valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side switch is turned off when zero inductor current is detected. As the load current is further decreased, it takes a longer time to discharge the output capacitor to the level that requires the next on-time. The switching frequency decreases and is proportional to the load current to maintain high efficiency at light loads.

17.3 Enable Control

The RTQ5765A/RTQ5765B provides an EN pin, as an external chip enable control, to enable or disable the device. If VEN is held below a logic-low threshold voltage (VEN_L) of the enable input (EN), the converter will disable the output voltage, that is, the converter is disabled, and switching is inhibited even if the VIN voltage is above the undervoltage lockout threshold (VUVLO). In shutdown mode, the supply current can be reduced to ISHDN (μA). If the EN voltage rises above the logic-high threshold voltage (VEN_H) while the VIN voltage is higher than the UVLO threshold, the device will turn on, that is, switching being enabled and the soft-start sequence being initiated.

17.4 Soft-Start (SS)

The RTQ5765A/RTQ5765B provides an internal soft-start feature for inrush control. At power-up, the external capacitor is charged by an internal current source to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching, and the output voltage will smoothly ramp up to its target regulation voltage only after this ramp voltage is greater than the feedback voltage VFB to ensure the converters have a smooth start-up from a pre-biased output.

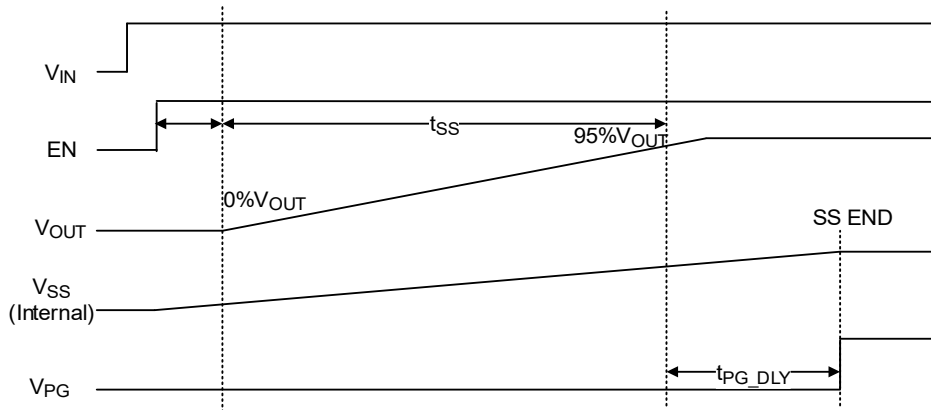


Figure 1. Start-Up Sequence

17.5 Maximum Duty Cycle Operation

The RTQ5765A/RTQ5765B is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than the minimum off-time, the RTQ5765A/RTQ5765B starts to enable the skip off-time function and keeps the high-side MOSFET switch on continuously. The RTQ5765A/RTQ5765B implements the skip off-time function to achieve a high duty cycle approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application when the input voltage momentarily drops to the normal output voltage requirement. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

17.6 Power-Good Indication

The RTQ5765A/RTQ5765B incorporates an open-drain power-good output (PG) that serves as a status indicator of the output voltage. The comparator's output delay plays a crucial role in preventing false flag operations in response to short excursions in the output voltage, such as those occurring during line and load transients. To configure the PG signal, it can be pulled up with a resistor to V_{IN} or an external voltage source, provided that the voltage does not exceed 5.5V.

The activation of the power-good function occurs after the completion of the soft-start and is controlled by a comparator connected to the feedback signal V_{FB} . When V_{FB} rises above a specified power-good high threshold (V_{TH_PGLH}), typically set at 90% of the reference voltage, the PG pin enters a high-impedance state, and V_{PG} remains in a high state after a certain delay period. On the other hand, if V_{FB} falls below the power-good low threshold (V_{TH_PGHL}), typically set at 85% of the reference voltage, the PG pin is pulled low.

Furthermore, once the device is started up, if any internal protection mechanism is triggered, the PG signal will be pulled low to ground.

A graphical representation of the power-good indication profile can be found in [Figure 2](#).

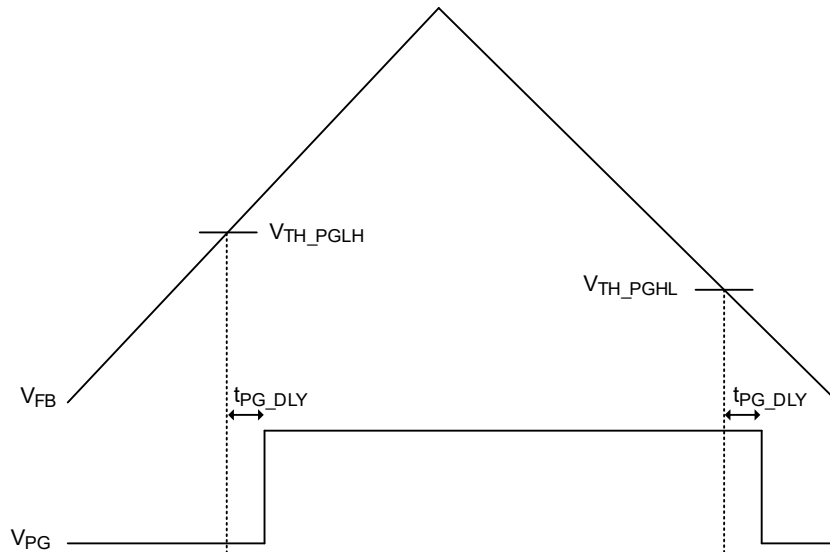


Figure 2. The Logic of PG

17.7 Input Undervoltage and Overvoltage Protection

The RTQ5765A/RTQ5765B is equipped with both input Undervoltage Lockout Protection (UVLO) and Overvoltage Lockout Protection (OVLO) to ensure proper operation. The device continuously monitors the VIN voltage and softly starts the buck converter to its regulated output voltage when the VIN voltage reaches the high threshold voltage 2.3V (typically) of UVLO. If the VIN voltage drops to its low threshold 2.1V (typically), the device shuts down immediately. In addition, the RTQ5765A/RTQ5765B also features a protection system. If the voltage on the VIN pin exceeds the predetermined OVLO threshold 6.1V (typically) during output OVP, the system will immediately trigger shutdown to prevent potential damage.

17.8 Overcurrent Protection

The RTQ5765A/RTQ5765B features cycle-by-cycle current-limit protection for both the high-side and low-side MOSFETs. The protection prevents the device from catastrophic damage in output short circuit, overcurrent, or inductor saturation.

The high-side MOSFET overcurrent protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch peak-current limit (I_{LIM_H}) after a certain amount of delay when the high-side switch being turned on each cycle. If an overcurrent condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current from exceeding the high-side current limit.

The low-side MOSFET overcurrent protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current, causing the output voltage to begin to drop. If it drops below the output undervoltage protection threshold, the IC will stop switching to avoid excessive heat.

17.9 Output Active Discharge

When the RTQ5765A/RTQ5765B is disabled by the EN pin, UVLO, or OTP, the device discharges the output capacitors through an internal 150/5Ω (typical) discharge resistor connected to ground. This function prevents the reverse current flow from the output capacitors to the input capacitors once the input voltage collapses. It does not need to rely on another active discharge circuit for discharging the output capacitors. This function will be turned off when the fault condition is removed.

17.10 Output Undervoltage Protection

The RTQ5765A/RTQ5765B includes output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB} . If V_{FB} drops below the undervoltage protection threshold (typically 50% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches. The RTQ5765A/RTQ5765B will enter output undervoltage protection with hiccup mode. During hiccup mode, the RTQ5765A/RTQ5765B shutting down for a predetermined off-time (t_{HICCUP_OFF}), typically 5 times of t_{SS} , and then automatically attempts to recover. When the fault is resolved before the soft-start completes, the device resumes normal operation. Otherwise, it continues to cycle through hiccup mode until the fault is rectified. This feature ensures the device operates safely, with reduced input current and power dissipation, and smoothly returns to normal operation once the fault is cleared. A short-circuit protection and recovery profile is shown below.

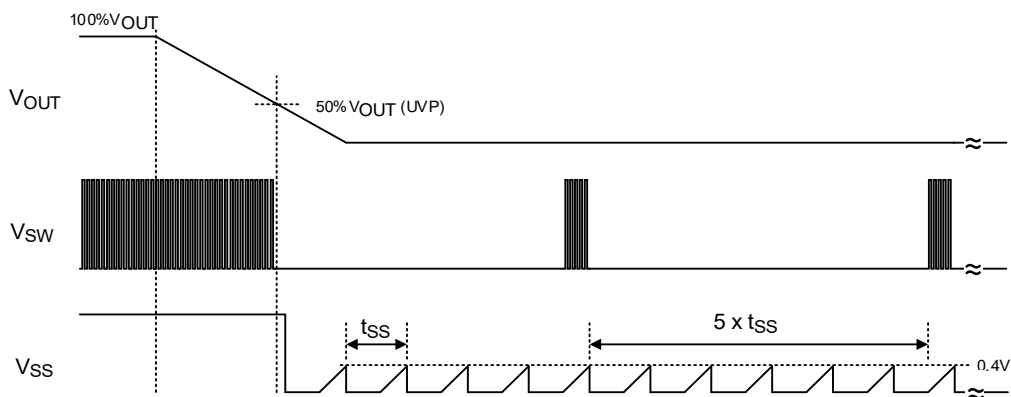


Figure 3. Hiccup Mode Behavior

17.11 Output Overvoltage Protection

The RTQ5765A/RTQ5765B includes an output overvoltage protection (OVP) circuit to limit output voltage and minimize output voltage overshoot. If the V_{FB} goes above 115% of the V_{FB} , the PG pin is still kept high. If the overvoltage condition still exists, the low-side MOSFET remains conducting until the low-side MOSFET valley current reaches the negative current limit $-1.5A$ (typical). If dynamic regulation cannot limit V_{OUT} increasing, once the input detects the input OVP 6.1V (typical), the RTQ5765A/RTQ5765B stops switching until the input voltage drops below 6V (typical). The RTQ5765A/RTQ5765B then resumes operation.

17.12 Over-Temperature Protection

The RTQ5765A/RTQ5765B includes an over-temperature protection (OTP) circuitry to prevent over-temperature due to excessive power dissipation. The OTP will shut down the switching operation when the junction temperature exceeds the over-temperature threshold ($T_{OTP} = 160^{\circ}C$). Once the junction temperature cools down by the over-temperature hysteresis ($T_{OTP_HYS} = 30^{\circ}C$), the IC will resume normal operation with a complete soft-start.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions.

The protection is activated outside the absolute maximum range of operation as a secondary fail-safe and should not be relied upon for regular operation. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

17.13 Negative Overcurrent Limit

The RTQ5765A/RTQ5765B is the factory optional part set for forced PWM (FCCM mode) operation, which allows for negative current operation. In FCCM mode, high negative current may be generated as an external power source tied to the output terminal unexpectedly. As the risk described above, the internal circuit monitors negative current during each on-time interval of the low-side MOSFET and compares it with the negative current limit (NOC) threshold. Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET will be turned on to discharge the energy from the output inductor. This behavior maintains the valley of negative current at the NOC threshold to protect the low-side MOSFET. However, the negative current cannot be limited at the NOC threshold anymore since minimum off-time is reached.

18 Application Information

(Note 8)

The basic RTQ5765A/RTQ5765B application circuit is shown in the [Typical Application Circuit](#). The external component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency, followed by C_{IN} and C_{OUT}.

18.1 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current, but it still depends on size considerations. The inductor used in the typical application circuit of the datasheet is recommended. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L(\mu\text{H}) = \frac{V_{\text{OUT}}(\text{V}) \times (V_{\text{IN}}(\text{V}) - V_{\text{OUT}}(\text{V}))}{V_{\text{IN}}(\text{V}) \times f_{\text{SW}}(\text{kHz}) \times \Delta I_L(\text{A})}$$

To enhance efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The selected inductor should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}):

$$\Delta I_L(\text{A}) = \frac{V_{\text{OUT}}(\text{V}) \times (V_{\text{IN}}(\text{V}) - V_{\text{OUT}}(\text{V}))}{V_{\text{IN}}(\text{V}) \times f_{\text{SW}}(\text{kHz}) \times L(\mu\text{H})}$$

$$I_{L_PEAK}(\text{A}) = I_{\text{OUT_MAX}}(\text{A}) + \frac{1}{2} \Delta I_L(\text{A})$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating that is equal to or greater than the switch current limit, rather than the peak inductor current.

18.2 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to accomplish this without causing a large variation in the input voltage. The waveform of the C_{IN} ripple voltage and ripple current are shown in [Figure 4](#). The peak-to-peak voltage ripple on the input capacitor can be estimated using the equation below:

$$\Delta V_{\text{CIN}}(\text{V}) = D \times I_{\text{OUT}}(\text{A}) \times \frac{1-D}{C_{\text{IN}}(\mu\text{A}) \times f_{\text{SW}}(\text{kHz})} + I_{\text{OUT}}(\text{A}) \times \text{ESR}(\Omega)$$

$$\text{where } D = \frac{V_{\text{OUT}}}{V_{\text{IN}} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low; therefore, the ripple caused by ESR can be ignored, and the minimum input capacitance can be estimated using the equation below:

$$C_{\text{IN_MIN}}(\mu\text{F}) = I_{\text{OUT_MAX}}(\text{A}) \times \frac{D(1-D)}{\Delta C_{\text{IN_MIN}}(\mu\text{F}) \times f_{\text{SW}}(\text{kHz})}$$

where $\Delta V_{\text{CIN_MIN}} < 100\text{mV}$.

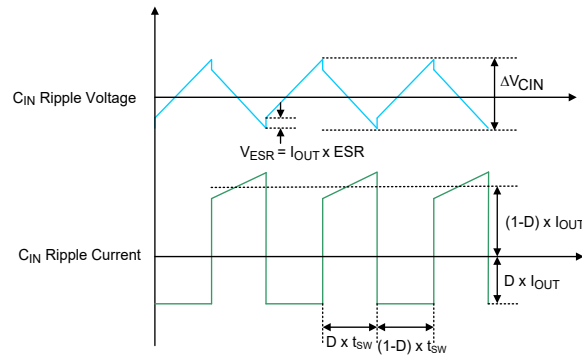


Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current, which can be calculated as follows:

$$I_{RMS}(A) \cong I_{OUT_MAX}(A) \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worse-case $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2 V_{OUT}$ for design purposes. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ5765A/RTQ5765B circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. It is recommended to connect a 10μF, X5R capacitor between the VIN pin to the PGND pin. This capacitor should have a package size of either 0402 or 0603.

18.3 Output Capacitor Selection

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output voltage ripple, ΔV_{OUT}, is determined by the following equation:

$$\Delta V_{OUT}(V) = \Delta I_L(A) \left(ESR + \frac{1}{8 \times C_{OUT}(\mu F) \times f_{SW}(kHz)} \right)$$

where f_{sw} is the switching frequency and ΔI_L is the inductor ripple current. The output voltage ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q factor of ceramic capacitors combined with trace inductance can also lead to significant ringing.

Nevertheless, high-value, low-cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications.

18.4 Output Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT} , and its equivalent series resistance, $RESR$, must be considered. The output peak-to-peak ripple voltage V_{RIPPLE} , caused by the inductor current ripple ΔI_L , is characterized by two components: ESR ripple $V_{RIPPLE(ESR)}$ and capacitive ripple $V_{RIPPLE(C)}$, and can be expressed as follows:

$$V_{RIPPLE}(V) = V_{RIPPLE(ESR)}(V) + V_{RIPPLE(C)}(V)$$

$$V_{RIPPLE(ESR)}(V) = \Delta I_L(A) \times RESR(\Omega)$$

$$V_{RIPPLE(C)}(V) = \frac{\Delta I_L(A)}{8 \times C_{OUT}(\mu F) \times f_{SW}(MHz)}$$

If ceramic capacitors are used as the output capacitors, both components need to be considered due to the extremely low ESR and relatively small capacitance.

18.5 Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT[®] transient response is very quick, and output transients are usually small. The following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components: the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formula to check if the ESR is low enough (typically not an issue with ceramic capacitors) and if the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

$$V_{ESR_STEP}(V) = \Delta I_{OUT}(A) \times RESR(\Omega)$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT[®] control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasites) and maximum duty cycle for a given input and output voltage as follows:

$$t_{ON}(s) = \frac{V_{OUT}(V)}{V_{IN}(V) \times f_{SW}(Hz)} \text{ and } D_{MAX} = \frac{t_{ON}(s)}{t_{ON}(s) + t_{OFF_MIN}(s)}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as follows:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT}(\mu F) \times (V_{IN_MIN}(V) \times D_{MAX} - V_{OUT}(V))}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage.

$$V_{SOAR}(V) = \frac{L(\mu H) \times (\Delta I_{OUT})^2 (A)}{2 \times C_{OUT}(\mu F) \times V_{OUT}(V)}$$

Because some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR step up or down should be taken into consideration.

Using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation:

$$V_{OUT} = 0.6V \times (1 + R_{FB1}/R_{FB2})$$

Place the FB resistors within 5mm of the FB pin. For output voltage accuracy, use divider resistors with a tolerance of 1% or better.

18.6 EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN} , as shown in [Figure 5](#), to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins.

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in [Figure 6](#). In this case, a pull-up resistor, R_{EN} , is connected between V_{IN} and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage lockout threshold, as shown in [Figure 7](#).

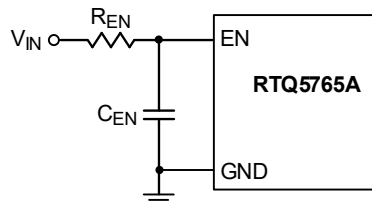


Figure 5. Enable Timing Control

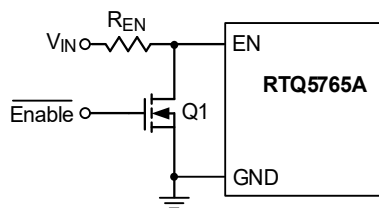


Figure 6. Logic Control for the EN Pin

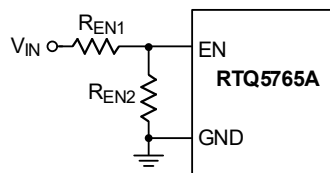


Figure 7. Resistive Divider for Undervoltage Lockout Threshold Setting

18.7 Power-Good Output

The PG pin is an open-drain power-good indication output and should be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 5.5V or the output of the RTQ5765A/RTQ5765B if the output voltage is regulated below 5.5V. It is recommended to connect a 100kΩ between the external voltage source to the PG pin.

18.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to- ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a SOT-583 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 66°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ) / (66^\circ\text{C/W}) = 1.52\text{W for a SOT-583 (FC) package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in [Figure 8](#) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

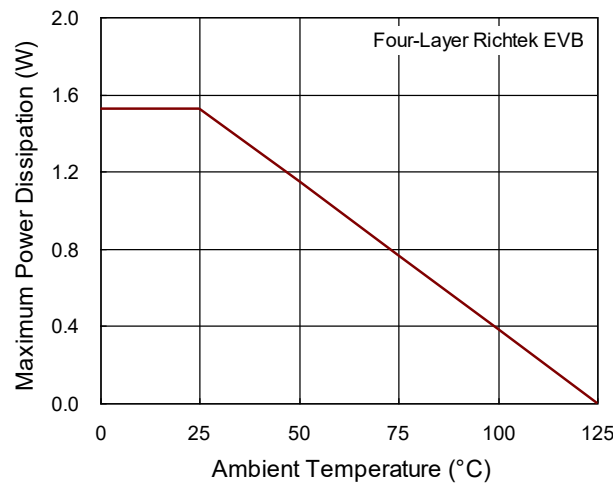


Figure 8. Derating Curve of Maximum Power Dissipation

18.9 Layout Considerations

For best performance of the RTQ5765A/RTQ5765B, the following layout guidelines must be strictly followed:

- The input capacitor must be placed as close as possible to the IC to minimize the power loop area. A typical 0.1μF decoupling capacitor is recommended to reduce the power loop area and any high frequency component on VIN.
- The SW node has high frequency voltage swings, so the SW node area should be kept small. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Keep every power trace connected to the pin as wide as possible for improving thermal dissipation.
- The feedback line should be kept as short as possible and away from the power inductor, especially from the area surrounding the inductor.

An illustration of a PCB layout guide is depicted in [Figure 9](#).

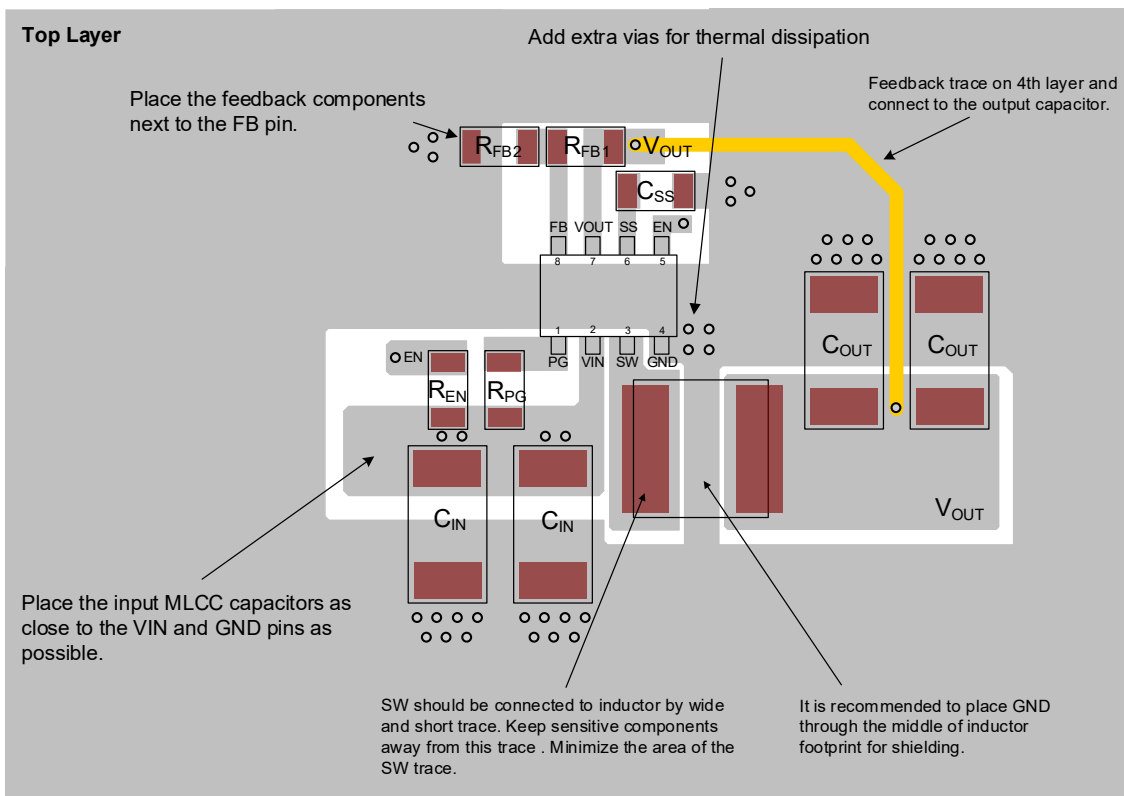
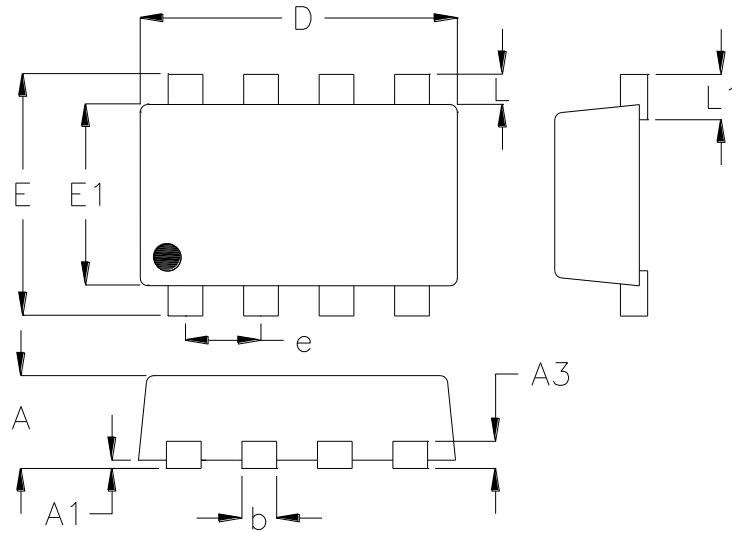


Figure 9. PCB Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

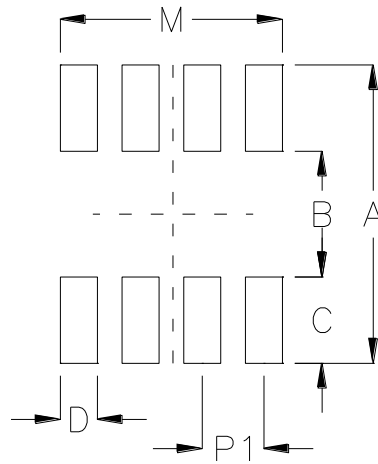
19 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.080	0.180	0.003	0.007
b	0.180	0.260	0.007	0.010
D	2.000	2.200	0.079	0.087
E	1.500	1.700	0.059	0.067
E1	1.100	1.300	0.043	0.051
e	0.500		0.020	
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016

SOT-583 Package (FC)

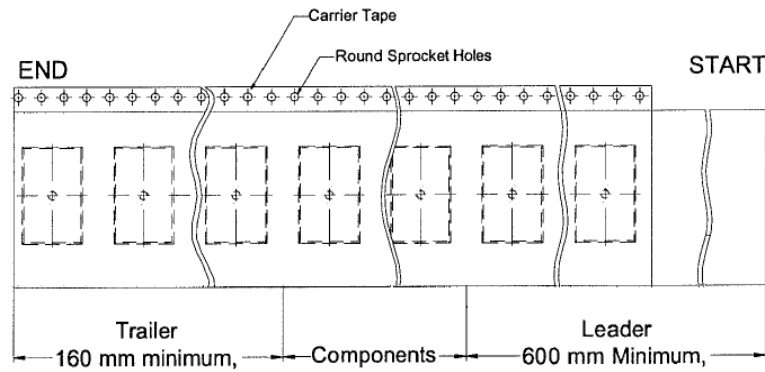
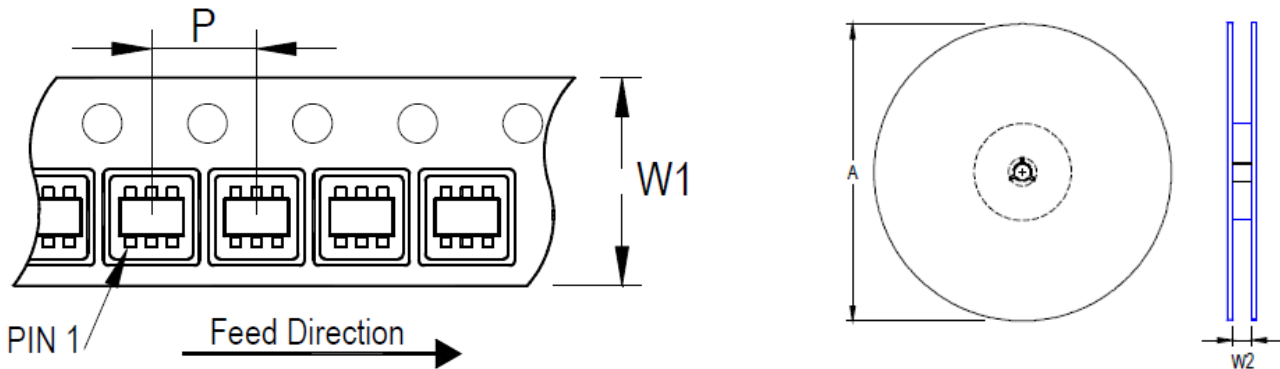
20 Footprint Information



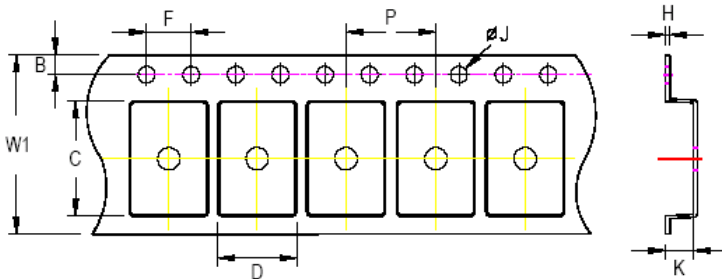
Package	Number of Pins	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
SOT-583(FC)	8	0.50	2.42	1.02	0.70	0.30	1.80	±0.10

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-583	8	4	180	7	5,000	160	600	8.4/9.9









C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1		P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.	
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.65mm	0.85mm	0.6mm	

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-583	7"	5,000	Box A	3	15,000	Carton A	12	180,000
			Box E	1	5,000	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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22 Datasheet Revision History

Version	Date	Description
00	2026/3/4	First Edition