Bi-Directional Current and Power Monitor with 16-Bit ADC and Alert Function for High-Side or Low-Side Measurement

1 General Description

The RTQ6056B-QA is a high-accuracy current-sense monitor featuring I^{2}C and SMBus interface, providing comprehensive system information by reading both load current and power.

The device monitors the voltage drop across sense resistor and the BUS voltage, converting these measurements into current in amperes and power in watts through internal analog-to-digital converter (ADC). Programmable calibration, adjustable conversion time, and an averaging function are integrated to offer enhanced design flexibility.

The RTQ6056B-QA operates over a wide temperature range from –40°C to 125°C and operates with an input voltage from 2.7V to 5.5V. The device is capable of sensing current on a common-mode bus voltage from 0V to 36V.

An open-drain alert output is provided for system protection, enabling the host to receive warnings in the event of overcurrent, overvoltage, or overpower conditions.

The RTQ6056B-QA is available in a compact MSOP-10 package.

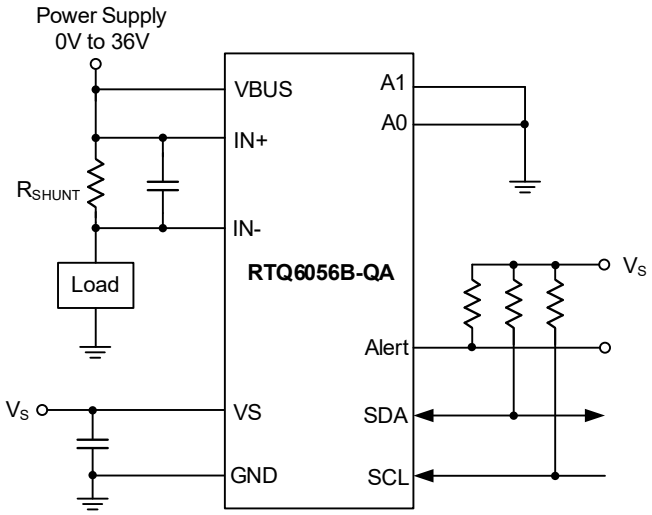
2 Features

- **AEC-Q100 Grade 1 Qualified**
- **I^{2}C and SMBus Compatible Interface**
- **Bi-Direction Current Sensing, Supporting Both High-Side and Low-Side Configurations**
- **2.7V to 5.5V Operation Supply Voltage Range**
- **Monitor Bus Voltage from 0V to 36V**
- **High Accuracy, Maximum 0.12% Gain Error**
- **Low Offset Voltage, Maximum 10μV Offset**
- **Current, Bus Voltage, and System Power Reporting**
- **Programmable Warning Threshold**
- **Overcurrent, Overvoltage, and Over-Power Alert Functions**
- **MSOP-10 Package**

3 Applications

- Body Control Units
- Automotive Seat Module Control
- Hybrid and Electric Vehicle Battery Management Systems
- Automotive Window Module Control
- Automotive Door Module Control
- Electronic Control Modules

4 Simplified Application Circuit



5 Ordering Information

RTQ6056B □ - □□

Packing
A: Standard
Pin 1 Orientation
(Quadrant 1, Follow EIA-481)

Product Grade
QA: Automotive Grade

Package Type(1)
D: MSOP-10

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

0L=: Product Code
YMDAN: Date Code

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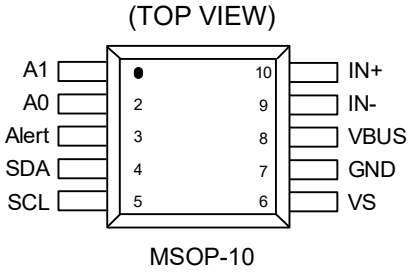
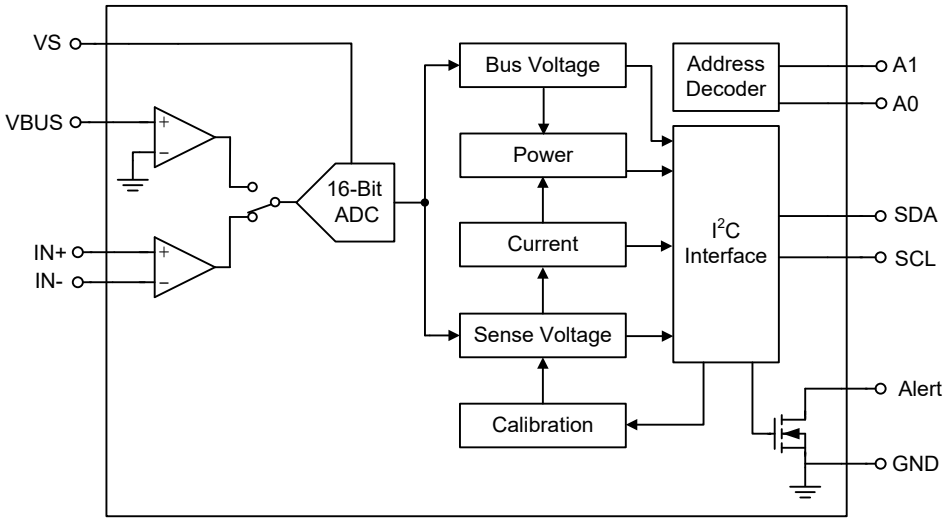
7 Pin Configuration



8 Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	A1	Digital Input	Address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Digital Input	Address pin. Connect to GND, SCL, SDA, or VS.
3	Alert	Digital Output	Multi-functional alert, open-drain output.
4	SDA	Digital IN/OUT	Bi-directional serial data interface.
5	SCL	Digital Input	Serial clock interface.
6	VS	Power	Power supply, 2.7V to 5.5V. Connect a 0.1μF capacitor as close to the VS pin as possible.
7	GND	Ground	Ground.
8	VBUS	Analog Input	Bus voltage input.
9	IN-	Analog Input	Negative current-sensing input. The load side connects to an external sense resistor.
10	IN+	Analog Input	Positive current-sensing input. The power side connects to an external sense resistor.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, V_S ---------- –0.3V to 6V
- Power Sensing Pins, Common Mode (V_{IN+} + $V_{IN–}$)/2, V_{CM} ---------- –0.3V to 40V
- Power Sensing Pins, Different Mode (V_{IN+} – $V_{IN–}$), V_{SENSE} (Note 3)---------- –40V to 40V
- Bus Voltage, V_{BUS} ---------- –0.3V to 40V
- Other Pins, ---------- –0.3 to 6V
- Input Current into Any Pin, I_{IN} ---------- 5mA
- Open-Drain Digital Output Current, I_{OUT}---------- 10mA
- Power Dissipation, P_D @ T_A = 25°C

  MSOP-10 ---------- 0.51W
- Package Thermal Resistance (Note 4)

  MSOP-10, θ_{JA} ---------- 195°C/W

  MSOP-10, θ_{JC} ---------- 64°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model) ---------- 2Kv

Note 2. Stresses listed as the above under "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 3. The voltage at V_{IN+} and $V_{IN–}$ pins must not exceed the range –0.3V to 40V.

Note 4. θ_{JA} is simulated in the natural convection at T_A = 25°C on a low effective thermal conductivity test board. θ_{JC} is simulated at the bottom of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 6)

- Common-Mode Input Voltage, V_{CM} ---------- 12V
- Operating Supply Voltage, V_S---------- 3.3V
- Junction Temperature Range ---------- –40°C to 125°C

Note 6. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = T_J = –40°C to 125°C, V_S = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV and V_{BUS} = 12V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Operating Supply Range	V_S		2.7	--	5.5	V
Quiescent Current	I_Q		--	550	650	μA
	I_{Q_SD}	Power-down (shutdown) mode	--	3.5	6	μA
Power-On Reset Threshold	V_{POR}		--	2	--	V
Input						
Sense Voltage Input Range	V_{SENSE}		–81.92	--	81.92	mV
Bus Voltage Input Range	V_{BUS}		0	--	36	V
Common-Mode Rejection (Note 8)	CMRR	0V ≤ V_{IN+} ≤ 36V	126	140	--	dB
Sense Offset Voltage, RTI (Note 9)	V_{S_OS}		--	±2.5	±10	μV
Sense Offset Voltage, RTI vs. Temperature		–40°C ≤ T_A ≤ 125°C	--	0.02	0.1	μV/°C
Sense Offset Voltage, RTI vs. Power Supply	PSRR	2.7 V ≤ V_S ≤ 5.5 V	--	2.5	--	μV/V
Bus Offset Voltage, RTI	V_{B_OS}		--	±1.25	±7.5	mV
Bus Offset Voltage, RTI vs. Temperature		–40°C ≤ T_A ≤ 125°C	--	10	40	μV/°C
Bus Offset Voltage, RTI vs. Power Supply (Note 8)	PSRR	2.7 V ≤ V_S ≤ 5.5 V	--	0.5	--	mV/V
Input Bias Current (I_{IN+} or $I_{IN–}$ Pins)	I_B		--	35	--	μA
VBUS Input Impedance			--	830	--	kΩ
Input Leakage		(IN+ pin) + (IN– pin), power-down mode	--	0.1	0.5	μA
DC Accuracy						
ADC Native Resolution			--	16	--	Bits
1 LSB Step Size		Sense voltage	--	2.5	--	μV
		Bus voltage	--	1.25	--	mV
Sense Voltage Gain Error (Note 9)			--	0.02	0.12	%
Sense Voltage Gain Error vs. Temperature		–40°C ≤ T_A ≤ 125°C	--	10	50	ppm/°C
Sense Voltage Nonlinearity			--	0.05	--	%
Bus Voltage Gain Error			--	0.02	0.4	%
Bus Voltage Gain Error vs. Temperature		–40°C ≤ T_A ≤ 125°C	--	10	72	ppm/°C
Bus Voltage Nonlinearity (Note 8)			--	0.05	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC Conversion Time, Continuous Mode	t_{CT1}	bit = 000	--	139	--	µs
		bit = 001	--	203	--	
		bit = 010	--	269	--	
		bit = 011	--	525	--	
		bit = 100	--	1037	--	
		bit = 101	--	2061	--	
		bit = 110	--	4109	--	
		bit = 111	--	8205	--	
I²C/SMBus						
Timeout			--	37	--	ms
Digital Input/Output						
Input Capacitance			--	5	--	pF
Leakage Input Current	I_{LEAK}	0 ≤ Input pin voltage ≤ V_S	--	0.1	--	µA
High-Level Input Voltage	V_{IH}		0.7 x V_S	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	0.3 x V_S	V
Low-Level Output Voltage, SDA, Alert	V_{OL}	I_{OL} = 3mA	--	--	0.4	V

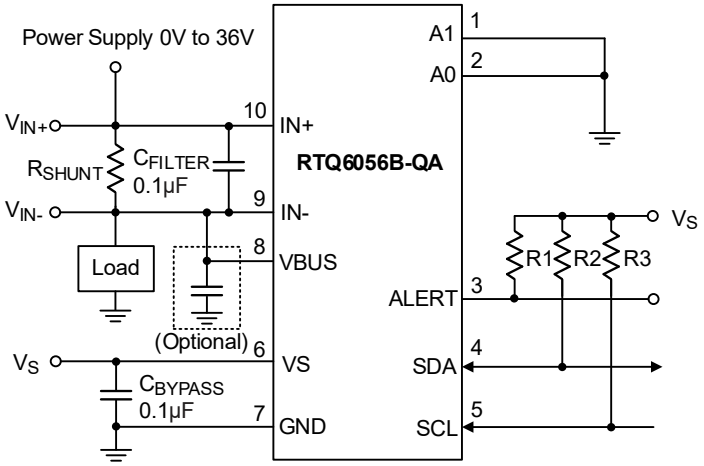
Note 7. RTI = Referred to input.

Note 8. Specifications are guaranteed by design, not production test.

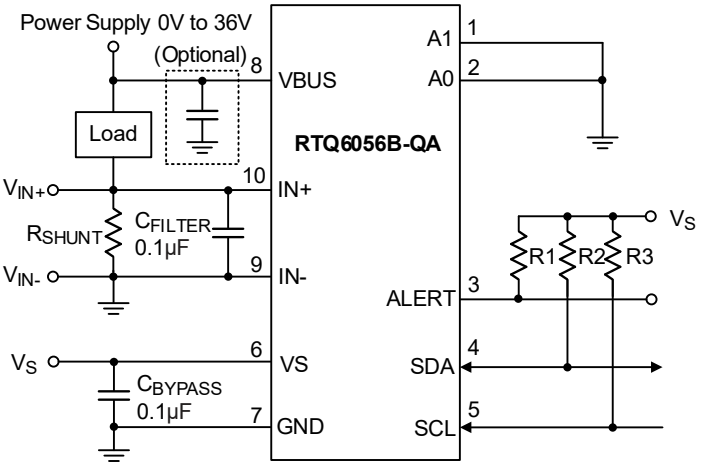
Note 9. Conversion time ≥ 525µs.

13 Typical Application Circuit

13.1 High-Side Sensing Circuit Application

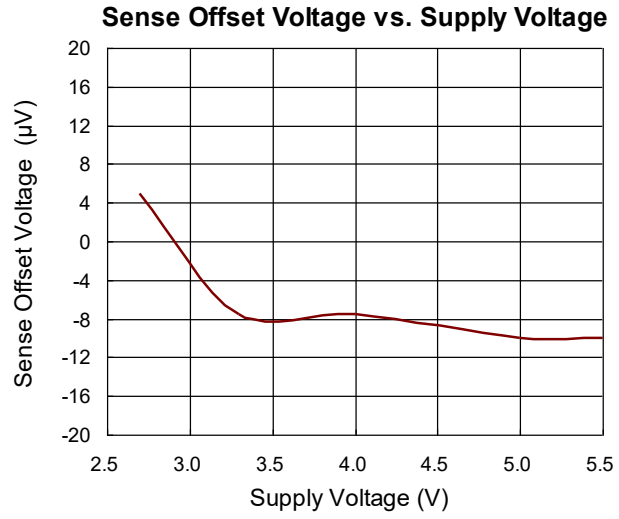


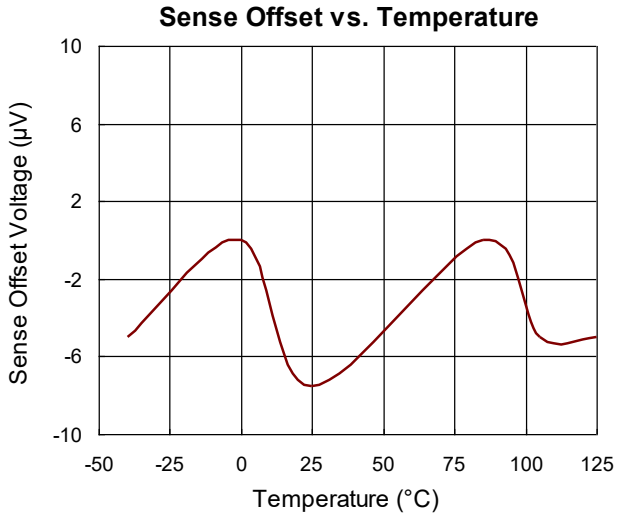
13.2 Low-Side Sensing Circuit Application

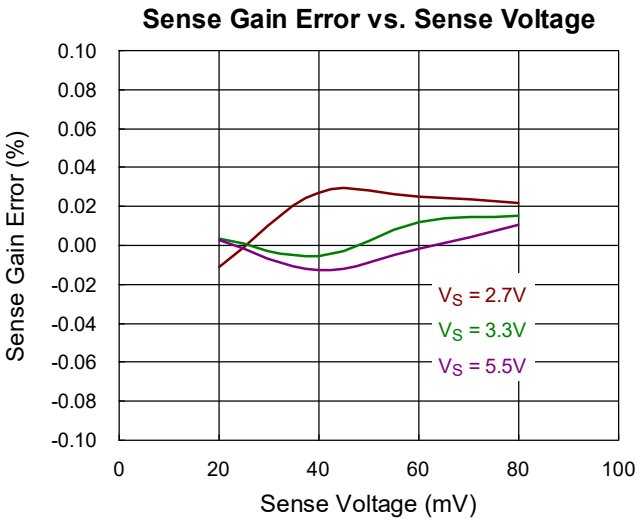


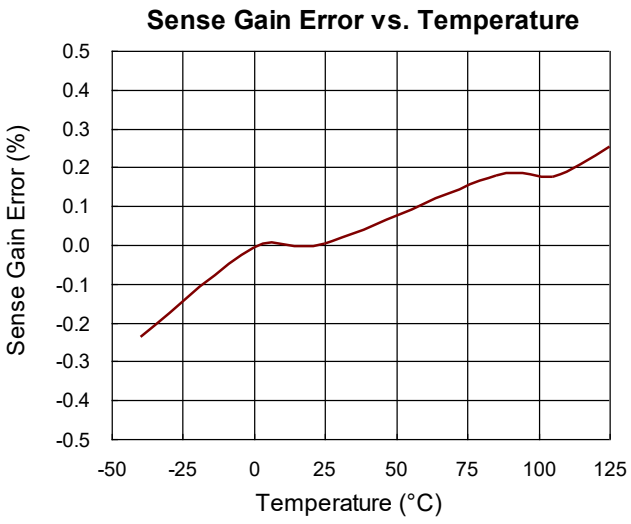
Note 10. All the input and output capacitors values are suggested and refer to the effective capacitances, considering any de-rating effects, such as DC bias.

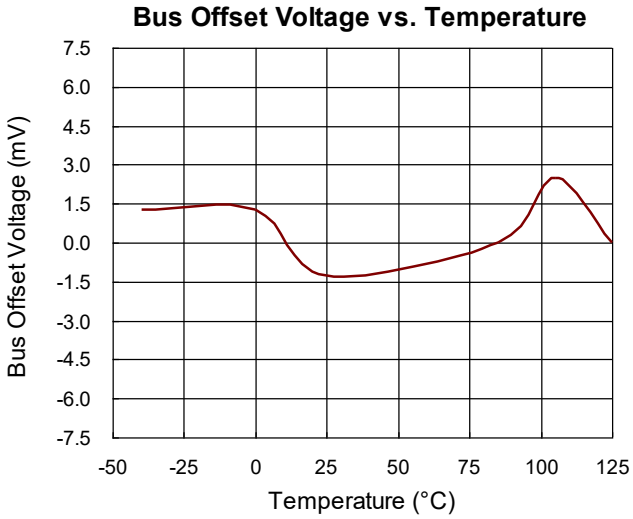
14 Typical Operating Characteristics

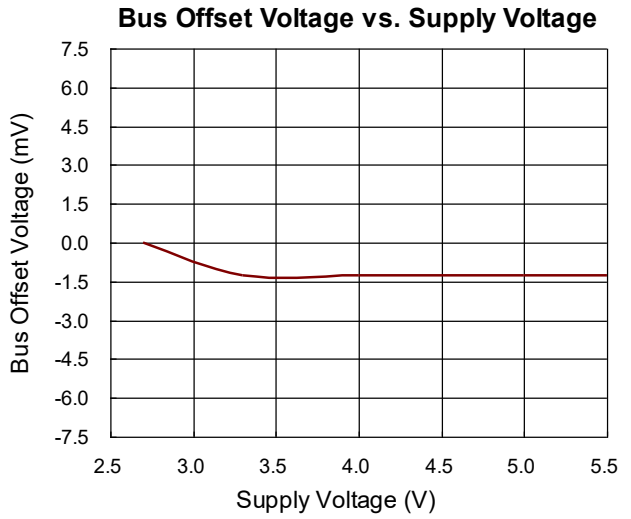




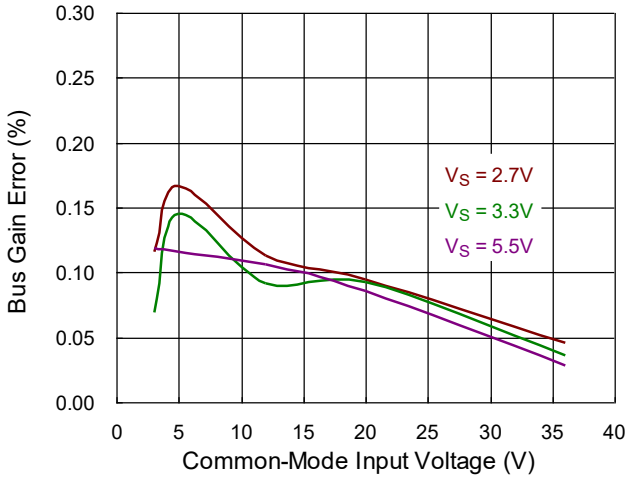




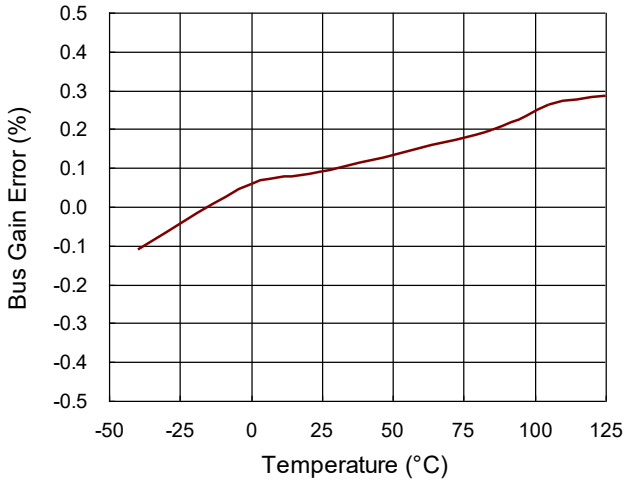




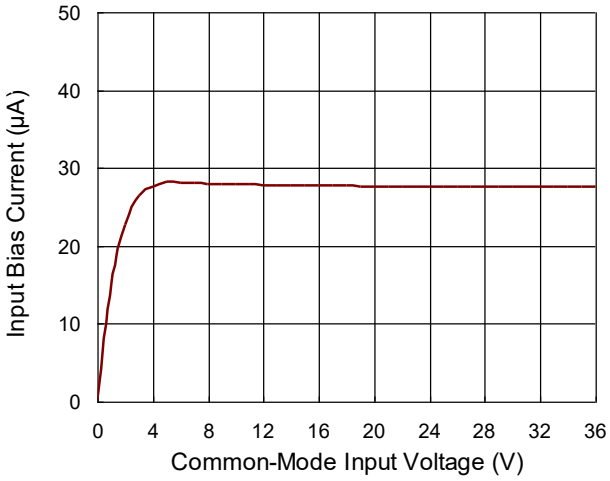
Bus Gain Error vs. Common-Mode Input Voltage



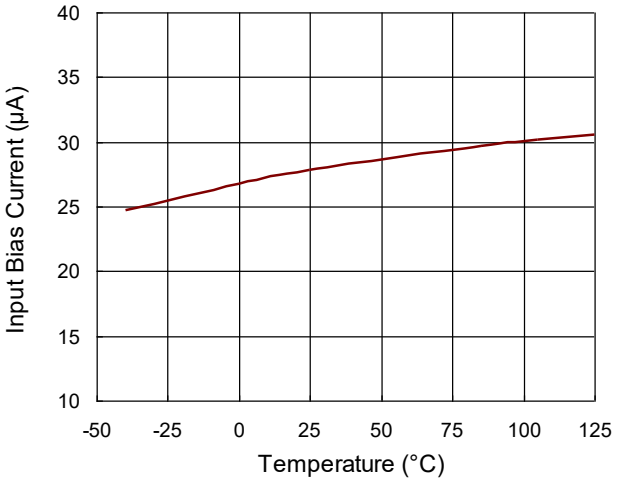
Bus Gain Error vs. Temperature



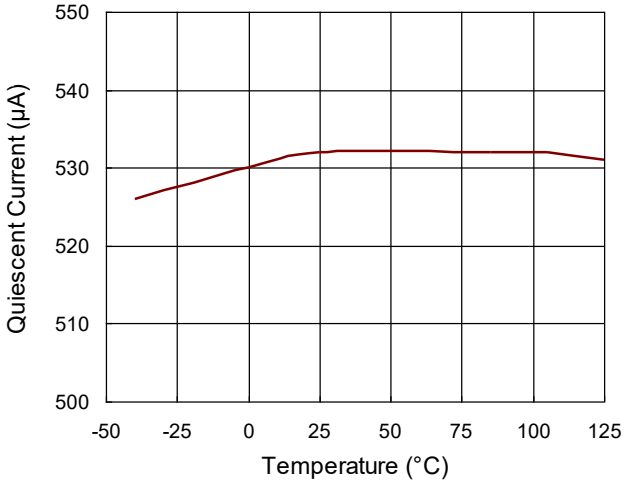
Input Bias Current vs. Common-Mode Input Voltage



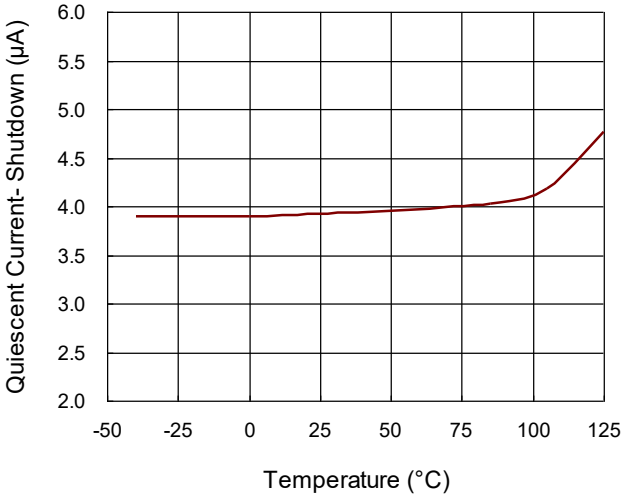
Input Bias Current vs. Temperature



Quiescent Current vs. Temperature



Quiescent Current-Shutdown vs. Temperature



15 Operation

The RTQ6056B-QA is a high-side/low-side current and power monitor with an integrated 16-bit ADC and an internal open-drain alert indicator. The device is ideal for a variety of industrial and telecom equipment applications.

The RTQ6056B-QA operates over a wide 0V to 36V input common-mode voltage range. Its internal 16-bit integrating analog-to-digital converter (ADC) allows users to read data such as voltage, current, and power. The full-scale sense voltage range from −81.9175mV and 81.92mV, combined with a programmable calibration function, enables wide dynamic range current measurement and flexibility in choosing sense resistor values.

15.1 Mode Configuration

The RTQ6056B-QA provides the ADC configuration through the Configuration Register (00h); which includes options for all-register reset, ADC conversion times, averaging mode, and operating mode selection.

The device supports several ADC operating modes: continuous mode, triggered mode, and shutdown mode. In the default continuous mode, the device continuously converts the sense voltage and bus voltage; after the voltage is read, the current is calculated using the calibration setting, and the power is subsequently determined.

In triggered mode, register data is retained, and the ADC only updates data after a new “WRITE” commend is executed to the Configuration Register (00h).

Shutdown mode is provided to minimize input quiescent current. While in shutdown mode, register read and write operations remain available. The device remains in shutdown mode until either continuous mode or triggered mode is selected.

15.2 Conversion Time and Averaging

The RTQ6056B-QA allows configurable conversion time and averaging time through the Configuration Register (00h), enabling users to optimize for accuracy and system timing requirements. The conversion time for both sense voltage and bus voltage can be selected from 139μs to 8.205ms. Longer conversion times provide higher noise immunity but require more time for data updates. Figure 1 illustrates the relationship between noise performance and conversion time. The averaging function also enhances the measurement accuracy by effectively filtering the signal. This approach allows the device to reduce noise in the measurement that may be caused by noise coupling into the signal. Increasing the number of averages enables the device to more effectively suppress the noise component, resulting in more stable and accurate readings.

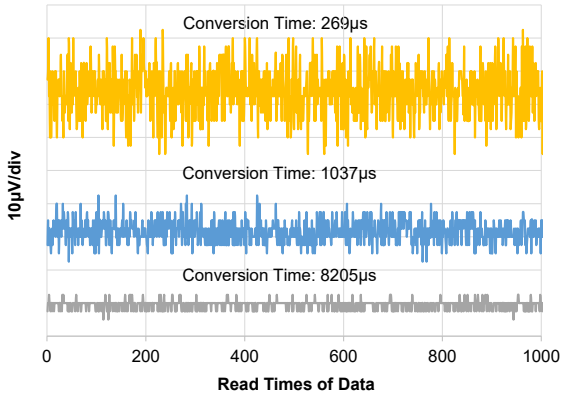


Figure 1. Noise vs. Conversion Time

15.3 Calibration and Current Calculation

The Calibration Register (05h) is programmed based on the value of the shunt resistor and the required current measurement resolution. The calibration value is calculated using the following equation:

$$\text{Calibration Setting (dec)} = \frac{0.00512}{R_{SHUNT} \times I_{LSB}}$$

where

- 0.00512 is an internal fixed value.
- I_{LSB} is the desired current measurement resolution.

The highest resolution for the Current Register (04h) can be achieved by using the smallest allowable Current_LSB based on the maximum output current, as shown below:

$$\text{Current resolution} = \frac{\text{Maximum Current}}{2^{15}}$$

If the highest resolution is lower than the expected resolution, it is common to select a value for the Current_LSB value that is a convenient round number and slightly higher than the minimum, to simplify the conversion of current in amperes and power in watts.

After programming the Calibration Register (05h), the value in the Current Register (04h) is calculated by multiplying the decimal value of the Sense Voltage Register (01h) by the decimal value of the Calibration Register, and then dividing by 2048, as shown below:

$$\text{Current} = \frac{\text{Sense Voltage} \times \text{Calibration Setting}}{2048}$$

After the device power-on, both the Current Register (04h) and the Power Register (03h) are initialized to zero. These registers are updated based on the corresponding sense voltage and bus voltage measurements.

15.4 Power Calculation

After the Current Register (04h) is updated, the power is calculated by multiplying the decimal value of the Bus Voltage Register (02h) by the decimal value of the Current Register (04h), and then dividing by 20000, as shown in the equation below:

$$\text{Power} = \frac{\text{Bus Voltage} \times \text{Current}}{20000}$$

15.5 Programing Example

Table 1 provides an example of register data and the calculation procedure in a real application.

Table 1. Power Calculation Procedure

Conditions: V_{CM} = V_{BUS} = 12V, R_{SHUNT} = 2mΩ, Load Current = 10A						
Procedure	**Register**	**Address**	**Data (Hex)**	**Data (Dec)**	**LSB**	**Value**
Step 1	Configuration	00h	4127	--	--	--
Step 2	Sense Voltage	01h	1F40	8000	2.5μV	20mV
Step 3	Bus Voltage	02h	2580	9600	1.25mV	12V
Step 4	Calibration	05h	A00	2560	--	--
Step 5	Current	04h	2710	10000	1mA	10A
Step 6	Power	03h	12C0	4800	25mV	120W

15.6 Alert Indicator

The RTQ6056B-QA provides a flexible response function that can be approached by a multi-functional indicator pin. Users can monitor up to five alert functions or a conversion Ready notification through the Mask/Enable Register (06h), with programmable thresholds set in the Alert Limit Register (07h). From the Mask/Enable Register (06h), one of the five alert events can be selected at a time. When the monitored event exceeds the threshold programmed in the Alert Limit Register (07h), the open-drain output of the Alert pin is pulled low. The five available alert functions are:

- Sense Overvoltage Limit (SOVL)
- Sense Undervoltage Limit (SUVL)
- Bus Overvoltage Limit (BOVL)
- Bus Undervoltage Limit (BUVL)
- Over-Power Limit (OPL)

If multiple alert functions are enabled, the function corresponding to the highest significant bit position takes priority and responds to the Alert Limit Register value. For example, if both the Sense Voltage Over-Limit function and the Sense Voltage Under-Limit functions are selected at the same time, the Alert pin asserts when the Sense Voltage Register exceeds the value in the Alert Limit Register.

The RTQ6056B-QA asserts a warning alert by comparing the actual measured value (“mathematics value”) to the programmed threshold, taking the sign bit into account. For instance, when the indicator is set to response to Sense Overvoltage Limit (SOVL), positive values are always considered higher than negative values. Examples for unidirectional OC alert and bidirectional OC alert are shown in Figure 2, respectively.

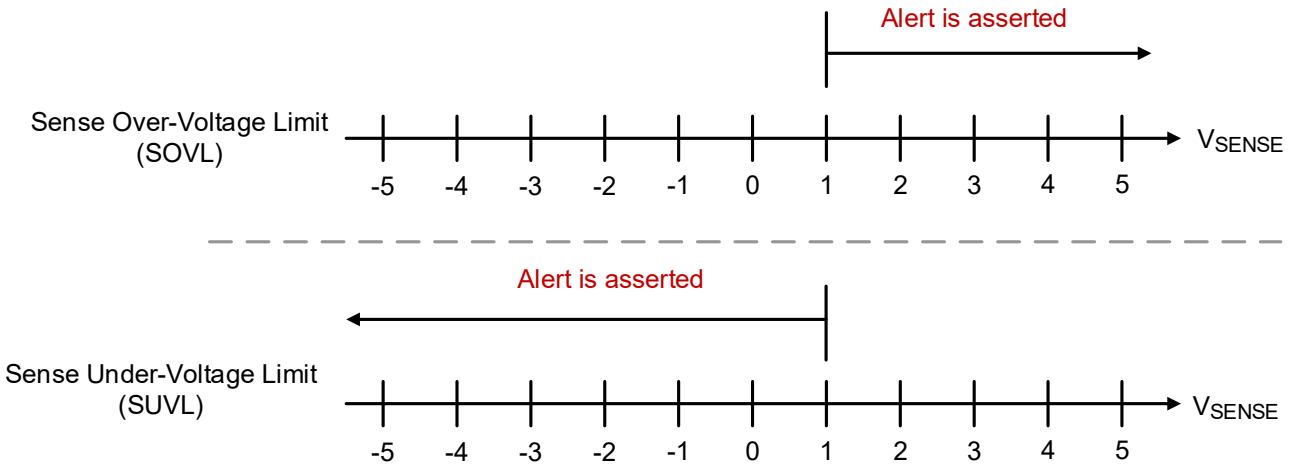


Figure 2. Alert Pin Response to SOVL and SUVL When Alert Limit Register (07h) is Set to 1 (Unidirectional OC Alert)

15.7 Conversion Ready Indicator

The Conversion Ready state can also be monitored via the Alert pin, providing notification when the device has completed the previous conversion and is ready to begin a new one. The Conversion Ready signal can be monitored at the Alert pin in conjunction with one of the alert functions. If both an alert function and the Conversion Ready feature are enabled, the source of the alert must be determined by reading the Mask/Enable Register after the ALERT pin is asserted. To identify the source, read the Conversion Ready Flag (CVRF, bit3), and the Alert Function Flag (AFF, bit4) in the Mask/Enable Register. If the Conversion Ready feature is not set, the Alert pin will only respond to alert limit events based on the enabled alert function.

15.8 Digital Interface

The RTQ6056B-QA supports a general-purpose serial interface compatible with both I^2C bus and SMBus protocols for configuration and monitoring. The device supports fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 2940kHz) operation.

Table 2 summarizes the timing requirements for both fast mode and high-speed mode.

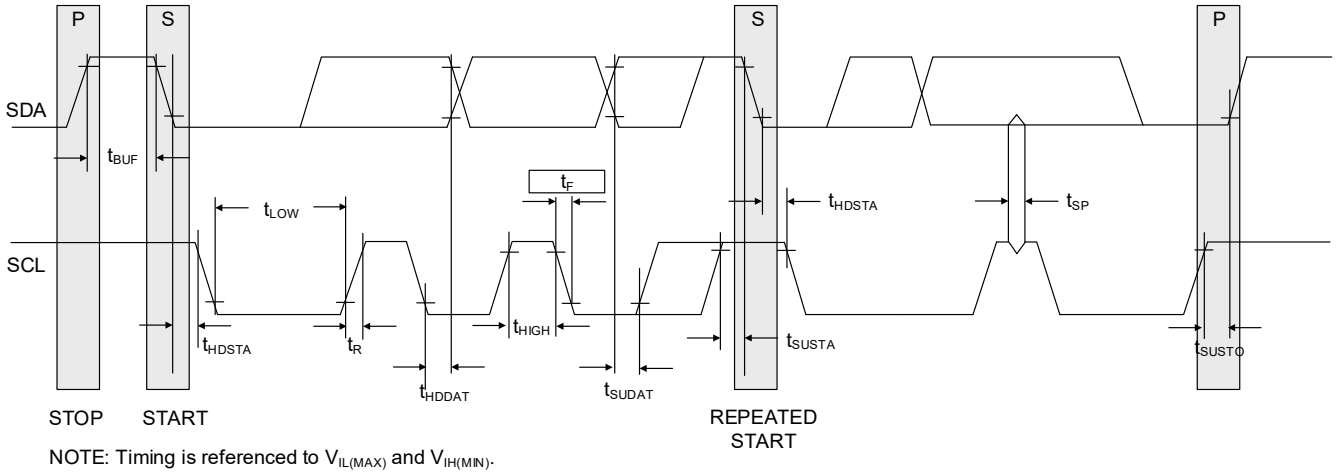


Figure 3. Bus Timing Diagram

Table 2. Timing Requirements

Parameter	Symbol	Fast Mode		High-Speed Mode		Unit
		Min	Max	Min	Max	
SCL Clock Rate	f_{SCL}	1	400	1	2940	kHz
Hold Time (Repeated) Start Condition. After this Period, the First Clock is Generated.	t_{HDSTA}	0.1	--	0.1	--	µs
Low Period of the SCL Clock	t_{LOW}	1.3	--	0.2	--	µs
High Period of the SCL Clock	t_{HIGH}	0.6	--	0.06	--	µs
Set-Up Time for a Repeated START Condition	t_{SUSTA}	0.1	--	0.1	--	µs
Data Hold Time	t_{HDDAT}	10	900	10	100	ns
Data Set-Up Time	t_{SUDAT}	100	--	20	--	ns
Set-Up Time for STOP Condition	t_{SUSTO}	0.1	--	0.1	--	µs
Bus Free Time between STOP and START Condition	t_{BUF}	0.6	--	0.16	--	µs
Clock Fall Time	t_F	--	300	--	80	ns
Data Fall Time	t_F	--	300	--	40	ns
Clock Rise Time	t_R	--	300	--	40	ns
Data Rise Time for $f_{SCL} \leq 100kHz$	t_R	--	1000	--	--	ns

15.9 Serial Bus Address

The system supports the configuration of 16 distinct slave addresses by utilizing two pins, A1 and A0, for address selection. This allows a maximum of 16 RTQ6056B-QA devices to be controlled on a single I^2C bus. The device samples the state of the A0 and A1 pins at every bus communication, so the address configuration must be set before any activity occurs on the interface. Table 3 lists the 16 possible slave addresses corresponding to the combination of the combination of the A1/A0 pins.

Table 3. Slave Address Selection

A1	A0	Slave Address	Slave Address (Hex)
GND	GND	1000000	40
GND	VS	1000001	41
GND	SDA	1000010	42
GND	SCL	1000011	43
VS	GND	1000100	44
VS	VS	1000101	45
VS	SDA	1000110	46
VS	SCL	1000111	47
SDA	GND	1001000	48
SDA	VS	1001001	49
SDA	SDA	1001010	4A
SDA	SCL	1001011	4B
SCL	GND	1001100	4C
SCL	VS	1001101	4D
SCL	SDA	1001110	4E
SCL	SCL	1001111	4F

15.10 Write Protocol

To write data to the RTQ6056B-QA, the master initiates communication with a START condition, followed by the 7-bit slave address with the $R\overline{W}$ bit set to low. After the RTQ6056B-QA acknowledges the address, the master sends a command byte that specifies the target register address. The device acknowledges the command byte and updates the internal register pointer to the selected register. The master then transmits two data bytes to be written to the addressed register, with the RTQ6056B-QA acknowledging receipt of each data byte. The write transaction is completed when the master sends a start or stop condition.

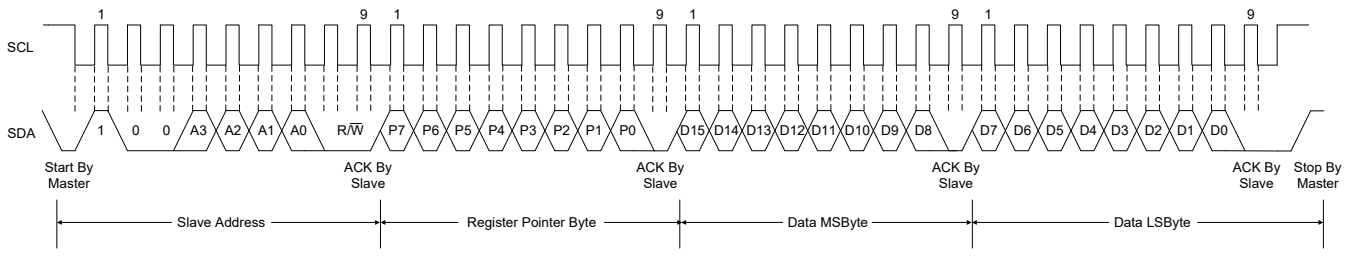


Figure 4. Timing Diagram for Write Word Format

15.11 Read Protocol

To initiate a read operation, the master begins with a START condition, followed by the 7-bit slave address and the R/$\overline{W}$ bit set to low. The register to be read is determined by the value currently stored in the register pointer, which is set during a previous write operation. To change the register pointer for a read operation, the master must first write the desired register address to the device.

This is accomplished by sending the slave address with the R/$\overline{W}$ bit (set to low), followed by the register pointer byte. No additional data bytes are required at this stage. The master then issues a start condition and sends the slave address with the R/$\overline{W}$ bit (set to high) to initiate the read command. The RTQ6056B-QA then transmits the most significant byte (MSB) of the selected register, followed by an Acknowledge (ACK) from the master. The device then transmits the least significant byte (LSB), which is also acknowledged by the master. The master may terminate the data transfer by issuing a Not-Acknowledge (NACK) after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are required, it is not necessary to resend the register pointer; the device retains the current register pointer value until it is updated by a subsequent write operation.

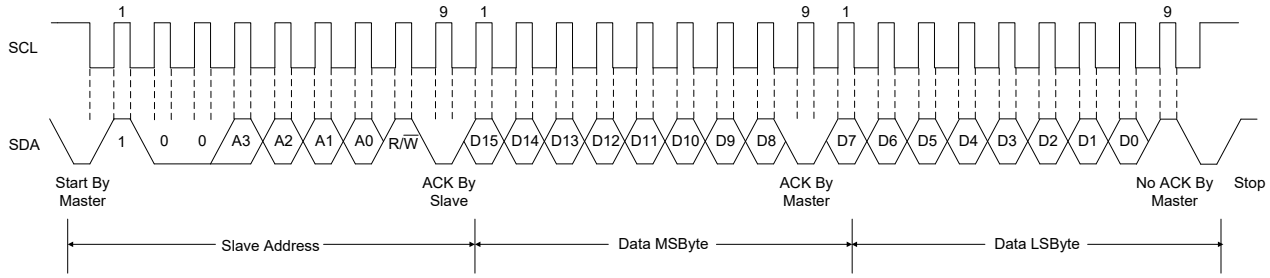


Figure 5. Timing Diagram for Read Word Format

15.12 SMBus Alert Response

The SMBus Alert Response feature provides a fast and efficient method for the master to identify devices that have generated an alert on a shared interrupt. When an interrupt is detected, the master broadcasts a receive byte request to the SMBus Alert Response slave address. Any slave device that has asserted an alert will attempt to respond by transmitting its own address onto the bus. If multiple devices respond simultaneously, standard bus arbitration rules apply: the device with the lower address wins arbitration and transmits its address, while other devices cease transmission and do not acknowledge. Devices that lose arbitration continue to hold their ALERT pin low until they are serviced. A successful reading of the alert response address by the master de-asserts the Alert indicator for the responding device.

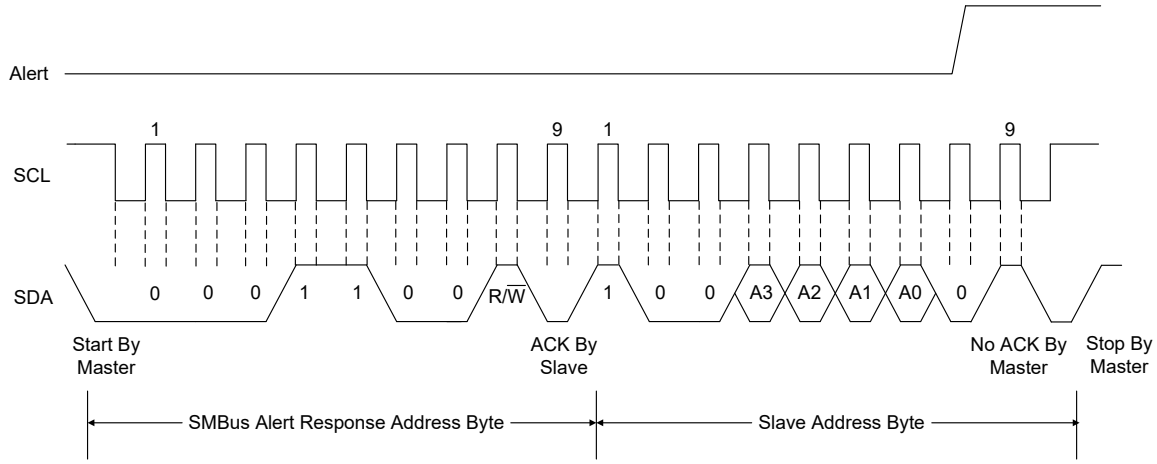


Figure 6. Timing Diagram for SMBus Alert

16 Application Information

(Note 11)

16.1 Power Up

The VS pin must exceed the Power-On Reset threshold (V_{POR}) of 2V to prevent the RTQ6056B-QA from entering power-on reset. When the supply voltage is below this threshold, the device enters power-on reset, which clears all register data.

16.2 Choosing the Sense Resistor

A high R_{SHUNT} value increases the voltage drop (IR loss) across the power source, so for minimal voltage loss, use the lowest R_{SHUNT} value. The full-scale sense voltage (V_{SENSE}) should remain within the device's input range of −81.9175mV to 81.92mV. For best performance with a 3.3V supply, select R_{SHUNT} to provide approximately 40mV to 60mV of sense voltage at the full-scale current.

At low current levels, a higher R_{SHUNT} value improves measurement accuracy, as offsets become less significant with larger sense voltages.

At high current levels, the I^2R loss in R_{SHUNT} can be significant. Consider both the resistor value and its power dissipation rating. Excessive heating may cause the resistor value to drift, affecting accuracy. The RTQ6056B-QA 's high precision (V_{OS} 10μV (maximum) and Gain Error 0.12% (maximum)) allows the use of small sense resistors, reducing power dissipation and minimizing hot spots.

16.3 Filtering and Input Considerations

The RTQ6056B-QA provides several methods to reduce input noise, such as configurable conversion time and averaging mode via register (00h). However, to prevent the device from damaging conditions, such as load dumps, reverse battery connection, fast load switching, and inductive kickback voltages, input filtering and voltage clamping schemes are recommended.

Figure 6 shows the recommended schematic for input filtering. Proper input filtering ensures that current noise is not amplified, allowing the RTQ6056B-QA to deliver a cleaner signal to the ADC without the need for output filtering, which could otherwise load down the ADC.

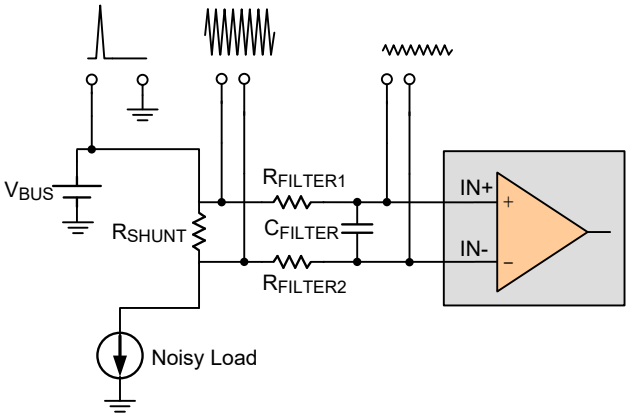


Figure 7. Input Filter

If the selected device's Absolute Maximum Common-Mode Voltage rating is less than the system's maximum expected voltage surge, input protection is required. In such cases, it is recommended to use transient voltage suppression (TVS) diodes or Zener diodes at the inputs, in combination with passive components, to safeguard the current sensor from voltage transients. Figure 7 shows an example of a cost-optimized current sensor input protection circuit.

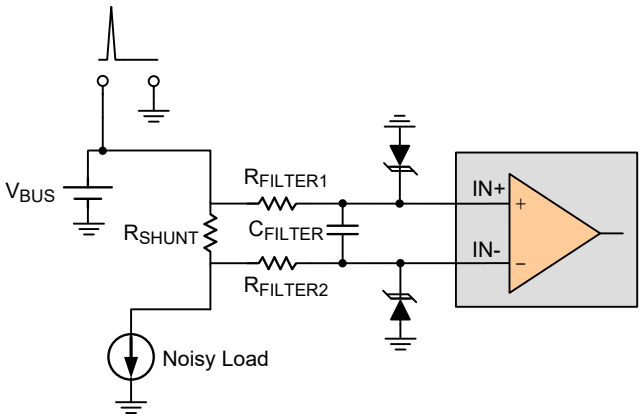


Figure 8. Input Protection Circuit in the RTQ6056B-QA

16.4 Total Error Analysis

To optimize system design, it is important to analyze the contribution of each error source affecting sense voltage measurements. The primary factors influencing sense voltage errors include:

- The tolerance of the shunt resistor (R_{SHUNT})
- Sense offset voltage, V_{S_OS}. When the sense voltage is low, especially at low load currents and with small shunt resistances, the error is dominated by the input offset error.
- Gain Error, GE%
- Power Supply Rejection Ratio (PSRR) of offset voltage
- Common-Mode Rejection Ratio (CMRR)
- The offset voltage caused by input bias current
- Nonlinearity Error (NLIN%)

16.5 Maximum Output Error Estimation

The section provides an example of estimating the maximum output voltage error. With a system bus voltage IN+ = 36V, a supply voltage V_S = 5V, a shunt resistor with 1% accuracy and 2mΩ resistance, and the load current is 25A. The design goals can be set by calculating the maximum output voltage errors as follows:

$$V_{OS\_err} = \frac{V_{OS(MAX)}}{V_{SENSE}} \times 100\% = \frac{10\mu V}{2m\Omega \times 25A} \times 100\% = 0.02\%$$

where

Input offset voltage error:

The rate of the offset error to the total error can be estimated directly from the Electrical Characteristics table. The input offset voltage is 10μV at T_A = 25°C.Sense Voltage Gain Error

According to the electrical characteristics, the maximum gain error is 1%.

16.6 Power Supply Rejection Ratio (PSRR) Error

The PSRR additional error caused by deviations in the supply voltage from the specified values. The RTQ6056B-QA specifies the input offset voltage at V_S = 3.3V. If the actual supply voltage differs, an additional error may occur. The maximum PSRR is specified as 2.5μV/V. The PSRR error can be calculated as:

$$PSRR\_err = \frac{\left|V_{S\_DS} - V_{S\_SYS} \times PSRR\right|}{V_{SENSE}} \times 100\%$$

$$= \frac{\left|3.3 - 5\right| \times 2.5\frac{\mu V}{V}}{2m\Omega \times 25A} \times 100\% = 0.0085\%$$

16.7 Common-Mode Rejection Ratio (CMRR) Error

The CMRR error reflects the influence of common-mode voltage variations on the input offset. The RTQ6056B-QA specifies a minimum CMRR of 126dB (0.501μV/V), with the offset voltage specified at a common-mode voltage of 12 V. To calculate the actual common-mode error at the system bus voltage:

$$126dB \text{ can be converted to } \mu V/V = \frac{1}{10^{\left(\frac{126dB}{20}\right)}} \times 10^6 \times \frac{\mu V}{V} = 0.501\frac{\mu V}{V}$$

$$CMRR\_err = \frac{\left|V_{CM\_DS} - V_{CM\_SYS}\right| \times CMRR}{V_{SENSE}} \times 100\% = \frac{\left|12 - 36\right| \times 0.501\frac{\mu V}{V}}{2m\Omega \times 25A} \times 100\% = 0.024\%$$

16.8 Input Bias Current Error

The input bias current flows into a shunt resistor to cause an additional offset. This error is calculated with respect to the ideal voltage across the sense voltage.

$$I_{B\_err} = \frac{I_B \times R_{SHUNT}}{V_{SENSE}} \times 100\% = \frac{35\mu A \times 2m\Omega}{2m\Omega \times 25A} \times 100\% = 0.0001\%$$

16.9 Nonlinearity Error

In an ideal scenario, the voltage gain remains constant over entire sense voltage range. However, in real-world applications, the voltage gain is not exactly constant, resulting in nonlinearity errors. For the RTQ6056B-QA, the nonlinearity error is specified as 0.1% over a sense voltage range of 20mV to 80mV.

16.10 Total Error

The equation below can be used to calculate the worst case of total error.

$$Total\_err = \sqrt{(GE\%)^2 + (R\%)^2 + (V_{OS\_err})^2 + (PSR\_err)^2 + (CMR\_err)^2 + (I_{B\_err})^2 + (NLIN\%)^2}$$

$$= \sqrt{(0.12\%)^2 + (1\%)^2 + (0.05\%)^2 + (0.021\%)^2 + (0.06\%)^2 + (0.00035\%)^2 + (0.045\%)^2}$$

$$= 1.01\%$$

16.11 Layout Guidelines

- For optimal performance, use a Kelvin (4-wire) connection to the sense resistor. Connect the input pins (IN+ and IN-) to the sense resistor using separate traces for current and voltage sensing.
- PCB trace resistance between the sense resistor and the IN+ and IN- pins can degrade the measurement accuracy. Place the sense resistors as close as possible to the RTQ6056B-QA and avoid using minimum-width PCB traces for these connections.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

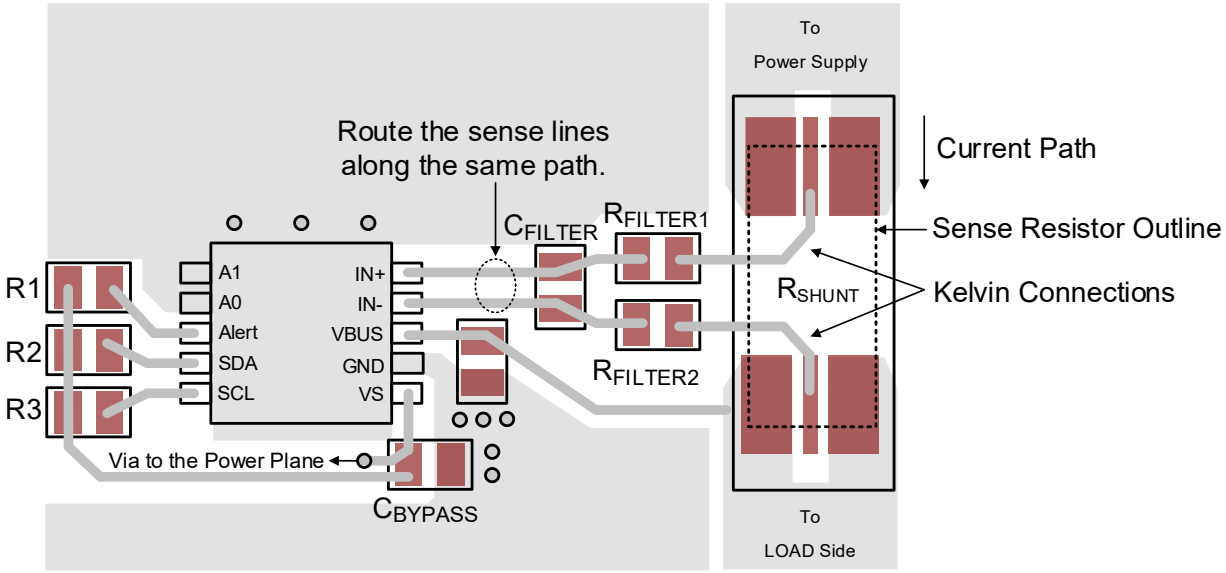


Figure 9. PCB Layout Guide

Note 11. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Functional Register Description

17.1 Register Map

Table 4 shows the summary of the RTQ6056B-QA registers. All registers are two bytes in length and are accessed via the I^2C interface.

Table 4. The Summary of the RTQ6056B-QA Registers

CMD CODE	COMMAND Name	Access	Command Description	Default Value
00h	Configuration	R/W	Operating mode configuration, conversion times and averaging setting	4127h
01h	Sense Voltage	R	Sense voltage measurement data.	0000h
02h	Bus Voltage	R	Bus voltage measurement data.	0000h
03h	Power	R	Calculated power data	0000h
04h	Current	R	Calculated current data	0000h
05h	Calibration	R/W	Current Calibration	0000h
06h	Mask/Enable	R/W	Alert configuration	0000h
07h	Alert Limit	R/W	Limit threshold setting	0000h
FEh	Manufacturer ID	R	Manufacturer identification number.	1214h
FFh	Die ID	R	Die identification number.	2260h

Configuration Register (00h)

Description: The Configuration Register settings control the operating modes for the device. This register controls the conversion time settings for both the sense and bus voltage measurements as well as the averaging mode used. The operating mode that controls what signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration Register halts any conversion in progress until the write sequence is completed resulting in a new conversion starting based on the new contents of the Configuration Register (00h). This halt prevents any uncertainty in the conditions used for the next completed conversion.

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	RST	X	X	X	AVG2	AVG1	AVG0	VBUSCT2	VBUSCT1	VBUSCT0	VSENCT2	VSHNCT1	VSENCT0	MODE3	MODE2	MODE1
Value	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

Bits	Name	Description
15	Reset Bit (RST)	Set this bit to '1' to reset all registers as the default value. This bit self-clears.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>11:9</td><td>Averaging Mode (AVG)</td><td>Determine the number of samples that are collected and averaged. Table 5 shows all the AVG bit settings and related number of averages for each bit setting.
Table 5. AVG Bit Settings [11:9] Combinations
<table>
<tr><th>Averaging</th><th>AVG2</th><th>AVG1</th><th>AVG0</th></tr>
<tr><td>1 (default)</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>4</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>16</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>64</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>128</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>256</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>512</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1024</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>8:6</td><td>Bus Voltage Conversion Time (VBUSCT)</td><td>Set the conversion time for the bus voltage measurement. Table 6 shows the VBUSCT bit options and related conversion times for each bit setting.
Table 6. VBUSCT Bit Settings [8:6] Combinations
<table>
<tr><th>Conversion Time (μs)</th><th>VBUSCT2</th><th>VBUSCT1</th><th>VBUSCT0</th></tr>
<tr><td>139</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>203</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>269</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>525</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1037 (default)</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>2061</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4109</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>8205</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>5:3</td><td>Sense Voltage Conversion Time (VSENCT)</td><td>Set the conversion time for the sense voltage measurement. Table 7 shows the VSENCT bit options and related conversion times for each bit setting.
Table 7. VSENCT Bit Settings [8:6] Combinations
<table>
<tr><th>Conversion Time (μs)</th><th>VSENCT2</th><th>VSENCT1</th><th>VSENCT0</th></tr>
<tr><td>139</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>203</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>269</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>525</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1037 (default)</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>2061</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4109</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>8205</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
</table>

Bits	Name	Description
2:0	Operating Mode (MODE)	Select continuous, triggered, or power-down mode of operation. These bits default to continuous sense and bus measurement mode. The mode settings are shown in Table 8.

Table 8. Mode Settings [2:0] Combinations

Mode Setting	MODE3	MODE2	MODE1
Shutdown Mode	0	0	0
Sense Voltage, Triggered	0	0	1
Bus Voltage, Triggered	0	1	0
Sense and Bus Voltage, Triggered	0	1	1
Shutdown Mode	1	0	0
Sense Voltage, Continuous	1	0	1
Bus Voltage, Continuous	1	1	0
Sense and Bus Voltage, Continuous (default)	1	1	1

Sense Voltage Register (01h)

Description: The Sense Voltage Register stores the current sense voltage reading, V_{SENSE}. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	SIGN	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	Sign Bit (SIGN)	SIGN Bit 0: Positive value 1: Negative value
14:0	Sense Voltage	**Example**: For a value of V_{SENSE} = –80mV: 1. Take the absolute value: 80mV 2. Translate this number to a whole decimal number (80mV ÷ 2.5μV) = 32000 3. Convert this number to binary = 0111 1101 0000 0000 4. Complement the binary result = 1000 0010 1111 1111 5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h If averaging is enabled, this register displays the averaged value. Full-scale range = 81.92 mV (decimal = 32767); LSB: 2.5μV.

Bus Voltage Register (02h)																
Description: The Bus Voltage Register stores the most recent bus voltage reading, VBUS. If averaging is enabled, this register displays the averaged value.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Bus Voltage	Full-scale range = 40.96V (decimal = 32767); LSB: 1.25mV. Note that Bit 15 is always zero because bus voltage can only be positive.

Power Register (03h)																
Description: If averaging is enabled, this register displays the averaged value. The Power Register LSB is internally programmed to equal 25 times the programmed value of the Current_LSB. The Power Register records power in watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Power	The power is always positive value.

Current Register (04h)																
Description: If averaging is enabled, this register displays the averaged value. The value of the Current Register is calculated by multiplying the decimal value in the Sense Voltage Register with the decimal value of the Calibration Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	SIGN	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	Sign Bit (SIGN)	SIGN Bit 0: Positive value 1: Negative value
14:0	Current	The current value

Calibration Register (05h)																
Description: This register provides the device with the value of the sense resistor that was present to create the measured differential voltage. It also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB. This register is also suitable for use in overall system calibration. See the Programming the Calibration Register for additional information on programming the Calibration Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Calibration	Bit 15 is always zero.

Mask/Enable (06h)																
Description: The Mask/Enable Register selects the function that is enabled to control the Alert pin as well as how that pin functions. If multiple functions are enabled, the highest significant bit position the Alert Function (Bit 15-Bit 11) takes priority and responds to the Alert Limit Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	SOVL	SUVL	BOVL	BUVL	OPL	CNVR	X	X	X	X	X	AFF	CNRF	OVF	APO	ALE
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	Sense Overvoltage Limit (SOVL)	Setting this bit high configures the Alert pin to be asserted if the sense voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
14	Sense Undervoltage Limit (SUVL)	Setting this bit high configures the Alert pin to be asserted if the sense voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
13	Bus Overvoltage Limit (BOVL)	Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
12	Bus Undervoltage Limit (BUVL)	Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
11	Over-Power Limit (OPL)	Setting this bit high configures the Alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register.
10	Conversion Ready (CNVR)	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.

Bits	Name	Description
4	Alert Function Flag (AFF)	While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.
3	Conversion Ready Flag (CNRF)	Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1. Writing to the Configuration Register (except for Power-Down selection) 2. Reading the Mask/Enable Register
2	Math Overflow Flag (OVF)	This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that the current and power data may be invalid.
1	Alert Polarity Bit (APO)	1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default)
0	Alert Latch Enable (ALE)	1 = Latch enabled 0 = Transparent (default) When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and the Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and the Alert Flag bit remains active following a fault until the Mask/Enable Register has been read.

Alert Limit Register (07h)

Description: The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded.

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Alert Limit	Store the alert limit values.

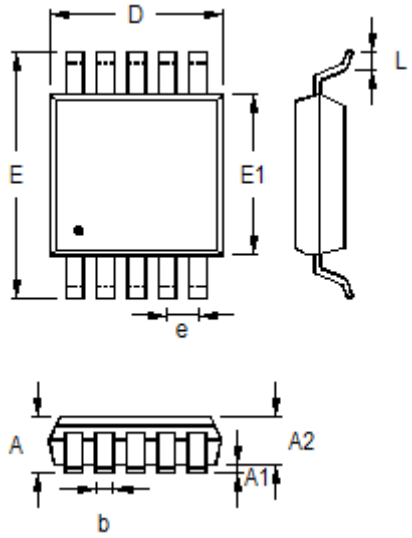
Manufacturer ID Register (FEh)																
Description: The Manufacturer ID Register stores a unique identification number for the manufacturer.																
Bit .	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	0

Bits	Name	Description
15:0	Manufacturer ID	Store the manufacturer identification bits

Die ID Register (FFh)																
Description: The Die ID Register stores a unique identification number and the revision ID for the die.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	0	0	1	0	0	0	1	0	0	1	1	0	0	0	0	0

Bits	Name	Description
15:4	Die ID	Store the device identification bits
3:0	Die Revision ID	Store the device revision identification bits

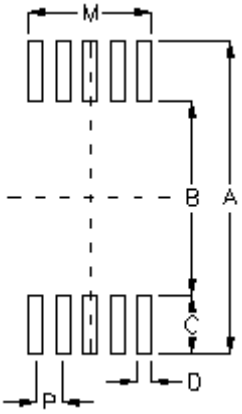
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.170	0.270	0.007	0.011
D	2.900	3.100	0.114	0.122
e	0.500		0.020	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

10-Lead MSOP Plastic Package

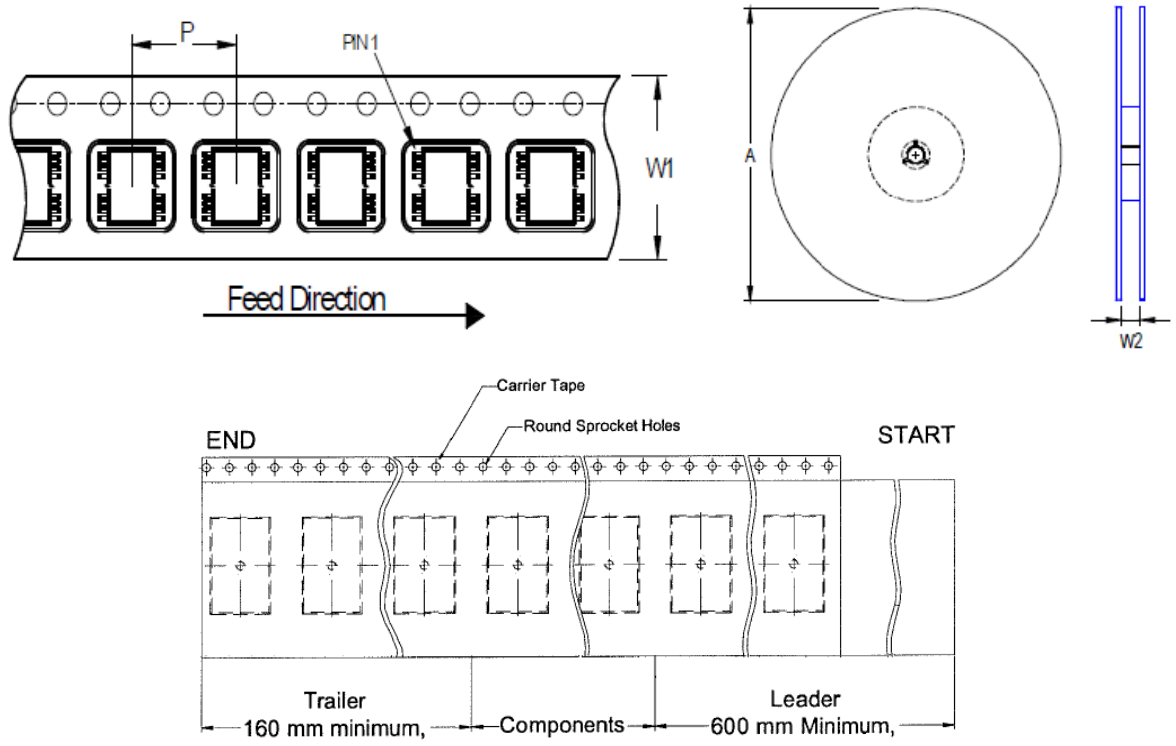
19 Footprint Information



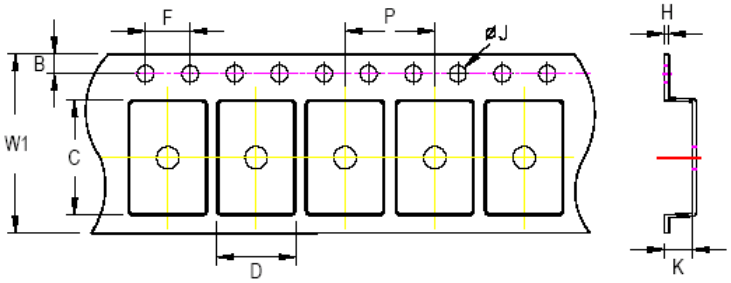
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
MSOP-10	10	0.50	5.80	3.60	1.10	0.25	2.25	±0.10

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
MSOP-10	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 1.0mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.5mm	1.7mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
MSOP-10	13”	2,500	Box G	1	2,500	Carton A	6	15,000

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
00	2025/11/04	First Edition