RICHTEK®

RTQ6136

60V, 16-Bit Bi-Directional Current and Power Monitor with I²C Interface for High-Side or Low-Side Measurement

1 General Description

The RTQ6136 is a high-accuracy current-sense monitor with an I²C and SMBus-compatible interface. The device delivers comprehensive system data by reading the load current and power.

The device monitors both the voltage drop across the sense resistor and the bus voltage, converting them into current in amperes and power in watts through an internal analog-to-digital converter (ADC). Programmable calibration, adjustable conversion times, and an averaging function are also built in for enhanced design flexibility.

The RTQ6136 provides a wide operating temperature range from –40°C to 125°C and operates with an input voltage range from 2.5V to 5.5V. The device can sense current on common-mode bus voltages ranging from –0.3V to 60V.

The RTQ6136 is available in the TSOT-28(COL) package.

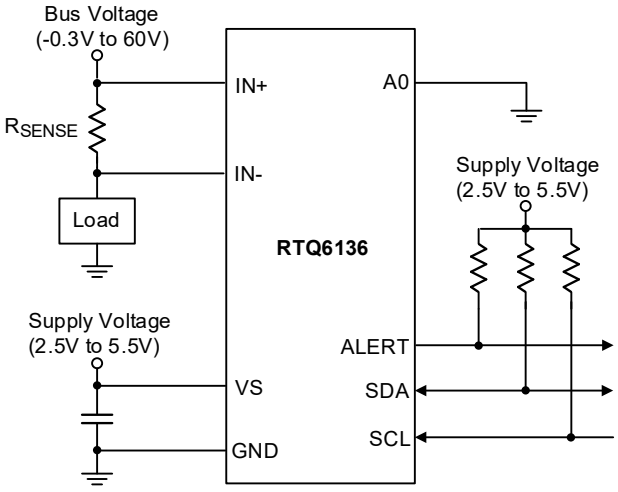
2 Features

- **I²C and SMBus-Compatible Interface**
- **Bi-Directional Current Sensing, Available for High-Side or Low-Side Sensing**
- **Input Voltage Range: 2.5V to 5.5V**
- **Common-Mode Input Voltage: -0.3V to 60V**
- **Current Monitoring Accuracy**
  - **16-bit ADC Resolution**
  - **0.1% Gain Error (Maximum)**
  - **10μV Offset (Maximum)**
- **Over/Under Current, Over/Under Voltage, and Overpower Alerts**
- **60V Common Mode Voltage, Suitable for 48V Server Systems**
- **Two Device Address Options, Each with Four Pin-Selectable I²C Slave Addresses**
- **Junction Temperature Range: –40°C to 125°C**
- **TSOT-28(COL) Package**

3 Applications

- Servers
- Network Equipment
- Notebook Computers
- POE Devices

4 Simplified Application Circuit



5 Ordering Information

5.1 Product Number Information

RTQ6136□-□□□

Packing
A: Pin 1 Orientation
(Quadrant 3, Follow EIA-481)

Device Option
Refer to Product Selection Table

Product Grade
T: Industrial Grade

Package Type(1)
D: TSOT-28(COL)

Note 1.

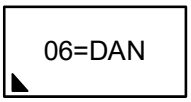
Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5.2 Product Selection Table

A0 Pin Configuration	RTQ6136D-TAA	RTQ6136D-TBA
GND	0x40	0x48
VS	0x41	0x49
SDA	0x42	0x4A
SCL	0x43	0x4B

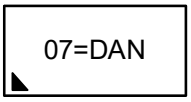
6 Marking Information

RTQ6136D-TAA



06= : Product Code
DAN : Date Code

RTQ6136D-TBA

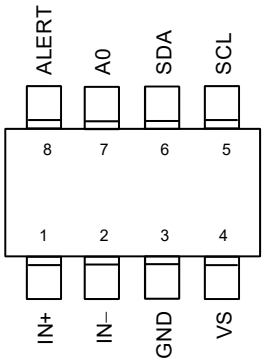


07= : Product Code
DAN : Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)

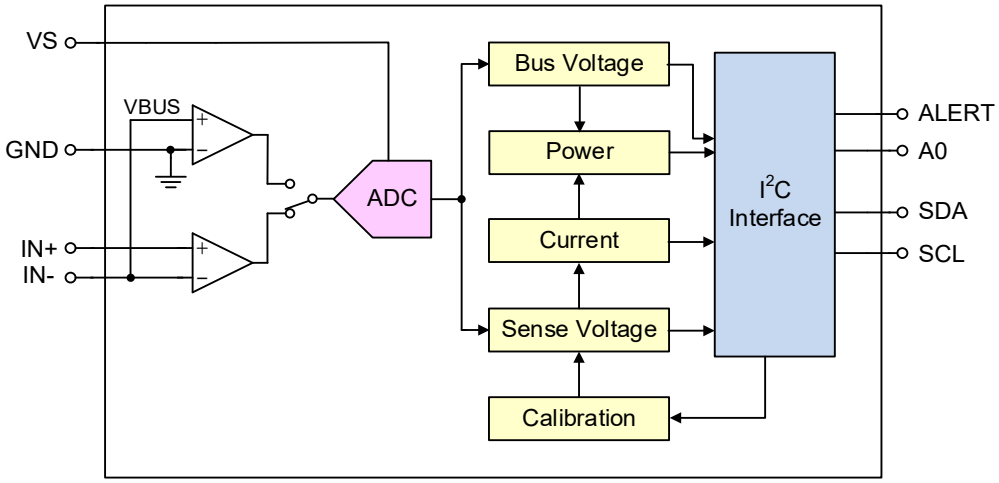


TSOT-28(COL)

8 Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	IN+	Analog Input	Positive current-sensing input. Connect this pin to the power side of an external sense resistor.
2	IN-	Analog Input	Negative current-sensing input. Connect this pin to the load side of an external sense resistor. The bus voltage is measured from this pin to ground.
3	GND	Ground	Ground.
4	VS	Power	Power supply, 2.5V to 5.5V. Connect a 0.1μF capacitor as close to the VS pin as possible.
5	SCL	Digital Input	Serial clock interface.
6	SDA	Digital IN/OUT	Bi-directional serial data interface.
7	A0	Digital Input	Address pin. Connect the pin to GND, SCL, SDA, or VS.
8	ALERT	Digital Output	Multi-functional alert, open-drain output.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, V_S ---------- –0.3V to 6V
- Common Mode (V_{IN+} + V_{IN-})/2, V_{CM} ---------- –0.3V to 75V
- Differential Mode (V_{IN+} - V_{IN-}), V_{SENSE} ---------- –26V to 26V
- Other Pins ---------- –0.3V to 6V
- Input Current into Any Pin, I_{IN} ---------- 5mA
- Open-Drain Digital Output Current, I_{OUT} ---------- 10mA
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Susceptibility

(Note 3)

- HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Common-Mode Input Voltage, V_{CM} ---------- –0.3V to 60V
- Operating Supply Voltage, V_S ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5)

Thermal Parameter		TSOT-28(COL)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	130.27	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	80.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	28.8	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

14 Electrical Characteristics

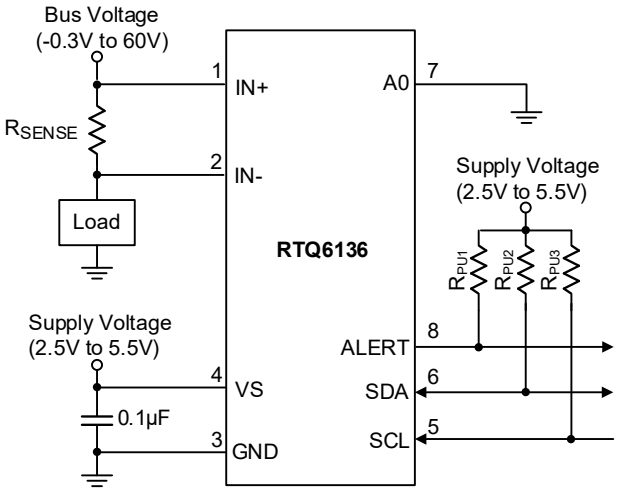
(T_A = 25°C, V_S = 3.3V, V_{IN-} = 12V, V_{SENSE} = (V_{IN+} – V_{IN-}) = 0mV, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
Common-Mode Rejection	CMRR	−40°C ≤ T_A ≤ 125°C 0V ≤ VCM ≤ 60V	136	150	--	dB
Sense Voltage Input Range	VSENSE	ADCRANGE = 0	-81.9175	--	81.92	mV
		ADCRANGE = 1	-20.4794	--	20.48	mV
Sense Offset Voltage, RTI	V_{S_OS}	VCM = 12V	--	±1	±10	μV
Sense Offset Voltage, RTI vs Temperature		−40°C ≤ T_A ≤ 125°C	--	±5	±25	nV/°C
Bus Offset Voltage, RTI	V_{B_OS}		--	±1	±7.5	mV
Bus Offset Voltage, RTI vs. Temperature		−40°C ≤ T_A ≤ 125°C	--	±10	±30	μV/°C
Sense Offset Voltage, RTI vs. Power Supply	PSRR	2.5V ≤ VS ≤ 5.5V	--	--	±10	μV/V
Bus Offset Voltage, RTI vs. Power Supply (Note 6)	PSRR	2.5V ≤ VS ≤ 5.5V	--	--	±5	mV/V
VBUS Input Impedance			--	1.05	--	MΩ
Input Leakage		(IN+ pin), (IN– pin), Shutdown Mode	--	0.1	5	nA
Input Bias Current	I_B	(IN+ pin), (IN– pin), Current Measurement Mode	--	0.1	10	nA
DC Accuracy						
Differential Input Impedance (IN+ to IN-)		Sense or Current Measurement Modes, V_{IN+} – V_{IN-} < 82mV	--	38	--	kΩ
ADC Native Resolution			--	16	--	Bits
1 LSB Step Size		Sense Voltage, ADCRANGE = 0	--	2.5	--	μV
		Sense Voltage, ADCRANGE = 1	--	625	--	nV
		Bus Voltage	--	1.6	--	mV
ADC Conversion Time, Continuous Mode	t_{CT}	bit = 000	129	136	143	μs
		bit = 001	190	200	210	μs
		bit = 010	251	264	277	μs
		bit = 011	494	520	546	μs
		bit = 100	984	1036	1088	μs
		bit = 101	1957	2060	2163	μs
		bit = 110	3903	4108	4313	μs
		bit = 111	7794	8204	8614	μs
Sense Voltage Gain Error			--	±0.015	±0.1	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Sense Voltage Gain Error vs Temperature		−40°C ≤ T_A ≤ 125°C	--	--	30	ppm/°C
Bus Voltage Gain Error			--	±0.015	±0.1	%
Bus Voltage Gain Error vs Temperature			--	--	30	ppm/°C
Nonlinearity			--	±1.5	±6	m%
Differential Nonlinearity (Note 6)			--	±0.1	--	LSB
Power Supply						
Operating Supply Range	V_S		2.5	--	5.5	V
Quiescent Current	I_Q		--	300	350	µA
		−40°C ≤ T_A ≤ 125°C	--	--	450	µA
	I_{Q_SD}	Power-down (Shutdown) Mode	--	3.3	4.9	µA
Power-On Reset Threshold	V_{POR}		--	1.3	--	V
SMBus						
SMBus Timeout			--	28	35	ms
DIGITAL INPUT/OUTPUT						
Input Capacitance (Note 6)			--	3	--	pF
SCL, SDA High-Level Input Threshold Voltage	V_{IH}		0.9	--	5.5	V
Hysteresis	V_{HYS}		--	70	--	mV
SCL, SDA Low-Level Input Threshold Voltage	V_{IL}		--	--	0.4	V
Output Low Level for SDA	V_{OL}	I_{OL} = 3mA	--	--	0.3	V
Leakage Input Current	I_{LK}	0 ≤ Input Pin Voltage ≤ V_S	-1	--	1	µA

Note 6. Guaranteed by design.

15 Typical Application Circuit

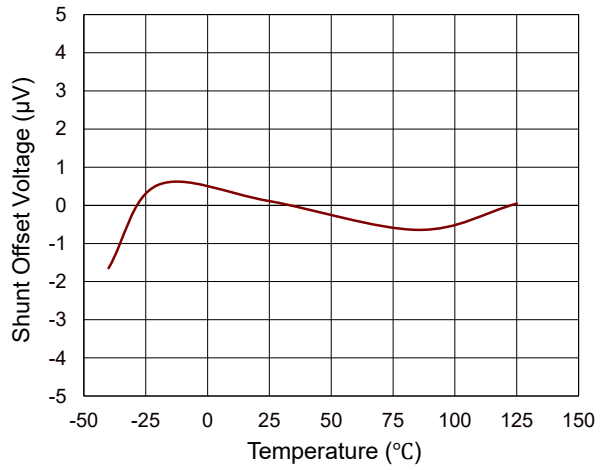


Note 7. All the input and output capacitors are the suggested values, referring to the effective capacitances and subject to any de-rating effects, such as DC Bias.

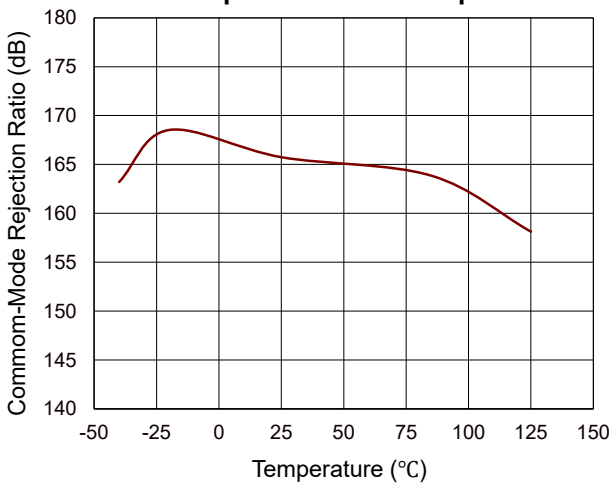
16 Typical Characteristics

(T_A = 25°C, V_S = 3.3V, V_{CM} = 12V, V_{SENSE} = (V_{IN+} – V_{IN-}) = 0mV, unless otherwise noted.)

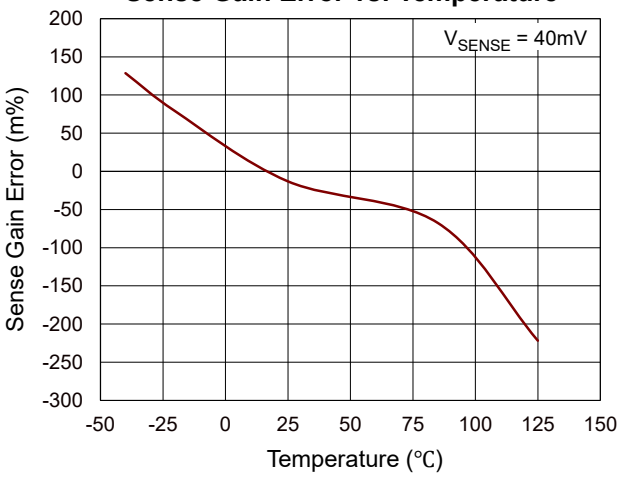
Sense Input Offset Voltage vs. Temperature



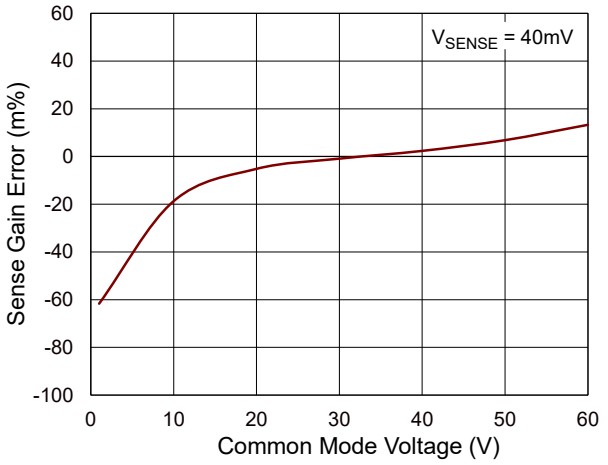
Sense Input CMRR vs. Temperature



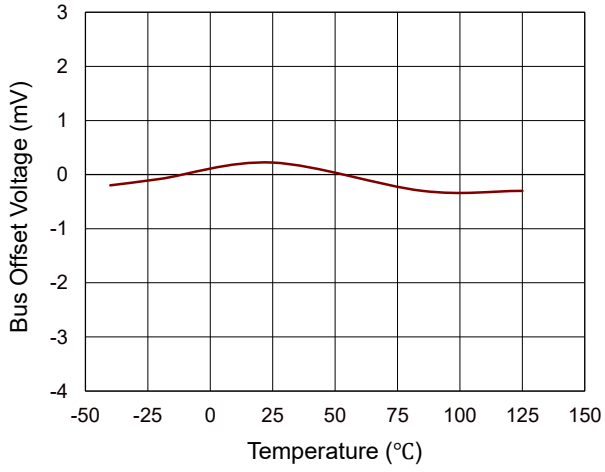
Sense Gain Error vs. Temperature



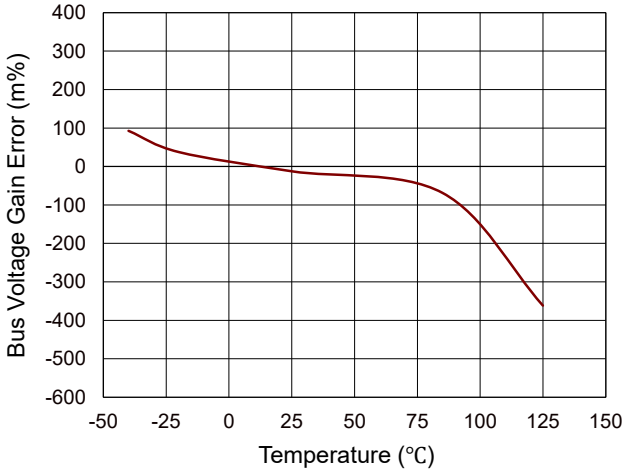
Sense Gain Error vs. Common-Mode Voltage



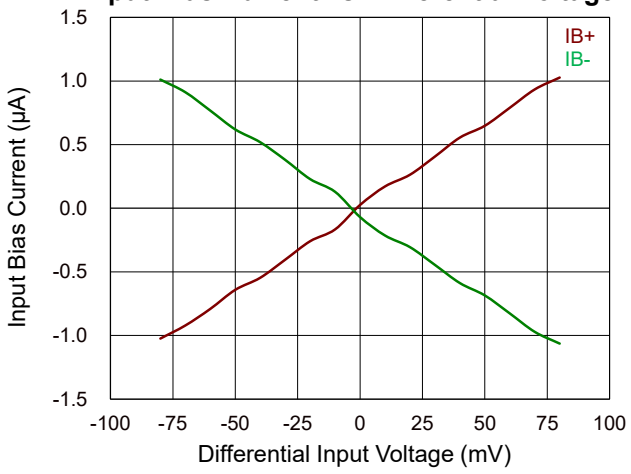
Bus Offset Voltage (V_{IN-}) vs. Temperature



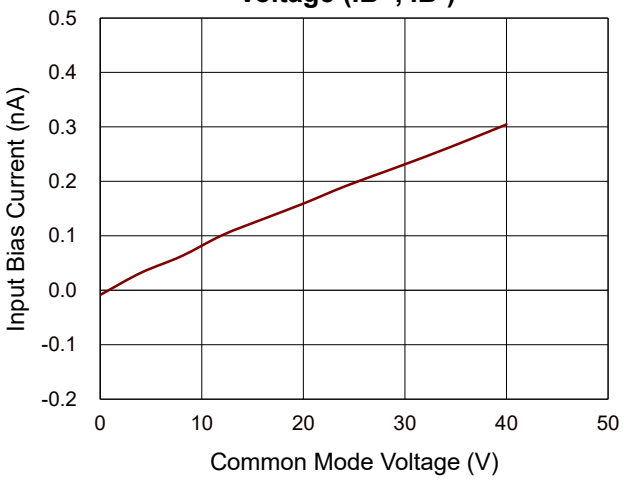
Bus Voltage (V_{IN-}) Gain Error vs. Temperature



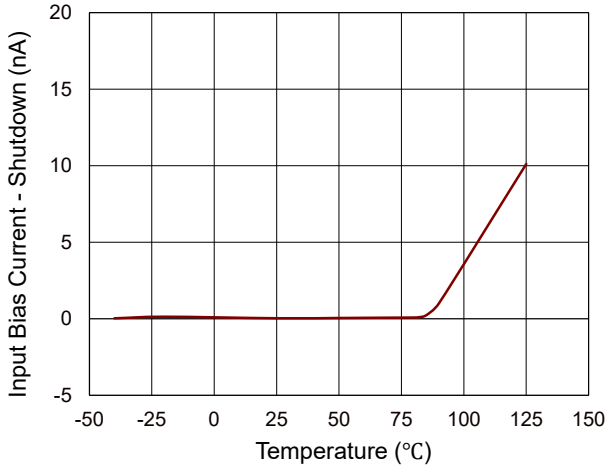
Input Bias Current vs. Differential Voltage



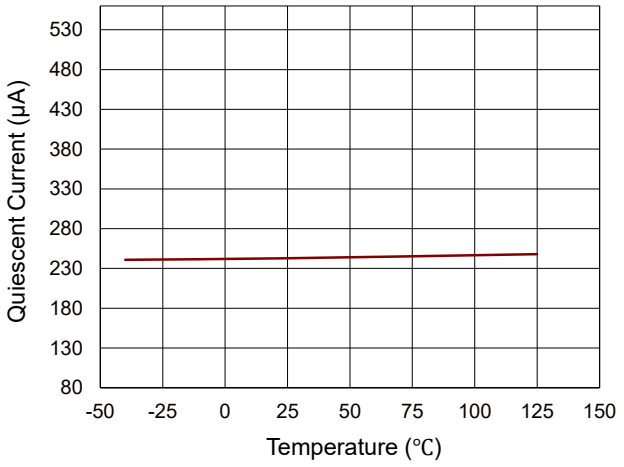
Input Bias Current vs. Common-Mode Voltage (IB+, IB-)



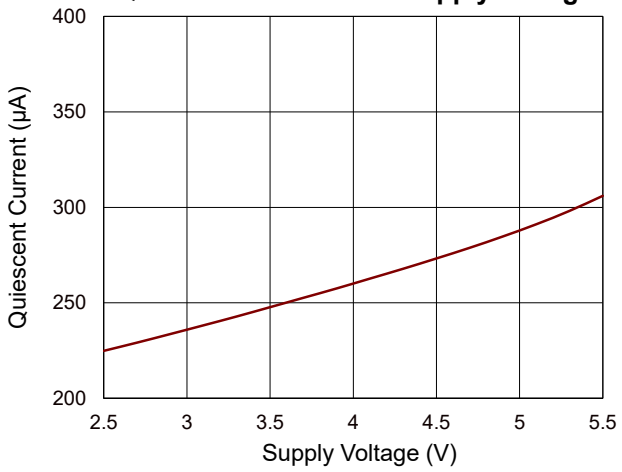
Input Bias Current vs. Temperature (Shutdown)



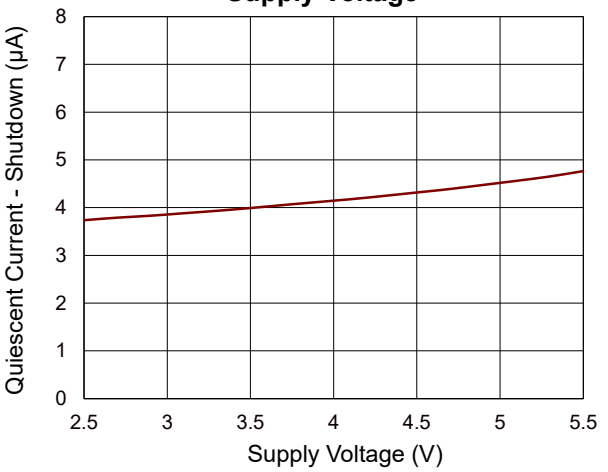
Quiescent Current vs. Temperature

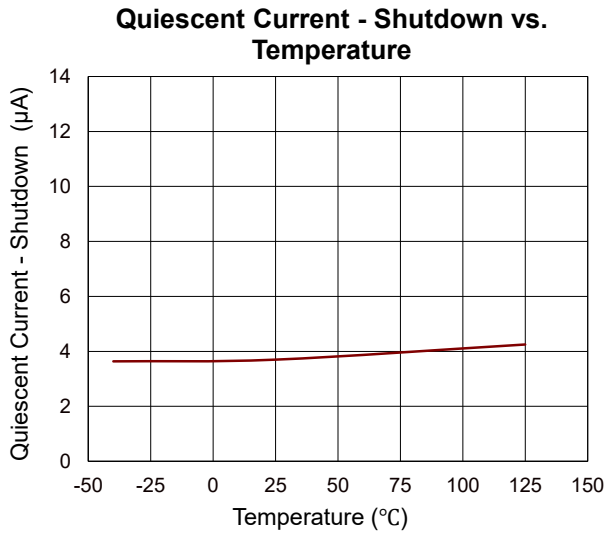


Quiescent Current vs. Supply Voltage



Quiescent Current - Shutdown vs. Supply Voltage





17 Operation Description

The device is a digital current-sense amplifier with an I²C/SMBus-compatible interface. It reports the measured current and supports programmable out-of-range limits to assert alerts when the current leaves the normal operating range. The integrated ADC supports configurable averaging modes and can be set for continuous or triggered conversions. See the Functional Register Description section for detailed register descriptions for configuration and readout.

17.1 Feature Description

17.1.1 Integrated Analog-to-Digital Converter (ADC)

The device integrates a low-offset, 16-bit delta-sigma (ΔΣ) ADC that is multiplexed to handle both sense voltage and bus voltage measurements. Bus voltage measurements are taken at the IN– pin with respect to GND, while the sense voltage measurement is a differential reading between the IN+ and IN– pins of the voltage developed across the sense resistor as the load current flows. The sense voltage path is designed to maintain a low offset and minimal gain error, which enhances light load accuracy and enables reliable detection of small voltage drops. This capability allows the use of lower-value sense resistors, helping reduce power loss and improve overall system efficiency.

There are no special power supply sequencing requirements because the bus common-mode voltage at the IN+/IN– pins and the supply voltage on the VS pin are independent; the bus common-mode voltage may be present while VS is off, and vice versa.

17.1.2 Internal Measurement and Calculation Engine

Figure 1 illustrates the device's internal measurement sequence for a single channel. The values in the current and power registers are computed from the sense and bus voltage measurements and are not directly tied to the ADC conversion time. These register values are updated after each measurement cycle is completed. With averaging enabled, the registers update only after the configured averaging count is completed. Fault comparators are evaluated immediately after each conversion or calculation, independent of the averaging count. Shorter conversion times yield a faster alert response but lower effective resolution; longer conversion times result in a slower response but improve noise performance. The Conversion Ready flag asserts at the end of the conversion once the configured averaging count is reached.

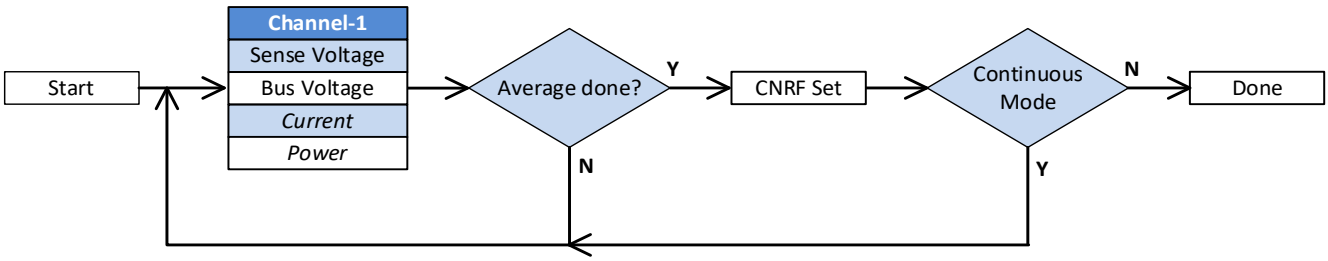


Figure 1. Internal Measurement and Calculation Engine – Flow Diagram

In Figure 1, the italicized registers indicate computed values that are generated in the background and are independent of the ADC conversion timing. These registers update once the configured averaging count is reached. Fault comparators are evaluated immediately after each conversion result, and averaged values do not generate alerts. The current is derived from the sense-voltage measurement and the value in the CALIBRATION register;

the power calculation uses the previous current result and the latest bus-voltage measurement. If the value in the CALIBRATION register is zero, the current and power registers will report zero. These background calculations do not increase the overall conversion time.

17.1.3 Low Bias Current

During current measurements, the device exhibits a very low input bias current, which provides multiple advantages. First, a lower bias current reduces the device's own supply current in both active and shutdown states. Second, it enables the use of input RC filters ahead of the ADC to reject high-frequency noise with minimal loss of accuracy, whereas traditional digital current sense monitors typically suffer a larger accuracy penalty when input filters are added. Third, the low input bias current permits the use of a larger sense resistor to improve small-current accuracy, enabling measurements below 1mA.

The input bias current is minimal at a zero load current. As the load current increases, the differential voltage across the sense resistor increases, and the bias current rises accordingly.

The device maintains a low input bias current only during current measurements. During bus-voltage measurements, the impedance at the IN– decreases because it is connected to an internal resistor divider of approximately 1MΩ. Therefore, configuring the ADC to measure only current keeps the device in the low-bias operating condition.

17.1.4 Low Voltage Supply and Wide Common-Mode Voltage Range

The device supports a 2.5V to 5.5V supply. The ability to operate at a minimum of 2.5V operation enables deployment on 2.5V rails. The input common-mode range extends to 60V, enabling current measurements on high-voltage rails independent of the supply voltage. This wide common-mode capability permits operation even when the bus common-mode voltage exceeds the device's supply voltage.

17.1.5 ALERT Pin

The device provides a single MASK_ENABLE register (06h) that programs the ALERT pin to either (a) respond to one user-selected event or (b) indicate a conversion-ready. One of five alert functions can be selected from this register; additionally, the Conversion Ready Mask bit (CNVR_MASK, MASK_ENABLE register) in the same register configures whether the ALERT pin also reports conversion completion. A threshold for the monitored function is written to the ALERT_LIMIT_TH register (07h); the ALERT pin asserts when the measured value crosses this threshold. The five selectable functions are: Sense Overvoltage Limit (SOVL), Sense Undervoltage Limit (SUVL), Bus Overvoltage Limit (BOVL), Bus Undervoltage Limit (BUVL), and Overpower Limit (OPL).

The ALERT pin is an open-drain output. It asserts when the function chosen in the MASK_ENABLE register exceeds the value programmed in the ALERT_LIMIT_TH register. Although multiple functions can be enabled, only one is actively monitored at a time; priority is determined by the highest-significant bit. For example, if both SOVL and SUVL are selected, the ALERT pin responds to the SOVL comparison against the ALERT_LIMIT_TH register setting.

The conversion-ready state may also be reported at the ALERT pin to indicate that the previous conversion is finished, and a new one can begin. When both the CNVR_MASK bit and a selected alert function are enabled, the Conversion Ready Flag (CNRF bit, MASK_ENABLE register) and the Alert Function Flag (AFF bit, MASK_ENABLE register) must be read after the ALERT pin asserts to identify the alert cause. If the Conversion Ready function is not enabled, the ALERT pin responds only to the selected alert function crossing its limit.

If the alert feature is not used, the ALERT pin can be left floating without affecting operation.

Refer to the timing diagram: after each corresponding conversion, the device compares the converted result to the ALERT_LIMIT_TH register. For example, with SOVL enabled, the measured sense voltage is checked against the

programmed limit after every sense voltage conversion. When the limit is exceeded, the Alert Function Flag (AFF bit, MASK_ENABLE register) sets, and the ALERT pin asserts according to the Alert Polarity bit (APO bit, MASK_ENABLE register). If the Alert Latch function is enabled, the AFF bit and the ALERT pin remain asserted until either the CONFIG register is written or the MASK_ENABLE register is read.

For the Bus Overvoltage Limit (BOVL bit, MASK_ENABLE register) and Bus Undervoltage Limit (BUVL bit, MASK_ENABLE register), the comparison to the ALERT_LIMIT_TH register after every bus voltage conversion; exceeding the limit asserts the AFF bit and the ALERT pin.

For the Overpower Limit (OPL bit, MASK_ENABLE register), the device compares the calculated power (updated after the bus-voltage measurement cycle) to the value in the ALERT_LIMIT_TH register; if the limit is exceeded, the AFF bit and the ALERT pin assert.

Because comparisons are performed on each conversion result, an alert may trigger even if the averaged output has not yet crossed the limit yet. This behavior enables faster detection of short-duration out-of-range events via the alert mechanism, while software can still supervise longer-duration conditions by reading the averaged registers.

17.2 Device Functional Modes

17.2.1 Basic ADC Functions

The device supports two operating modes: continuous and single-shot, and the selected mode determines the ADC's behavior following each conversion. When the MODE bits are set for continuous operation, the monitor continues scanning the enabled channels in sequence until the configuration is reprogrammed. The MODE bits in the CONFIG register also provide sense-only and bus-only conversion options. This flexibility allows the device to be tailored to specific application needs.

In single-shot (triggered) mode, writing any single-shot mode setting to the CONFIG register (CONFIG.MODE = 001b, 010b, or 011b) initiates a single conversion cycle. This cycle converts the enabled measurement(s) — sense and/or bus voltage — once, and then the device automatically enters power-down mode. To execute another single-shot conversion, write to the CONFIG register again, even if the MODE value doesn't change, the write acts as the trigger. Registers can be read at any time, including during power-down; they hold the results of the last completed conversion results. The Conversion Ready Flag (CNRF bit, MASK_ENABLE register) is set when all conversions are complete; this is especially useful when longer conversion times are configured.

The CNRF bit is cleared by:

1. Writing to the CONFIG register (unless setting the MODE bits to power-down), or
2. Reading the MASK_ENABLE register.

17.2.2 Device Shutdown

In addition to the two measurement modes (continuous and single-shot), the device provides an independent power-down mode that lowers the quiescent current. This mode minimizes the supply drain when the device is idle. Exiting the power-down mode to a fully operational state requires a recovery time of 100μs before valid measurements are available. While in the power-down mode, all registers remain readable and writable. The device stays in power-down mode until a valid active operating mode is programmed into the CONFIG register.

17.2.3 Power-On Reset

The POR asserts when the supply voltage falls below the defined threshold (V_{POR}), resetting all registers to their default values. The default power-up settings are provided in the register list table.

17.2.4 Averaging and Conversion Time Considerations

The device supports programmable conversion times for sense and bus voltage measurements, selectable from 136μs to 8.204ms. Combined with programmable averaging, these settings enable optimization of the system timing. Different conversion times may be used for sense and bus voltage measurements; in applications with a stable bus, the bus voltage conversion time can be shortened relative to the sense voltage conversion time. Conversion time and averaging present trade-offs: averaging improves accuracy by reducing coupled noise, and higher averaging counts yield greater noise reduction, while longer conversion times improve noise performance. Figure 2 illustrates the relationship between the conversion time and noise. For maximum accuracy, choose the longest practical conversion times and the highest averaging count allowed by the system timing constraints.

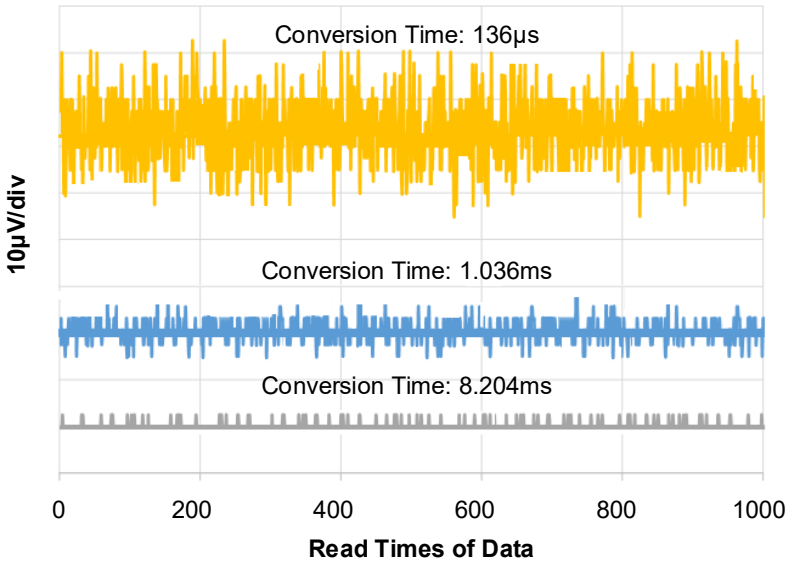


Figure 2. Noise vs. Conversion Time

17.3 Programming

17.3.1 I^2C Serial Interface

The device is an SMBus/I^2C target. The SDA and SCL pins are open-drain with integrated glitch filters and Schmitt-trigger inputs to reduce spikes and bus noise. Good PCB layout further limits coupling: avoid capacitive edge coupling between the SDA and SCL pins, reference routing to a solid ground plane or guard trace and consider shielding to prevent spurious START/STOP detection.

The device supports Fast-mode (1kHz to 400kHz) and High-speed mode (1kHz to 2.94MHz) transfer rates and is compliant with the SMBus 3.0 transfer protocol. Bits are sent MSB-first; multi-byte data are transferred most-significant byte first. The controller addresses the device using a 7-bit slave address plus an R/$\overline{W}$ bit.

One address pin (A0) provides 4 selectable addresses (see Table 1) for both the A and B versions of the device. The A0 pin is sampled on each bus transaction; establish its state before bus activity.

Table 1. Address Pins and Slave Address

A0	RTQ6136D-TAA	RTQ6136D-TBA
GND	1000000	1001000
VS	1000001	1001001
SDA	1000010	1001010
SCL	1000011	1001011

17.3.2 Writing to and Reading Through the I²C Serial Interface

For a write operation (see Figure 3), the master sends the slave (device) address byte with the R/$\overline{W}$ bit set to 0, a register-pointer byte, and then two data bytes (MSB first); each is acknowledged by the slave. The sequence ends with a STOP or a repeated START condition.

During a read operation (see Figure 4), the device returns data from the register whose address was last written to the register pointer. To change this register pointer (see Figure 5), the master writes the slave address with the R/$\overline{W}$ bit set to 0, followed by the register pointer byte. Once set, the master issues a repeated START and sends the slave address with the R/$\overline{W}$ bit set to 1 to begin the read operation. The device returns the MSB first; the master ACKs that byte, and the LSB follows. The master may ACK or NACK the second data byte; the master can terminate the transfer by issuing a NACK after receiving any data byte, or by generating a START or STOP condition. For repeated reads from the same register, resending the pointer is not required; the device retains the pointer value until a subsequent write operation changes it.

The 7-bit I²C slave address (SA6-SA0) is set by the hardware configuration of the address pin(s); see Table Table 1. The device does not provide packet error checking (PEC) or clock-stretching capability.

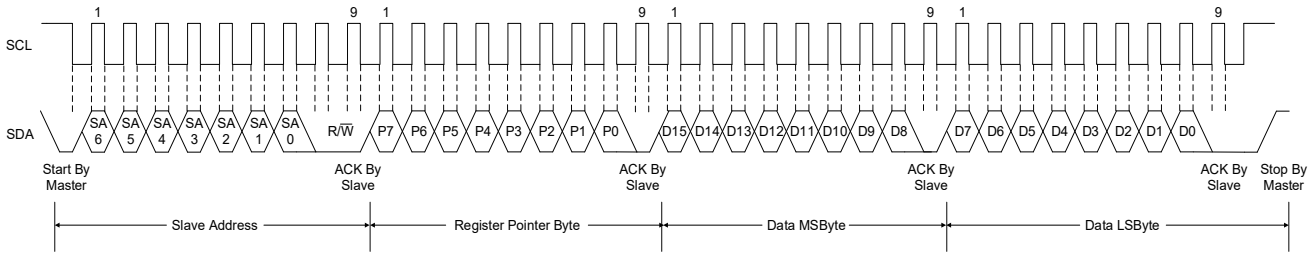


Figure 3. Timing Diagram for Write Word Format

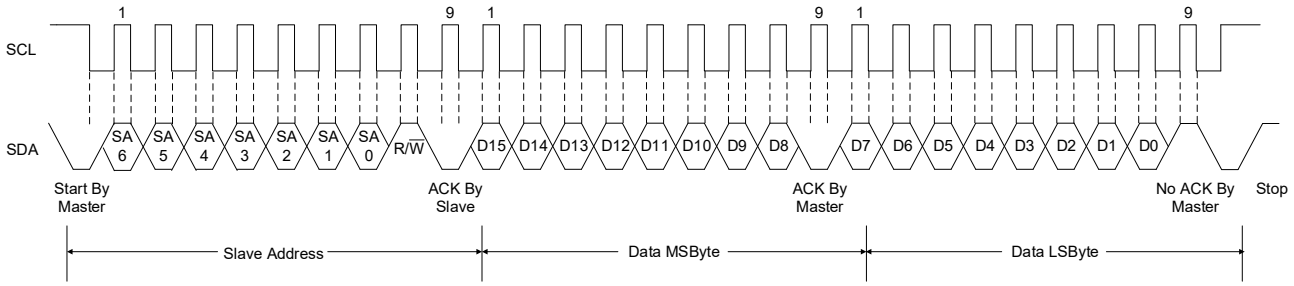


Figure 4. Timing Diagram for Read Word Format

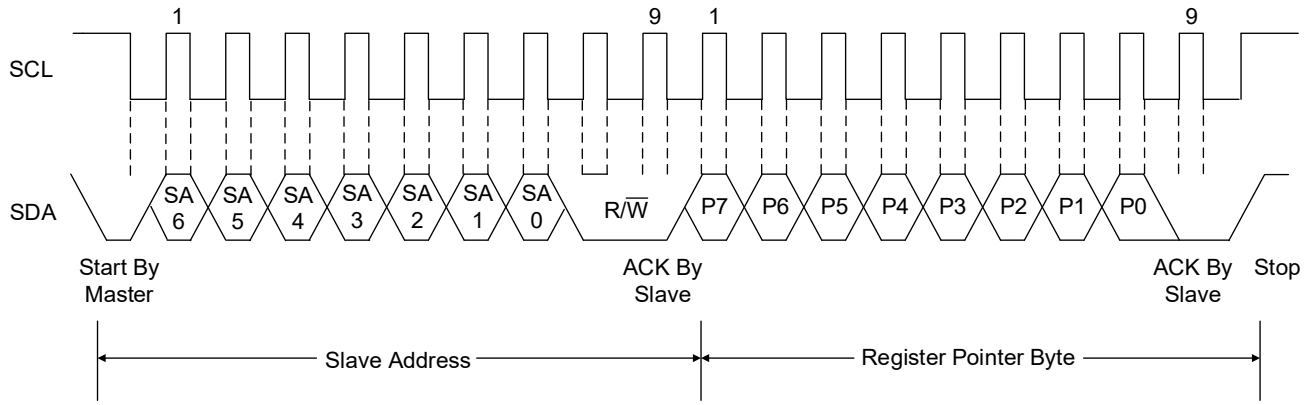


Figure 5. Typical Register Pointer Set

17.3.3 High-Speed I²C Mode

When the bus is idle, the SDA and SCL lines are pulled high by pull-ups. Hs-mode is entered by a START condition followed by the Hs-mode controller code 00001xxx, transmitted at ≤400kHz in F/S mode. The device does not ACK this code; instead, it recognizes the code and reconfigures input filtering for operation up to 2.94MHz. The controller then issues a repeated START; subsequent transfers follow the F/S protocol but may run at up to 2.94MHz. Maintain Hs-mode by issuing repeated STARTs; issuing a STOP condition exits Hs-mode and restores the F/S filtering.

17.3.4 General Call Reset

To issue a General Call reset, send the General Call address 0000_000b (0x00) with R/$\overline{W}$ = 0, and then transmit the data byte 0000_0110b (0x06). Upon receiving the 2-byte sequence, the device is designed to respond to the general call reset; The device performs a soft reset and reverts to the default power-up settings.

17.3.5 SMBus Alert Response

The device supports the SMBus Alert Response Address (ARA). When an alert occurs, the controller issues the ARA (0001_100b; R/$\overline{W}$ = 1). The alerted device that wins the arbitration ACKs and returns its own address, identifying itself to the controller. If multiple targets respond, standard arbitration selects one; non-winning devices do not complete the response and continue to assert the ALERT pin low until serviced.

18 Application Information

(Note 8)

18.1 Feature Description

The device is a current-sense and bus-voltage monitor with an I²C/SMBus-compatible digital interface. It measures sense-voltage drop and bus voltage at the IN- pin to derive the current and power. Programmable calibration, conversion-time, and averaging settings, combined with an internal multiplier, provide direct readings of the current (A) and power (W).

18.1.1 Device Measurement Range and Resolution

The device provides two sense-measurement ranges: ±81.92mV or ±20.48mV across the IN+ and IN− pins, which are selected by the CONFIG.ADCRANGE (00h). The BUS_VOLTAGE register can represent voltage from 0V to 104.856V (65535 × 1.6mV/LSB). However, the measurable bus voltage is limited to the common-mode input range specified under the recommended operating voltage.

Table 2. ADC Full Scale Values

Parameter	Full Scale Value	Resolution
Sense Voltage	±81.92mV (ADCRANGE = 0)	2.5μV/LSB
	±20.48mV (ADCRANGE = 1)	625nV/LSB
Bus Voltage	0V to 104.856V (Limit usable range to recommended operating voltage)	1.6mV/LSB

Sense and bus voltage results are available in the SENSE_VOLTAGE and BUS_VOLTAGE registers, respectively. Sense voltage is signed to accommodate bi-directional current; the bus voltage is always positive (unsigned). Convert codes to volts by multiplying by the corresponding LSB (resolution).

18.1.2 Current and Power Calculations

The CALIBRATION register must be programmed with a constant conversion value (SENSE_CAL) to enable reporting the current in amperes. The constant is computed from CURRENT_LSB and R_{SENSE} (see Equation (1)). CURRENT_LSB is the chosen code step size for the CURRENT register (04h); Equation (2) specifies the minimum CURRENT_LSB for the expected IMAX, and thus the maximum resolution. For convenience, a rounded CURRENT_LSB of up to 8× the minimum may be used to simplify the arithmetic. R_{SENSE} is the external sense resistor across the IN+ and IN− pins. Use Equation (1) for ADCRANGE = 0; for ADCRANGE = 1, divide SENSE_CAL by 4.

$$SENSE\_CAL = \frac{0.00512}{CURRENT\_LSB \times R_{SENSE}} \quad (1)$$

where:

- 0.00512 is an internal scaling constant used in the calibration equation.
- CURRENT_LSB is the chosen code step size for the CURRENT register. Choose a CURRENT_LSB that is ≥ CURRENT_LSB(min) and < 8× CURRENT_LSB(min); smaller values provide higher resolution, while larger rounded values simplify the conversion at the expense of resolution.
- For ADCRANGE = 1, set SENSE_CAL = SENSE_CAL(ADCRANGE = 0) / 4.

$$CURRENT\_LSB(min) = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

The current is derived from the sense voltage measurement and the programmed SENSE_CAL value. If SENSE_CAL = 0, the CURRENT register reads 0A. After SENSE_CAL is programmed, read CURRENT[15:0] from the CURRENT register. Use Equation (3) to obtain the current by applying the CURRENT_LSB scaling:

Current [A] = CURRENT_LSB x CURRENT[15:0] (3)

The power value, POWER[15:0], is available in the POWER register; use Equation (4) to obtain the power in watts from the register code:

Power [W] = 32 x CURRENT_LSB x POWER[15:0] (4)

18.1.3 Filtering and Input Considerations

Current measurement is often noise-sensitive. The device supports independent selection of the conversion time and averaging depth in the CONFIG register (00h), with separate conversion-time settings for the sense and bus voltage measurements.

The ADC employs a ΔΣ front end with a 1MHz (±5% maximum) sampling rate, providing strong noise rejection. Transients at harmonics of the sampling rate (≥2MHz) may cause aliasing and should be mitigated by applying input filtering. The high sampling frequency permits the use of low-value series resistors in the input filter with negligible accuracy impact. Applying filtering only if transients occur at exact harmonics of 1MHz; use the lowest practical series resistance (typically ≤27Ω) and a ceramic capacitor (0.1μF to 1μF). See Figure 6 for an example input filter.

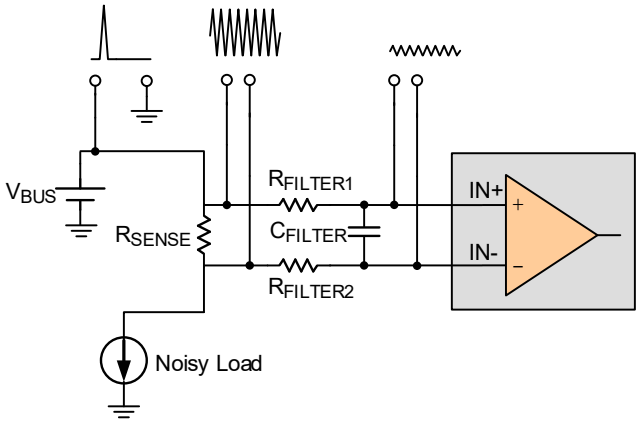


Figure 6. Input Filtering

Input overloads must be considered. The inputs tolerate up to 26V differential across the IN+ and IN− pins. A load-side short to ground can apply the full supply across the R_{SENSE}; clearing the short may produce inductive kickback that can exceed the 26V differential and 60V common-mode ratings. Limit these transients with Zener-type TVS clamps and adequate energy-storage capacitance. A hard short can produce an excessive input dV/dt that may overstress the input pins. Adding a 10Ω resistors in series with each input helps limit fault-induced transients with minimal impact on measurement accuracy.

18.2 Typical Application

The device senses the voltage drop across an external current-sense resistor (R_{SENSE}) as the load current flows through the resistor. It also measures the bus voltage and, once the calibration is configured, can compute the corresponding power. In addition, the device provides an alert function: the ALERT pin can be set to assert on a user-defined condition or to indicate that a conversion has completed (conversion-ready)

Table 3. Example Design Requirements

Design Item	Example Value
Device Supply (V_S)	3.3V
Bus Power (V_{CM})	12V
Average Current	3A
Overcurrent Alert Threshold	4A
Maximum current monitored (I_{MAX})	5A
ADC Range Selection (V_{SENSE_MAX})	±81.92mV (ADCRANGE = 0)

This design example walks through the process of selecting the sense resistor, programming the CALIBRATION register, setting the correct fault thresholds, and demonstrates how to properly scale the returned values from the device.

18.2.1 Select the Sense Resistor

Using the design inputs listed in Table 3, the maximum allowable sense resistance is determined from the maximum measured current (I_{MAX}) and the full-scale sense limit (V_{SENSE_MAX}) of the selected ADC range. At I_{MAX}, the differential voltage across the sense inputs must remain within the device full-scale range (V_{SENSE_MAX}). Applying Equation 5 to the stated parameters yields a maximum R_{SENSE} of 16.384mΩ, so the nearest standard value below this limit is chosen as 16mΩ. A lower sense of resistance can further reduce power dissipation, but this typically trades off measurement resolution/accuracy. Finally, the selected sense resistor must be rated to safely dissipate the expected power at the maximum load over the intended operating temperature.

$$R_{SENSE} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \quad (5)$$

18.2.2 Configure the Device

To begin configuring the device, the CONFIG register (00h) must be set correctly. When the device is powered up, this register loads its default reset values. In the default power-on state, the device selects the ±81.92mV sense range and the ADC continuously converts both the sense voltage and the bus voltage. If the default power-up settings do not match the design requirements, the required register settings must be reconfigured after every VS power cycle.

18.2.3 Program the Sense Calibration Register

To ensure the device can correctly output any current-derived results, the sense CALIBRATION register must be programmed properly each time the supply (V_S) powers up. First, determine the minimum current LSB using Equation 2. With a maximum expected current of 5A, this yields a minimum LSB of 152.588μA. The device permits selecting a CURRENT_LSB up to eight times larger than this minimum; in this example, 200μA is chosen. Next, applying Equation 1 with the selected CURRENT_LSB and the chosen sense resistor value gives a sense CALIBRATION register value of 1600 (decimal), which is 0x640. If the sense CALIBRATION register is not programmed, any results that depend on current will read as zero. However, programming this register is not necessary for reading the sense voltage, reading the bus voltage, or configuring the alert limits.

18.2.4 Set Desired Alert Thresholds

The device can drive the ALERT pin for multiple fault conditions, as described in the ALERT pin section. To choose which fault condition will assert the ALERT pin, program the MASK_ENABLE register (06h) accordingly. The trip

threshold for the selected fault is then set by writing the desired limit into the ALERT_LIMIT_TH register (07h).

For instance, to detect an overcurrent event, set the SOVL bit in the MASK_ENABLE register to 1. Next, write the intended overcurrent threshold into the ALERT_LIMIT_TH register. In this example, the overcurrent threshold is 4A and the sense resistor is 16mΩ, which corresponds to a sense voltage limit of 64mV. After determining the sense voltage limit, compute the sense overvoltage limit code by dividing that limit by the sense voltage LSB size. With these values, the ALERT_LIMIT_TH register code is 64mV ÷ 625nV = 25600 (decimal), or 0x6400.

18.2.5 Calculate Returned Values

Table 4 lists the register contents based on the design assumptions in Table 3. It includes the user-configured settings written to the CONFIG, CALIBRATION, MASK_ENABLE, and ALERT_LIMIT_TH registers, along with the device readback results for sense voltage, current, bus voltage, and power. The parametric values are calculated by multiplying the returned value by the corresponding LSB.

Table 4. Example Design Requirements

Register	Contents	LSB	Calculated
CONFIG (00h)	16679d (4127h)	-	-
CALIBRATION (05h)	1600d (640h)	-	-
MASK_ENABLE (06h)	32768 (8000h)	-	-
ALERT_LIMIT (07h)	25600d (6400h)	2.5μV	25600 × 2.5μV = 0.064V
SENSE_VOLTAGE (01h)	19200 (4B00h)	2.5μV	19200 × 2.5μV = 0.048V
BUS_VOLTAGE (02h)	7500d (1D4Ch)	1.6mV	7500 × 1.6mV = 12V
CURRENT (04h)	15000d (3A98h)	200μA	15000 × 200μA = 3A
POWER (03h)	5625d (15F9h)	Current LSB x 32 = 6.4mW	5625 × 6.4mW = 36W

The sense voltage and current readings are reported in two's-complement format. In this representation, a negative number is indicated by the most-significant bit being set to 1. To convert a negative two's-complement value to a decimal number, first invert all bits and add 1 to get the magnitude as an unsigned value; then convert that magnitude to decimal and apply a negative sign.

18.2.6 Application Curves

Figures 18-2 and 18-3 illustrate how the ALERT pin behaves during a bus overvoltage event when the bus-voltage conversion time is set to 136μs and averaging is set to 1. To capture the spread in response across repeated fault occurrences, oscilloscope persistence is enabled on the ALERT pin waveform. The alert response delay is not constant; it can vary depending on the operating point prior to the fault (for example, the pre-fault current level) and on how far the fault condition exceeds the programmed threshold. Figure 7 shows a faster response when the fault overshoots the threshold by a large margin, whereas Figure 8 shows the response when the bus overvoltage only slightly exceeds the limit. The response time varies mainly because the externally applied fault is not aligned to the internal ADC conversion start time. With continuous ADC sampling, an alert is usually raised faster when the signal is already near the threshold, and slower when it starts far below it. For systems that require deterministic timing, the worst-case alert response can be estimated as 2 × (tconv_sense + tconv_voltage). If the alert is configured for an overpower condition, allow an additional 60μs for internal background computations.

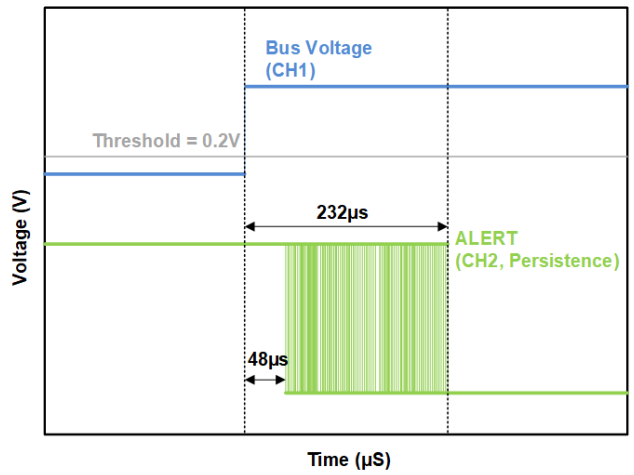


Figure 7. ALERT Response Time (Samples Well Above the Threshold)

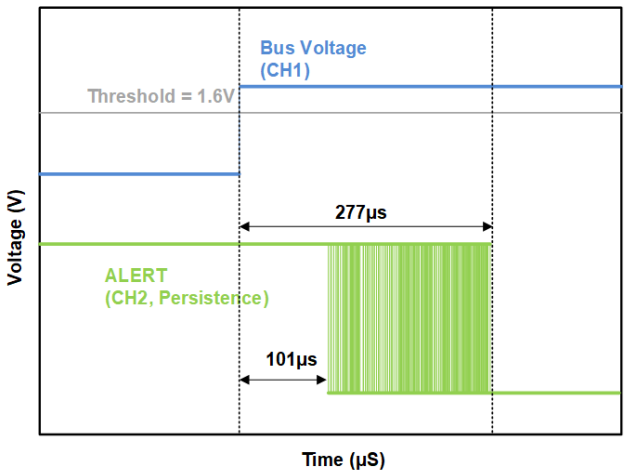


Figure 8. ALERT Response Time (Samples Just Above the Threshold)

18.3 Power Supply Recommendations

The Typical Application Circuit in Section 15 shows that the device input circuitry can accurately measure signals even when the common-mode voltage exceeds the supply voltage (V_S). For instance, V_S may be 5V while the monitored bus (common-mode) can be as high as 60V. In addition, the input pins can tolerate the full –0.3V to 60V range regardless of whether the device itself is powered.

Place the supply bypass capacitor(s) as close as possible to the device's supply and ground pins to maintain stable operation. A typical bypass capacitor value is 0.1µF. In applications with noisy or high-impedance supplies, additional decoupling capacitance may be required to reduce supply noise.

Note that the ALERT_LIMIT_TH register resets back to its default contents after any V_S power-cycle, so the threshold must be written again each time power is applied.

18.4 Thermal Consideration

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TSOT-28(COL) package, the thermal resistance, θ_{JA}, is 130.27°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (130.27°C/W) = 0.77W for a TSOT-28(COL) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 9 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

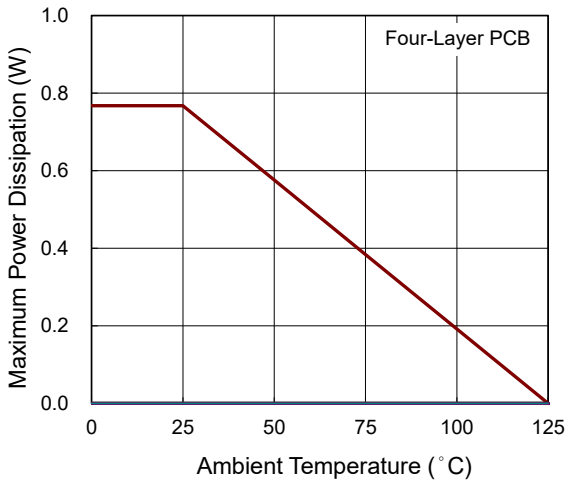
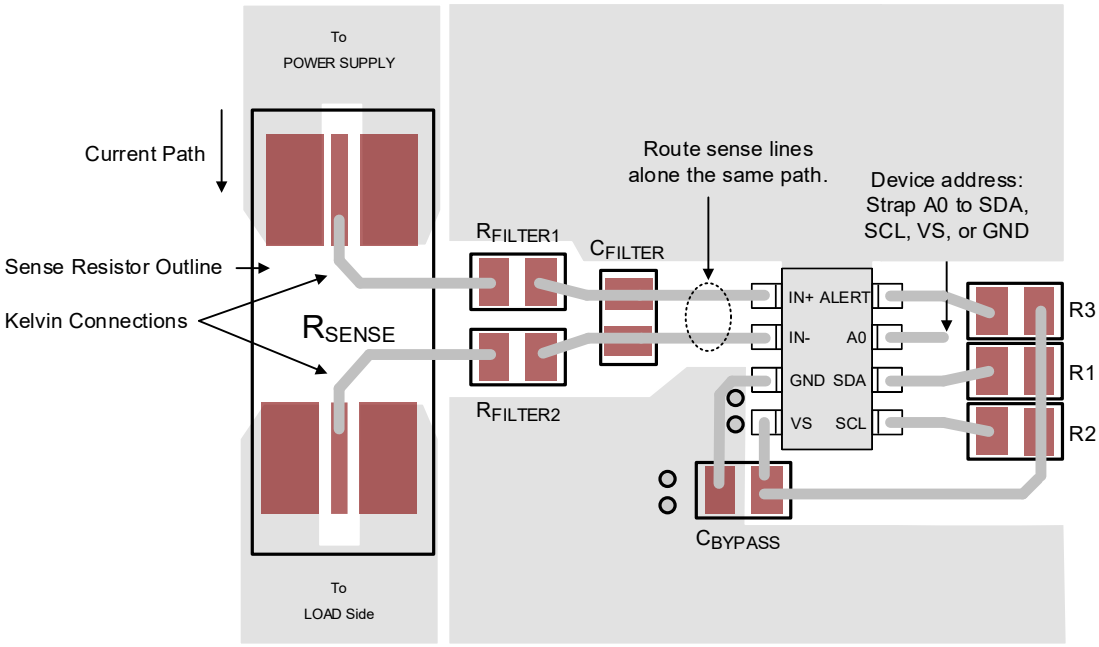


Figure 9. Derating Curve of Maximum Power Dissipation

18.5 Layout Guidelines

- A Kelvin-sense arrangement is required for optimal performance. Connect the input pins (IN+ and IN-) to the sense resistor using a 4-wire connection.
- The PCB trace resistance from the sense resistor to the IN+ and IN- pins can affect the power measurement accuracy. Place the sense resistor as close to the device as possible and avoid using minimum-width PCB traces.
- Place the power-supply bypass capacitor as close to the supply and ground pins as possible.



Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Functional Register Description

The table shows a summary of the device registers. These registers are two bytes with an I^2C interface.

Table 5. Register List

Register Name	Address	Type	Default	Description
CONFIG	00h	R/W	4127h	Operating mode configuration, conversion times and averaging setting
SENSE_VOLTAGE	01h	R	0000h	Sense voltage measurement data
BUS_VOLTAGE	02h	R	0000h	Bus voltage measurement data
POWER	03h	R	0000h	Calculated power data
CURRENT	04h	R	0000h	Calculated current data
CALIBRATION	05h	R/W	0000h	Current calibration
MASK_ENABLE	06h	R/W	0000h	Alert configuration
ALERT_LIMIT_TH	07h	R/W	0000h	Limit threshold setting
AUX_FUNCTION	08h	R/W	0000h	Auxiliary function setting
MANUFACTURER_ID	3Eh	R	1214h	Manufacturer identification number.
DEVICE_ID	3Fh	R	6000h	Die identification number.

Table 6. CONFIG Register

Address (00h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RST	RSVD		ADCRANGE	AVG			VBUSCT			VSENCT			MODE		
Default	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1
Type	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
15	RST (Reset Bit)	Set this bit to '1' to reset all registers to their default values. This bit self-clears.
14:13	RSVD	Reserved value always returns 10b
12	ADCRANGE	Select sense voltage full scale input range across IN+ and IN–. 0: ±81.92mV (default) 1: ±20.48mV
11:9	AVG (Averaging Mode)	Set the number of samples that are collected and averaged 000: 1 (default) 001: 4 010: 16 011: 64 100: 128 101: 256 110: 512 111: 1024
8:6	VBUSCT (Bus Voltage Conversion Time)	Set the conversion time for the bus voltage measurement. 000: 136μs 001: 200μs 010: 264μs 011: 520μs 100: 1036μs (default) 101: 2060μs 110: 4108μs 111: 8204μs
5:3	VSENCT (Sense Voltage Conversion Time)	Set the conversion time for the sense voltage measurement 000: 136μs 001: 200μs 010: 264μs 011: 520μs 100: 1036μs (default) 101: 2060μs 110: 4108μs 111: 8204μs
2:0	MODE (Operating Mode)	Select continuous, triggered, or power-down mode of operation 000: Shutdown 001: Sense voltage triggered, single shot 010: Bus voltage triggered, single shot 011: Sense voltage and bus voltage triggered, single shot 100: Shutdown 101: Sense voltage continuous 110: Bus voltage continuous 111: Sense and bus voltage continuous (default)

Table 7. SENSE_VOLTAGE Register

Address (01h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	SIGN	VSENSE														
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Description
15	SIGN (Sign Bit)	SIGN Bit 0: Positive value (default) 1: Negative value, encoded in 2's complement format
14:0	VSENSE (Sense Voltage)	The SENSE_VOLTAGE register stores the current sense voltage reading **Example**: For a value of V_{SENSE} = –80mV: 1. Take the absolute value: 80mV 2. Translate this number to a whole decimal number (80mV ÷ 2.5μV) = 32000 3. Convert this number to binary = 0111 1101 0000 0000 4. Complement the binary result = 1000 0010 1111 1111 5. Add '1' to the complement to create the two's complement result =1000 0011 0000 0000 = 8300h If averaging is enabled, this register displays the averaged value. ADCRANGE= 0, Full-scale range = 81.92mV (decimal = 32767); LSB: 2.5μV. ADCRANGE= 1, Full-scale range = 20.48mV (decimal = 32767); LSB: 625nV. Default: 0h

Table 8. BUS_VOLTAGE Register

Address (02h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	VBUS															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Description
15:0	VBUS (Bus Voltage)	The BUS_VOLTAGE register stores the most recent bus voltage reading LSB: 1.6mV. Default: 0h

Table 9. POWER Register

Address (03h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	POWER															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Description
15:0	POWER	The POWER register records power in watts by multiplying the decimal values of the CURRENT register with the decimal value of the BUS_VOLTAGE register. The power is always a positive value. Default: 0h

Table 10. CURRENT Register

Address (04h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	SIGN	CURRENT														
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
15	SIGN (Sign Bit)	SIGN Bit 0: Positive value (default) 1: Negative value, encoded in 2's complement format
14:0	CURRENT	The value of the CURRENT register is calculated by multiplying the decimal value in the SENSE_VOLTAGE register with the decimal value of the CALIBRATION register. Default: 0h

Table 11. CALIBRATION Register

Address (05h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RSVD	SENSE_CAL														
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ype	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
15	RSVD	Reserved value always returns 0.
14:0	SENSE_CAL	Programming this register sets the Current_LSB and the Power_LSB. Default: 0h

Table 12. MASK_ENABLE Register

Address (06h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	SOVL	SUVL	BOVL	BUVL	OPL	CNVR_ MASK	RSVD				MEM _ST	AFF	CNRF	OVF	APO	ALE
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R	RW	RW

Bits	Name	Description
15	SOVL (Sense Overvoltage Limit)	Setting this bit high configures the ALERT pin to be asserted if the sense voltage measurement following a conversion exceeds the value programmed in the ALERT_LIMIT_TH register.
14	SUVL (Sense Undervoltage Limit)	Setting this bit high configures the ALERT pin to be asserted if the sense voltage measurement following a conversion drops below the value programmed in the ALERT_LIMIT_TH register.
13	BOVL (Bus Overvoltage Limit)	Setting this bit high configures the ALERT pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the ALERT_LIMIT_TH register.
12	BUVL (Bus Undervoltage Limit)	Setting this bit high configures the ALERT pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the ALERT_LIMIT_TH register.
11	OPL (Overpower Limit)	Setting this bit high configures the ALERT pin to be asserted if the Power calculation exceeds the value programmed in the ALERT_LIMIT_TH register.
10	CNVR_MASK (Conversion Ready Mask)	Setting this bit high configures the ALERT pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion. 0: Disable conversion ready flag on ALERT pin (default) 1: Enables conversion ready flag on ALERT pin
9:6	RSVD	Reserved value always returns 0.
5	MEM_STAT (Memory Status Flag)	Indicates the integrity status of the internal trim memory. 0: Integrity OK (default) 1: Integrity error detected

Bits	Name	Description
4	AFF (Alert Function Flag)	Although only one alert function can be monitored on the ALERT pin at a time, the conversion ready function can also be enabled to assert the ALERT pin. After an alert occurs, reading the AFF bit allows the user to determine whether the alert function caused the alert. When the ALE bit is configured for Latch mode, the AFF bit is cleared only by reading the MASK_ENABLE register. When the ALE bit is configured for Transparent mode, the AFF bit is cleared after the next conversion that does not generate an alert condition.
3	CNRF (Conversion Ready Flag)	While the last conversion result can be read at any time, the CNRF bit is used to indicate completion of one-shot or triggered conversions. This bit is set only after all conversions, averaging, and multiplication operations are finished. The CNRF bit clears under the following conditions: 1.) Writing to the CONFIG Register (except for Power-Down selection) 2.) Reading the MASK_ENABLE register
2	OVF (Math Overflow Flag)	This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that the current and power data may be invalid.
1	APO (Alert Polarity bit)	The Alert Polarity bit controls the polarity of the ALERT pin. 0: Active low (default) 1: Active high
0	ALE (Alert Latch Enable)	When the ALE bit is set to Transparent mode, the ALERT pin and the AFF bit are reset when the fault is cleared. When the ALE bit is set to Latch mode, the ALERT pin and the AFF bit remains active following a fault until the MASK_ENABLE register has been read. 0: Transparent Mode (default) 1: Latch Mode

Table 13. ALERT_LIMIT_TH Register

Address (07h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	ALERT_LIMIT_TH															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
15:0	ALERT_LIMIT_TH	The ALERT_LIMIT_TH register stores the threshold value that is compared with the register specified by the MASK_ENABLE register to determine whether the limit has been exceeded. Default: 0h

Table 14. AUX_FUNCTION Register

Address (08h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RSVD														AVG_AUX	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bits	Name	Description
15:2	RSVD	Reserved value always returns 0.
1:0	AVG_AUX	00: AVG sample refer to CONFIG.AVG[11:9] (default) 01: AVG sample refer to CONFIG.AVG[11:9] 10: AVG sample 2048 11: AVG sample 4096

Table 15. MANUFACTURER_ID Register

Address (3Eh)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	MANUFACTURER_ID															
Default	0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

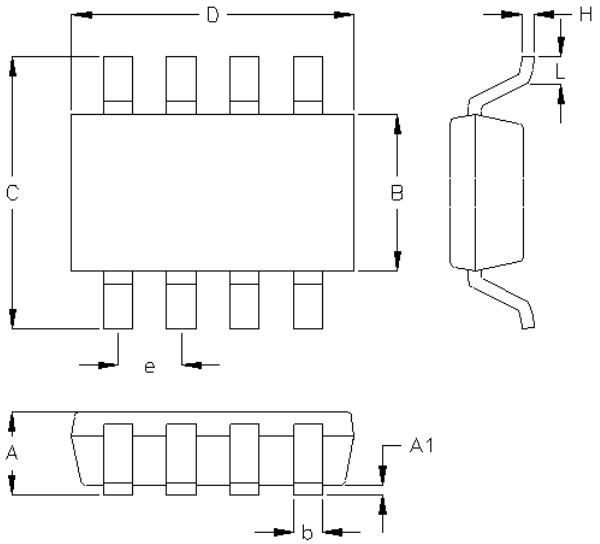
Bits	Name	Description
15:0	MANUFACTURER_ID	Stores the manufacturer identification bits

Table 16. DEVICE_ID Register

Address (3Fh)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	DEVICE_ID												RSVD			
Default	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
15:4	DEVICE_ID	Stores the device revision identification bits
3:0	RSVD	Reserved value always returns 0.

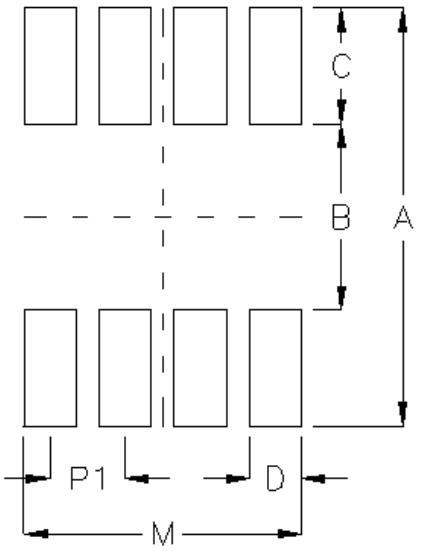
20 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-28(COL) Package

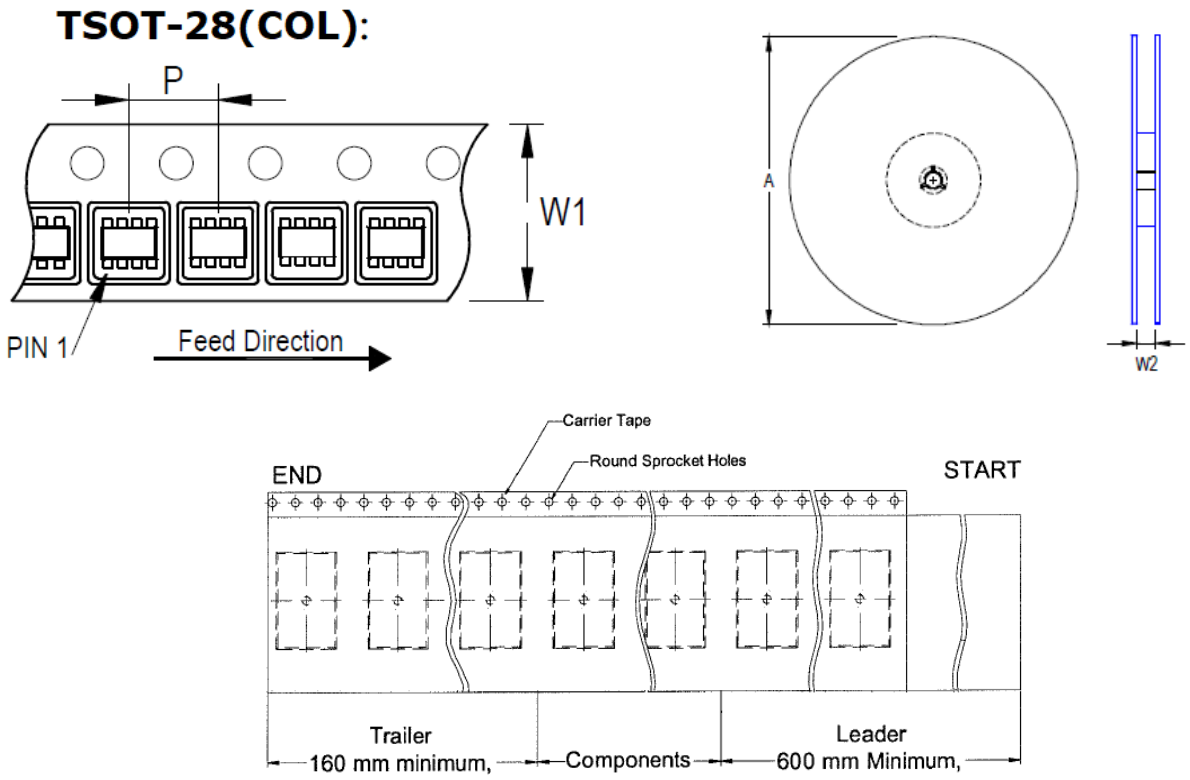
21 Footprint Information



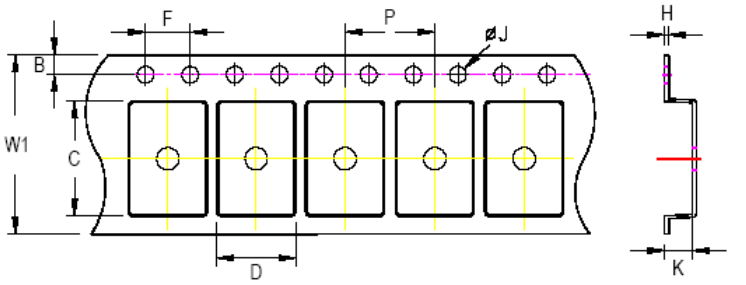
Package	Number of Pins	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-28(COL)	8	0.65	3.60	1.60	1.00	0.45	2.40	±0.10

22 Packing Information

22.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
TSOT-28(COL)	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.37mm	0.43mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
TSOT-28(COL)	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation

14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

23 Datasheet Revision History

Version	Date	Description
00	2026/08/06	First Edition