RICHTEK®

RTQ6749-QT-A2

TFT-LCD Integrated Power Module for Automotive Applications

1 General Description

The RTQ6749 is a programmable power management IC with an I^2C interface, designed for automotive TFT-LCD panel applications. It integrates two synchronous boost converters for PAVDD and VGH, a synchronous NAVDD buck-boost converter, a VGL charge pump, a high-performance VCOM with 8-bit calibration, and a RESET voltage detector. The device is available in a compact WQFN-32L 5x5 package.

The RTQ6749 operates from a 2.5V to 5.5V input voltage range. Its high switching frequency minimizes interference with the AM radio band. Comprehensive protection features include overcurrent protection for all internal-switch converters and output-fault shutdown, which protects all converters against output-fault and asserts a FAULT signal for communication with automotive systems. Programmable soft-start functions for all output voltages help limit input inrush current during startup. The recommended junction temperature is –40°C to 150°C, and the recommended ambient temperature is –40°C to 105°C.

2 Ordering Information

RTQ6749□□-QT-A2

- **Package Type**(1)
  QW: WQFN-32L 5x5 (W-Type)
- **Lead Plating System**
  G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates Richtek products are Richtek Green Policy compliant.

3 Features

- **AEC-Q100 Grade 2 Qualified**
- **2.5V to 5.5V Input Supply Voltage**
- **I^2C Interface**
- **Power-On and Power-Off Sequence Free**
- **PAVDD Programmable Output Voltage 5V to 7.3V**
- **PAVDD Output Current Capability up to 200mA**
- **NAVDD Programmable Output Voltage –5V to –7.3V**
- **NAVDD Output Current Capability up to 200mA**
- **VGH Programmable Output Voltage 7V to 30V**
- **VGH Output Current Capability Up to 60mA**
- **VGH Output Voltage Temperature Compensation**
- **VGL Programmable Output Voltage –6V to –18V**
- **VGL Output Current Capability Up to 60mA**
- **VCOM 8-bit Programmable Output Voltage**
- **Outputs Power-Off Discharge Function**
- **Programmable Voltage Detector**
- **Built in UVLO, UVP, OVP, SCP and OTP Protection**
- **Ambient Temperature Range: –40°C to 105°C**
- **Junction Temperature Range: –40°C to 150°C**

4 Applications

- Infotainment LCD Panels

5 Marking Information

RTQ6749
GQW-QT
YMDNN

RTQ6749GQW-QT: Product Code
YMDNN: Date Code

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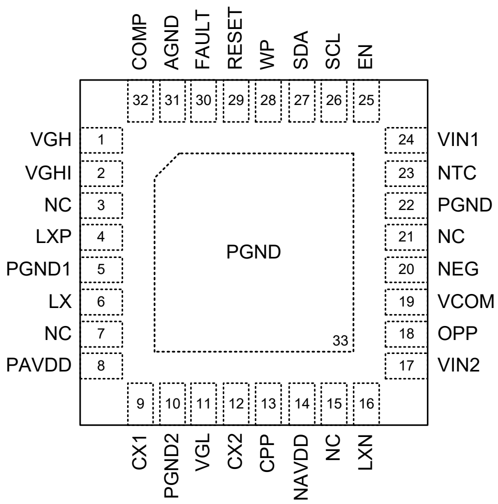
6 Pin Configuration

(TOP VIEW)



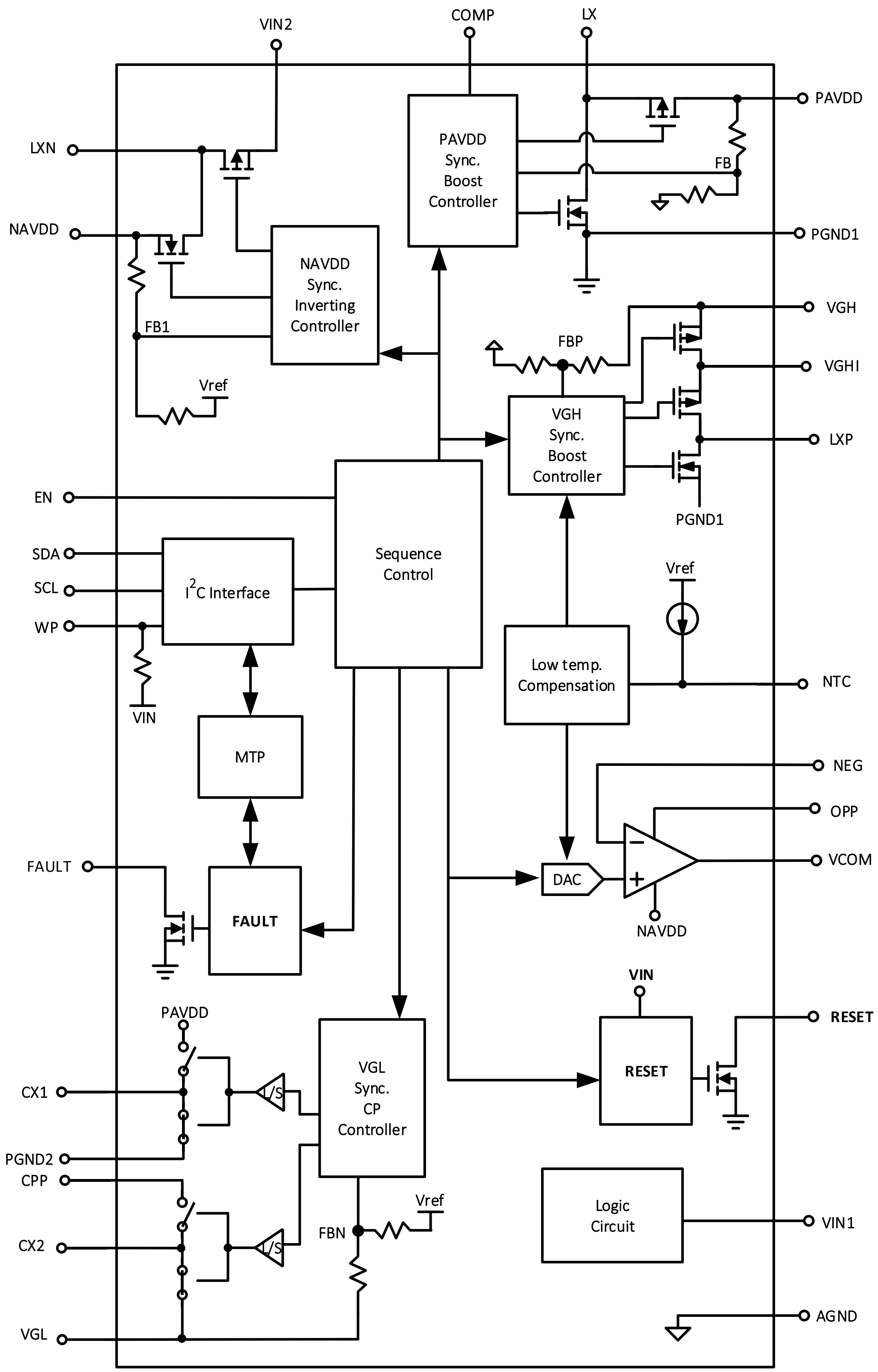
WQFN-32L 5x5

7 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VGH	VGH boost converter output.
2	VGHI	VGH boost converter output without sequence control. The output is not isolated from input.
3	NC	No internal connection.
4	LXP	Switching node of VGH boost converter.
5	PGND1	Power ground of PAVDD and VGH boost converter.
6	LX	Switching node of PAVDD boost converter.
7	NC	No internal connection.
8	PAVDD	PAVDD boost converter output.
9	CX1	VGL charge pump flying cap node1.
10	PGND2	Power ground of VGL charge pump.
11	VGL	VGL charge pump output.
12	CX2	VGL charge pump flying capacitor node2.
13	CPP	VGL charge pump power input.
14	NAVDD	NAVDD inverting converter output.
15	NC	No internal connection.
16	LXN	Switching node of NAVDD inverting converter.
17	VIN2	NAVDD supply voltage input.
18	OPP	VCOM OP-Amp positive power supply. Do not leave floating.
19	VCOM	VCOM Op-Amp output.
20	NEG	Inverting input of VCOM calibrator.
21	NC	No internal connection.

Pin No.	Pin Name	Pin Function
22	PGND	Power ground.
23	NTC	Thermistor network connection for temperature compensation.
24	VIN1	IC supply voltage input.
25	EN	Enable control input.
26	SCL	I^2C clock input.
27	SDA	I^2C data input.
28	WP	MTP write protection. When WP = 1, MTP is protected, but the register still can be written. WP = 0, both register and MTP can be written. Internal 175kΩ pull-up to VIN.
29	RESET	Output of voltage detection function.
30	FAULT	Fault signal output.
31	AGND	Analog ground.
32	COMP	AVDD boost converter compensation input.
33 (Exposed Pad)	PGND	The exposed pad must be soldered to a large PCB and connected to PGND for maximum thermal dissipation.

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 2)

- VIN1, VIN2 to AGND -- –0.3 to 6V
- PGND1, PGND2, AGND to PGND -- –0.3 to 0.3V
- COMP, RESET, FAULT, WP, SDA, SCL, EN, NTC to AGND--- –0.3 to 6V
- LX, PAVDD to PGND -- –0.3 to 10V
- VIN2 to LXN--- –0.3 to 13V
- NAVDD to PGND --- –12 to 0.3V
- PAVDD to CX1 -- –0.3 to 10V
- CX1 to PGND2 -- –0.3 to 10V
- CX2 to CPP -- –0.3 to 10V
- CX2 to VGL -- –0.3 to 20V
- CPP to PGND --- NAVDD to 0.3V
- VGL to PGND-- –20 to 0.3V
- LXP, VGHI, VGH to PGND --- –0.3 to 35V
- OPP to VCOM, NEG -- –0.3 to 16V
- VCOM, NEG to NAVDD --- –0.3 to 16V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN 32L 5x5 --- 4.18W
- Package Thermal Resistance (Note 3)

  WQFN 32L 5x5, θ_{JA} --- 29.85°C/W

  WQFN 32L 5x5, θ_{JC} --- 0.72°C/W
- Lead Temperature (Soldering, 10 sec) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range --- –60°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model)--- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

10 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN1 --2.5V to 5.5V
- Junction Temperature Range -- –40°C to 150°C
- Ambient Temperature Range -- –40°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

11 Electrical Characteristics

(VIN1 = 2.5V to 5.5V, T_A = –40°C to 105°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
VIN1 Range	V_{VIN1}		2.5	--	5.5	V
VIN1 Undervoltage-Lockout Threshold	V_{UVLO_R}	VIN1 rising, turn on IC	2.16	2.33	2.5	V
	V_{UVLO_H}	$V_{UVLO\_H} = V_{UVLO\_R} - V_{UVLO\_F}$	0.01	0.15	0.3	V
EN/WP Input Threshold	V_{IH}		1.5	--	--	V
	V_{IL}		--	--	0.8	V
VIN1 Quiescent Current	I_{Q_VIN1}	SW not switching	0	2	4.5	mA
		SW switching	0	2.35	5	mA
VIN1 Shutdown Current	I_{SHDN_VIN1}	EN = Low, VIN1 = 3.3V	0	200	400	μA
Switch Frequency Range	f_{OSC}		600	--	2200	kHz
Switch Frequency Accuracy	f_{OSC_ACC}		–15	--	15	%
UVP Voltage Percentage	UVP		58	70	78	%
UVP Fault Delay Duration to IC Shutdown	t_{UVP}		30	50	70	ms
SCP Voltage Percentage	SCP		23	30	37	%
SCP Delay	t_{SCP}		85	100	115	μs
Power-Off Delay Time	t_{DLY_OFF}	3ms/step, 16 steps	0	--	45	ms
Over-Temperature Protection	T_{OTP}	Temperature rising	--	150	--	°C
	ΔT_{OTP}	Hysteresis	--	20	--	°C
PAVDD Synchronous Boost Converter						
Output Voltage Range	V_{PAVDD}	0.05V/step, f_{OSC} = 2.2MHz	5.0 or VIN + 2.2	--	7.3	V
		0.05V/step, f_{OSC} ≤ 1MHz	5.0 or VIN + 1.3	--	7.3	V
Output Voltage Tolerance		T_A = 25°C, (V_O – V_S) / V_S x 100%, no load	–1	--	1	%
		T_A = –40°C to 105°C, (V_O – V_S) / V_S x 100%, no load	–2	--	2	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On Delay Time	t_{DLY_PAVDD}	5ms/step, 16 steps	0	--	75	ms
Soft-Start Time	t_{SS_PAVDD}	5ms/step, 8 steps	5	--	40	ms
Delay/Soft-start Time Tolerance			–15	--	15	%
Maximum Duty	D_{MAX_PAVDD}		83	90	97	%
OVP Voltage percentage	V_{OVP_PAVDD}	PAVDD rising	110	120	130	%
Overcurrent Protection	I_{OCP_PAVDD}		1.5	1.8	2.3	A
On-Resistance of Low-Side MOSFET	$R_{DSON\_LS\_PAVDD}$		0.05	0.2	0.4	Ω
On-Resistance of High-Side MOSFET	$R_{DSON\_HS\_PAVDD}$		0.05	0.3	0.4	Ω
Power-On/Off Discharge R_{ON}	R_{DIS_PAVDD}		3	5	7	Ω
Pre-Charge Threshold	V_{PC}	V_{IN} = 3.3V, V_{PC} = V_{IN} – V_{PAVDD}	--	0.2	--	V
PAVDD SCP level	V_{SCP_PAVDD}	Before PAVDD Soft-start finish	1.134	1.26	1.386	V
NAVDD Synchronous Buck-Boost Converter						
Output Voltage Range	V_{NAVDD}	0.05V/step	–5	--	–7.3	V
Output Voltage Tolerance		T_A = 25°C, (V_O – V_S) / V_S x 100%, no load	–1	--	1	%
		T_A = –40°C to 105°C, (V_O – V_S) / V_S x 100%, no load	–2	--	2	%
On Delay Time	t_{DLY_NAVDD}	5ms/step, 16 steps	0	--	75	ms
Soft-Start Time	t_{SS_NAVDD}	5ms/step, 8 steps	5	--	40	ms
Delay/Soft-Start Time Tolerance			–15	--	15	%
Maximum Duty	D_{MAX_NAVDD}		83	90	97	%
OVP Voltage Percentage	V_{OVP_NAVDD}	NAVDD falling	110	120	130	%
On-Resistance of High-Side MOSFET	$R_{DSON\_HS\_NAVDD}$		0.05	0.14	0.4	Ω
On-Resistance of Low-Side MOSFET	$R_{DSON\_LS\_NAVDD}$		0.05	0.23	0.4	Ω
Power-On/-Off Discharge On-Resistance	R_{DIS_NAVDD}		6	10	14	Ω
Overcurrent Protection	I_{OCP_NAVDD}		1.5	1.9	2.5	A
VGL Charge-Pump Regulator						
Output Voltage Range	V_{VGL}	0.25V/step	–6	--	–18	V
Output Voltage Tolerance		T_A = –40°C to 105°C, (V_O – V_S) / V_S x 100%, no load	–3	--	3	%
On Delay Time	t_{DL_VGL}	5ms/step, 16 steps	0	--	75	ms
Soft-Start Time	t_{SS_VGL}	3ms/step, 8 steps	3	--	24	ms
Delay/Soft-Start Time Tolerance			–15	--	15	%
PMOS R_{ON}	$R_{DSON\_PMOS\_VGL}$		0.15	0.5	1.5	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On-Resistance of N-MOSFET1	$R_{DSON\_NMOS1\_VGL}$		0.15	0.32	1.5	Ω
On-Resistance of N-MOSFET2	$R_{DSON\_NMOS2\_VGL}$		0.15	0.9	1.5	Ω
On-Resistance of N-MOSFET3	$R_{DSON\_NMOS3\_VGL}$		0.15	0.4	1.5	Ω
Power-On/-Off Discharge On-Resistance	R_{DIS_VGL}		50	175	300	Ω
VGH Sync. Boost Converter						
Output Voltage Range	V_{VGH}		7 or PAVDD + 2	--	30	V
Output Voltage Tolerance		T_A = 25°C, (V_O – V_S) / V_S x 100%, no load	–3	--	3	%
		T_A = –40°C to 105°C, (V_O – V_S) / V_S x 100%, no load	–4.5	--	4.5	%
VGH Low Temperature Compensation Output Voltage Range	VGH_LT	2V/step, 4 steps. VGH = VGH + VGH_LT @ Low temperature compensation. (VGH + VGH_LT) > 30V, VGH is limited on 30V at low temperature.	2	--	8	V
On Delay Time	t_{DLY_VGH}	5ms/step, 16 steps	0	--	75	ms
Soft-Start Time	t_{SS_VGH}	5ms/step, 4 steps	5	--	20	ms
Delay/Soft-Start Time Tolerance			–15	--	15	%
Maximum Duty	D_{MAX_VGH}		83	90	97	%
OVP Voltage Percentage	V_{OVP_VGH}	(VGH + VGH_LT)*120%	105	120	135	%
Maximum OVP Voltage Threshold	$V_{OVP\_VGH\_Max}$	(VGH + VGH_LT) > 28.5V	32.5	34.5	34.5	V
On-Resistance of Low-Side MOSFET	$R_{DSON\_LS\_VGH}$		0.2	0.36	0.6	Ω
On-Resistance of High-Side MOSFET	$R_{DSON\_HS\_VGH}$		0.3	0.6	1	Ω
On-Resistance of High-Side GD MOSFET	$R_{DSON\_HS\_GD\_VGH}$		0.3	0.65	1	Ω
Power-On/-Off Discharge On-Resistance	R_{DIS_VGH}		150	200	250	Ω
Overcurrent Protection	I_{OCP_VGH}		0.56	0.7	0.88	A
VCOM Operational Amplifier						
VCOM_C Output Voltage Range	V_{COM_C}	20mV/step, 251 steps	-3	--	2	V
VCOM_F Output Voltage Range	V_{COM_F}	10mV/step, 256 steps	V_{COM_C} – 1.27	--	V_{COM_C} + 1.28	V
On Delay Time	t_{DLY_VCOM}	5ms/step, 16 steps	0	--	75	ms
Slew Rate	SR		1	15	40	V/μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Short Circuit Current	I_{VCOM_SC}	Unit Gain,VCOM = –1V,	±100	±350	±600	mA
RESET Function						
On Delay Time	t_{DLY_RESET}	5ms/step, 16 steps	0	--	75	ms
I²C Interface						
High-Level Input Threshold Voltage	V_{IH}	SCL, SDA	1.05	--	--	V
Low-Level Input Threshold Voltage	V_{IL}	SCL, SDA	--	--	0.4	V
SCL Clock Frequency	f_{SCL}		15	400	1000	kHz

Note 6. Limits apply to the recommended operating temperature range of –40°C to 105°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN1 = 2.5V to 5.5V.

Note 7. In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R\theta_{JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX} - (R\theta_{JA} \times P_{D-MAX})$.

12 Typical Application Circuit

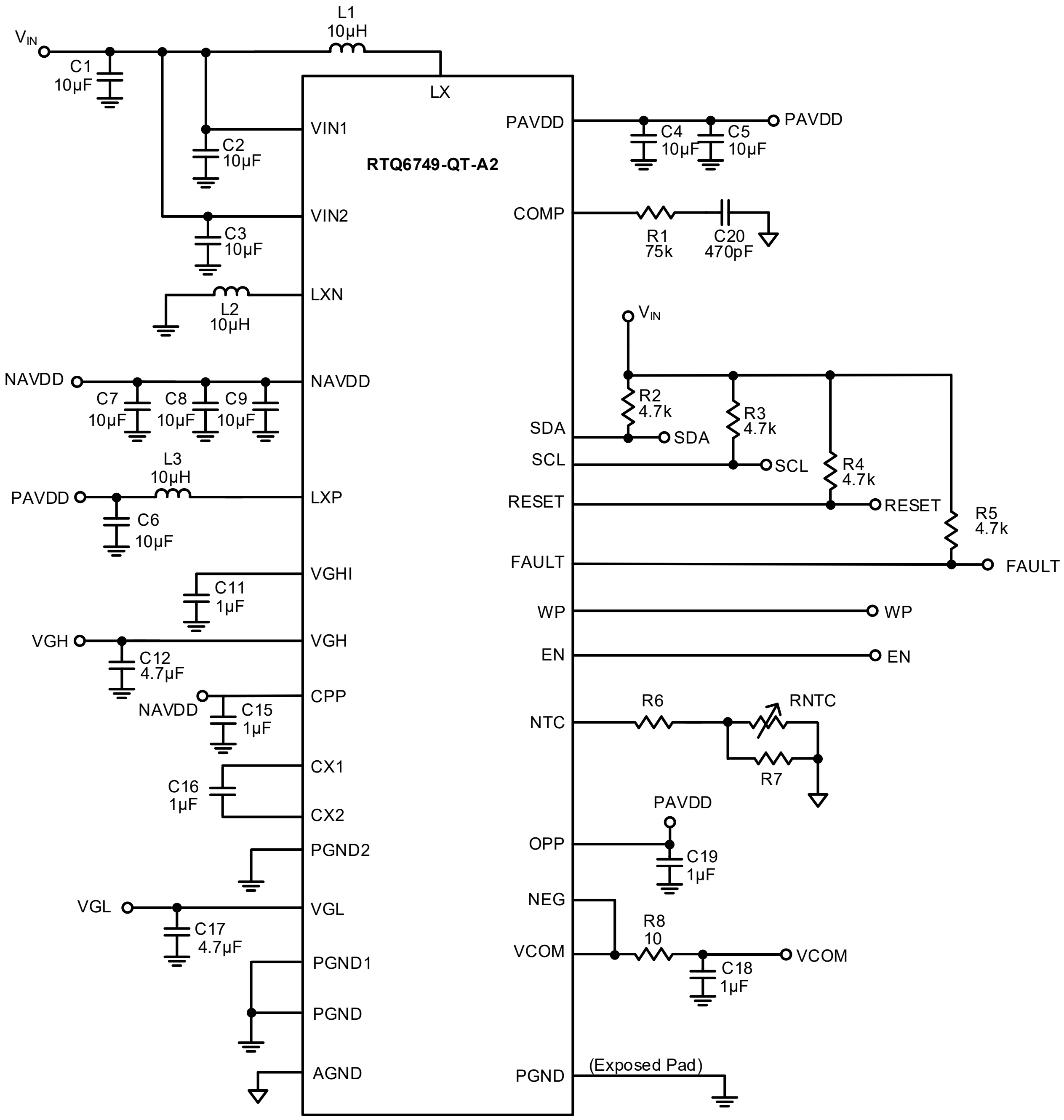


Figure 1. Typical Application Circuit with Internal Topology of VGL (PAVDD < |VGL| < PAVDD + |NAVDD|)

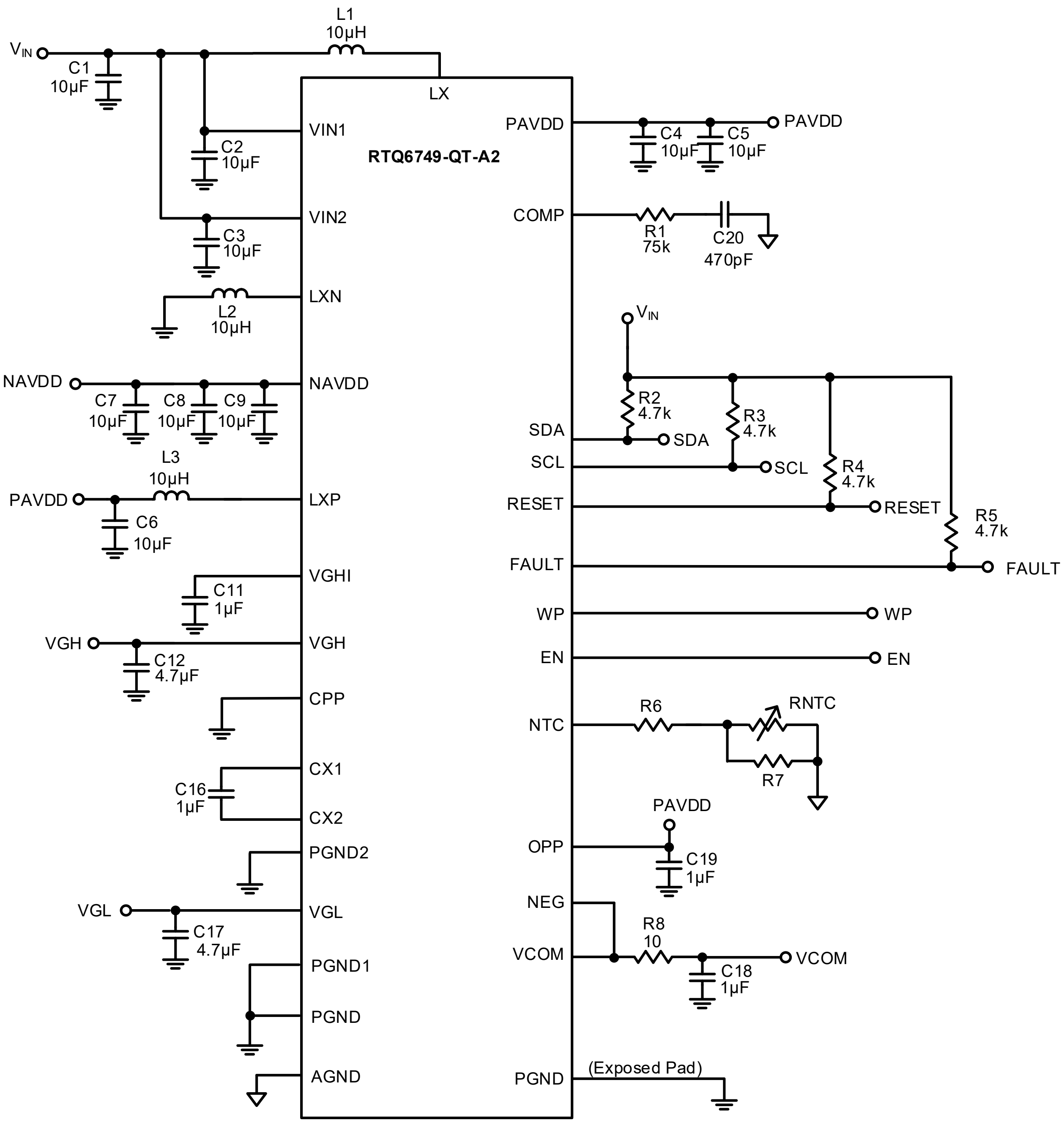


Figure 2. Typical Application Circuit with Internal Topology of VGL (|VGL| < PAVDD)

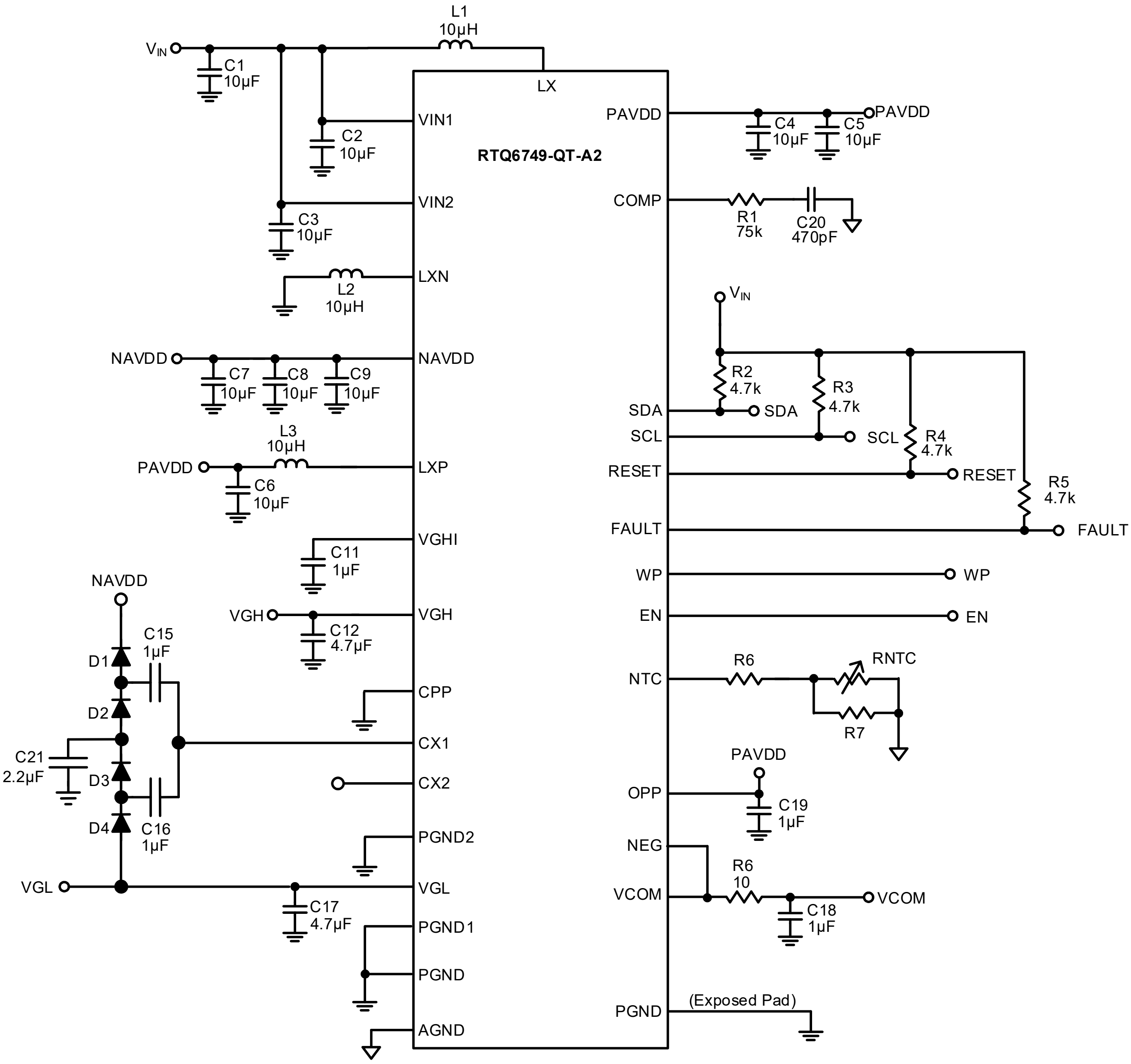


Figure 3. Typical Application Circuit with External Topology of VGL (|VGL| > PAVDD + |NAVDD|)

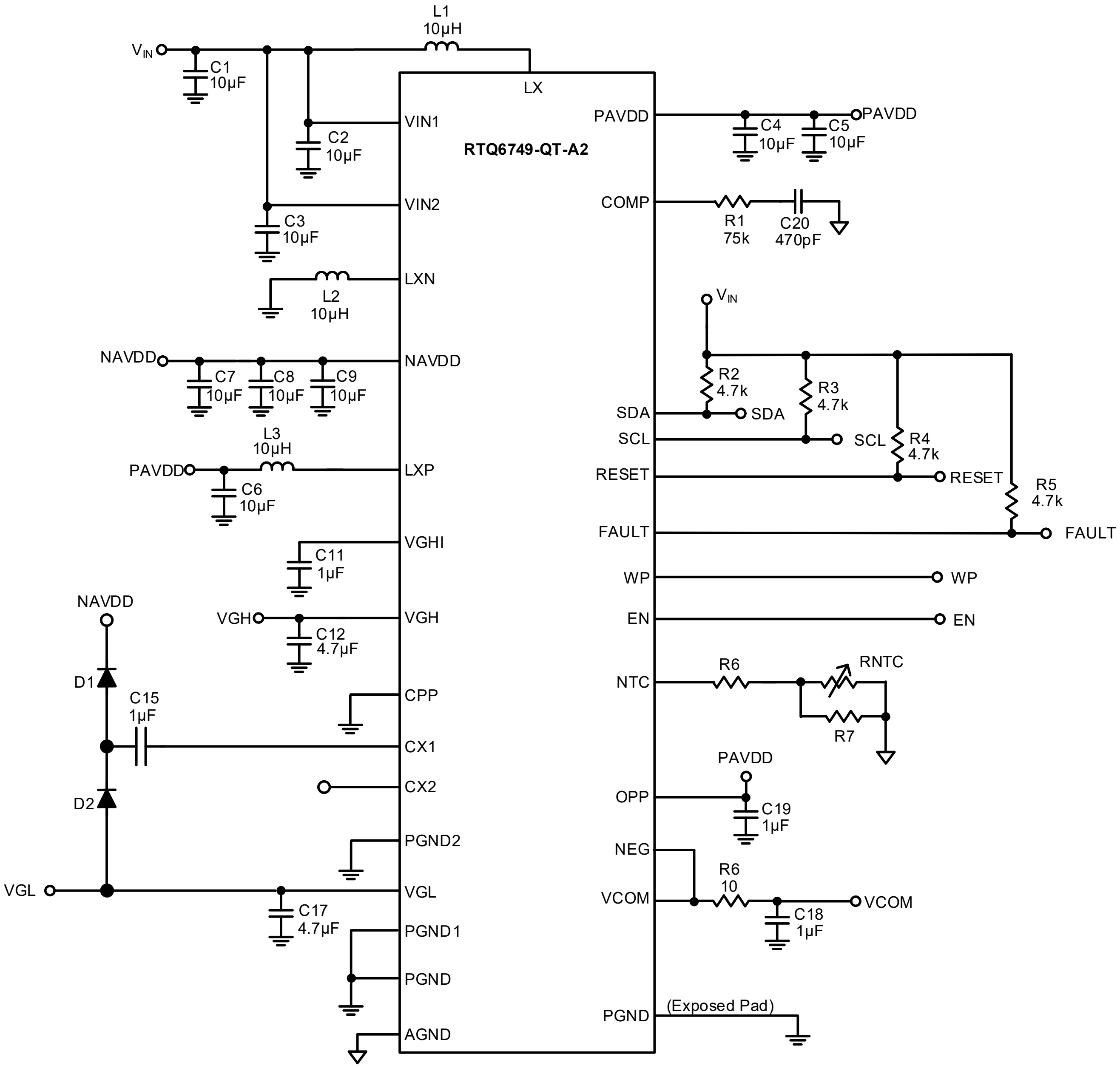


Figure 4. NAVDD Power Sequence Leading VGL Application Circuit with External Topology of VGL (PAVDD < |VGL| < PAVDD + |NAVDD|)

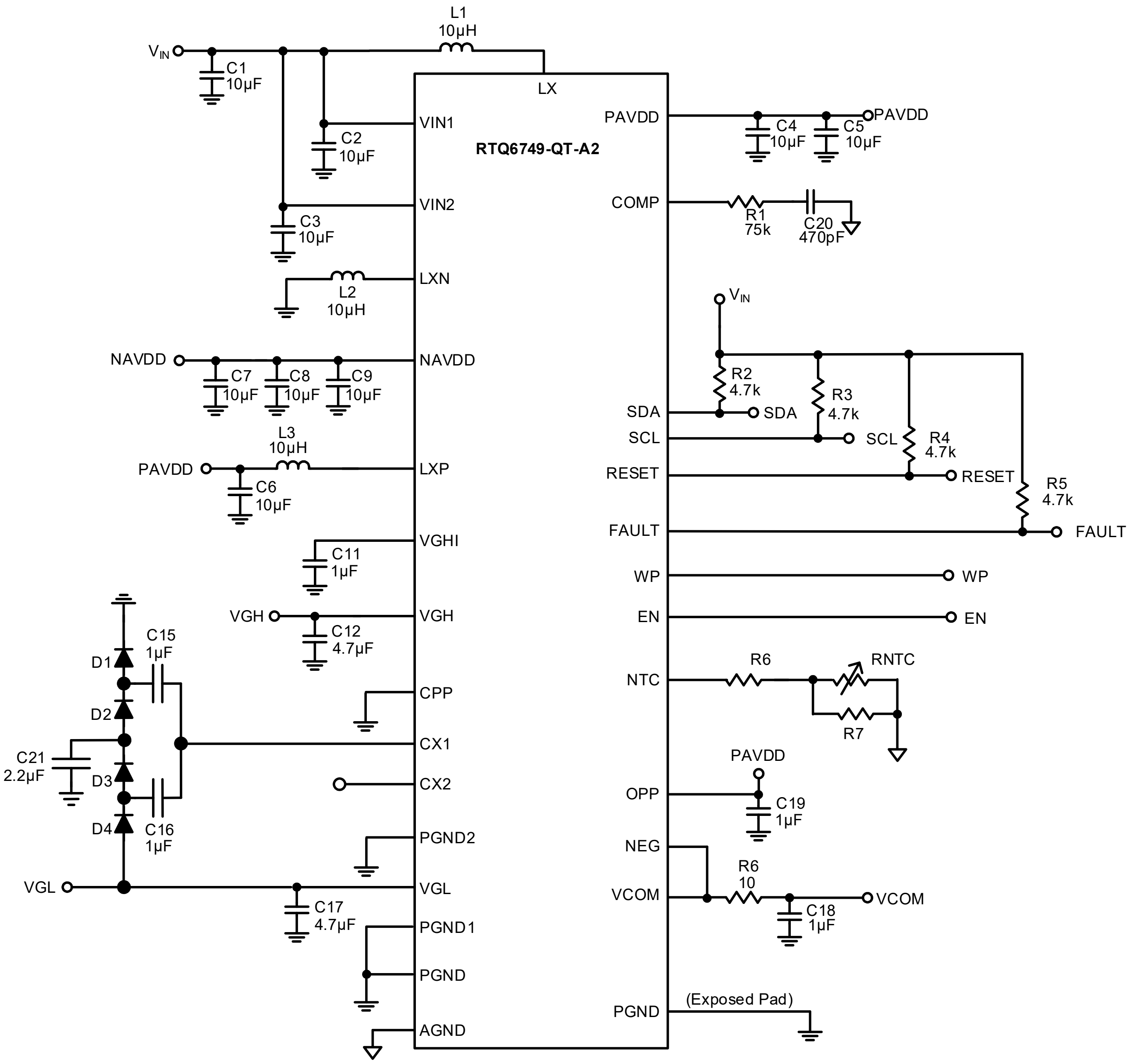


Figure 5. NAVDD Power Sequence Leading VGL and VGL Discharge Function Enabling Application Circuit with External Topology of VGL (PAVDD < |VGL|< 2 x PAVDD)

Note 8. The voltage output can be increased by adding a fly capacitor to achieve tripling the voltage output.

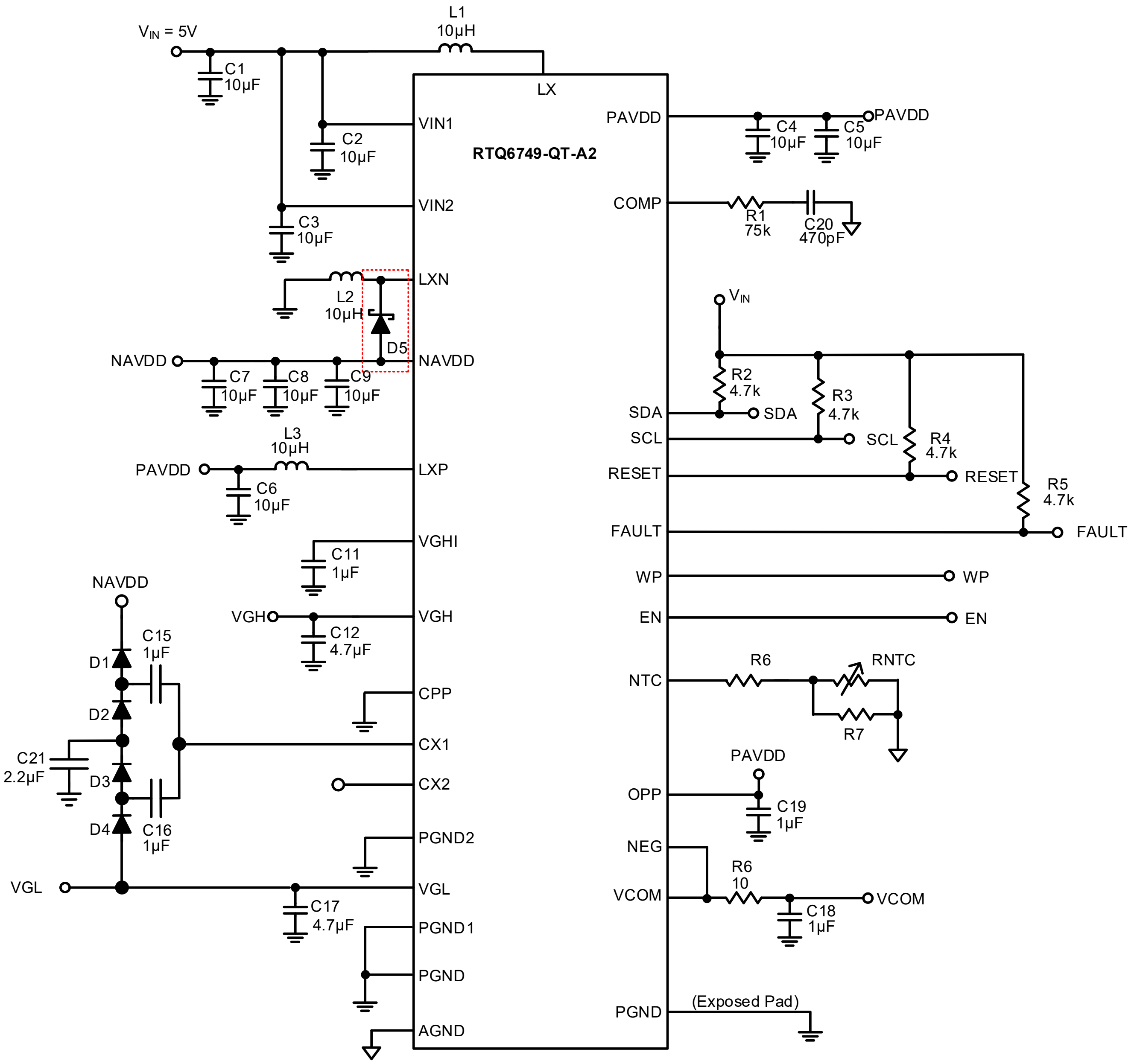


Figure 6. Typical Application Circuit with VIN > 4V Application

Table 1. Recommended Component List for Figure 1

Component	Part Number	Description	Package	Supplier
C1~C9	GRT21BC71C106KE13	10μF/16V/X7S/0805	2mmx1.25mmx1.25mm	MURATA
C11	GRT21BR71H105KE01	1μF/50V/X7R/0805	2mmx1.25mmx1.25mm	MURATA
C12	GRT32ER71H475KE01	4.7μF/50V/X7R/1210	3.2mmx2.5mmx2.5mm	MURATA
C15, C16, C18, C19	GRT188R71E105KE13	1μF/25V/X7R/0603	1.6mmx0.8mmx0.8mm	MURATA
C17	GRT32ER71H475KE01	4.7μF/50V/X7R/1210	3.2mmx2.5mmx2.5mm	MURATA
C20	GRT155R71H471KE01	470pF/50V/X7R/0402	1.0mmx0.5mmx0.5mm	MURATA
L1, L2, L3	VCHA042A-100MS6	10μH	4.5mmx4.3mmx2.1mm	CYNTEC

Table 2. VGL Application Condition with Circuit

<table>
<tr><th>VIN</th><th>VGL Conditions</th><th>Power Sequence</th><th>Circuit No.</th><th>LXN-NAVDD Schottky</th><th>14[5]</th><th>VGL D/C</th><th>CPP Connection</th><th>VGL Follow NAVDD at Power-Up</th></tr>
<tr><td rowspan="9">2.5V~4V (3.3V)</td><td rowspan="2">|VGL| < PAVDD</td><td>VGL → NAVDD</td><td rowspan="2">Figure 2</td><td rowspan="9">X</td><td>0</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td>NAVDD → VGL</td><td>0</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td rowspan="3">PAVDD < |VGL| < (PAVDD+|NAVDD|)</td><td rowspan="2">VGL → NAVDD</td><td>Figure 1</td><td>0</td><td>V</td><td>NAVDD</td><td>X</td></tr>
<tr><td rowspan="2">Figure 4</td><td>1</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td>NAVDD → VGL</td><td>1</td><td>X</td><td>GND</td><td>V</td></tr>
<tr><td rowspan="2">PAVDD < |VGL| < 2 x PAVDD</td><td>VGL → NAVDD</td><td rowspan="2">Figure 5</td><td>1</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td>NAVDD → VGL</td><td>1</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td rowspan="2">|VGL| > (PAVDD + |NAVDD|)</td><td>VGL → NAVDD</td><td rowspan="2">Figure 3</td><td>1</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td>NAVDD → VGL</td><td>1</td><td>X</td><td>GND</td><td>V</td></tr>
<tr><td rowspan="9">4V~5.5V (5V)</td><td rowspan="2">|VGL| < PAVDD</td><td>VGL → NAVDD</td><td rowspan="2">Figure 2 + Schottky</td><td rowspan="9">V</td><td>0</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td>NAVDD → VGL</td><td>0</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td rowspan="3">PAVDD < |VGL| < (PAVDD+|NAVDD|)</td><td rowspan="2">VGL → NAVDD</td><td>Figure 1 + Schottky</td><td>0</td><td>V</td><td>NAVDD</td><td>X</td></tr>
<tr><td rowspan="2">Figure 4 + Schottky</td><td>1</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td>NAVDD → VGL</td><td>1</td><td>X</td><td>GND</td><td>V</td></tr>
<tr><td rowspan="2">PAVDD < |VGL| < 2 x PAVDD</td><td>VGL → NAVDD</td><td rowspan="2">Figure 5 + Schottky</td><td>1</td><td>V</td><td>GND</td><td>X</td></tr>
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<tr><td rowspan="2">|VGL| > (PAVDD + |NAVDD|)</td><td>VGL → NAVDD</td><td rowspan="2">Figure 6</td><td>1</td><td>V</td><td>GND</td><td>X</td></tr>
<tr><td>NAVDD → VGL</td><td>1</td><td>X</td><td>GND</td><td>V</td></tr>
</table>

13 Timing Diagram

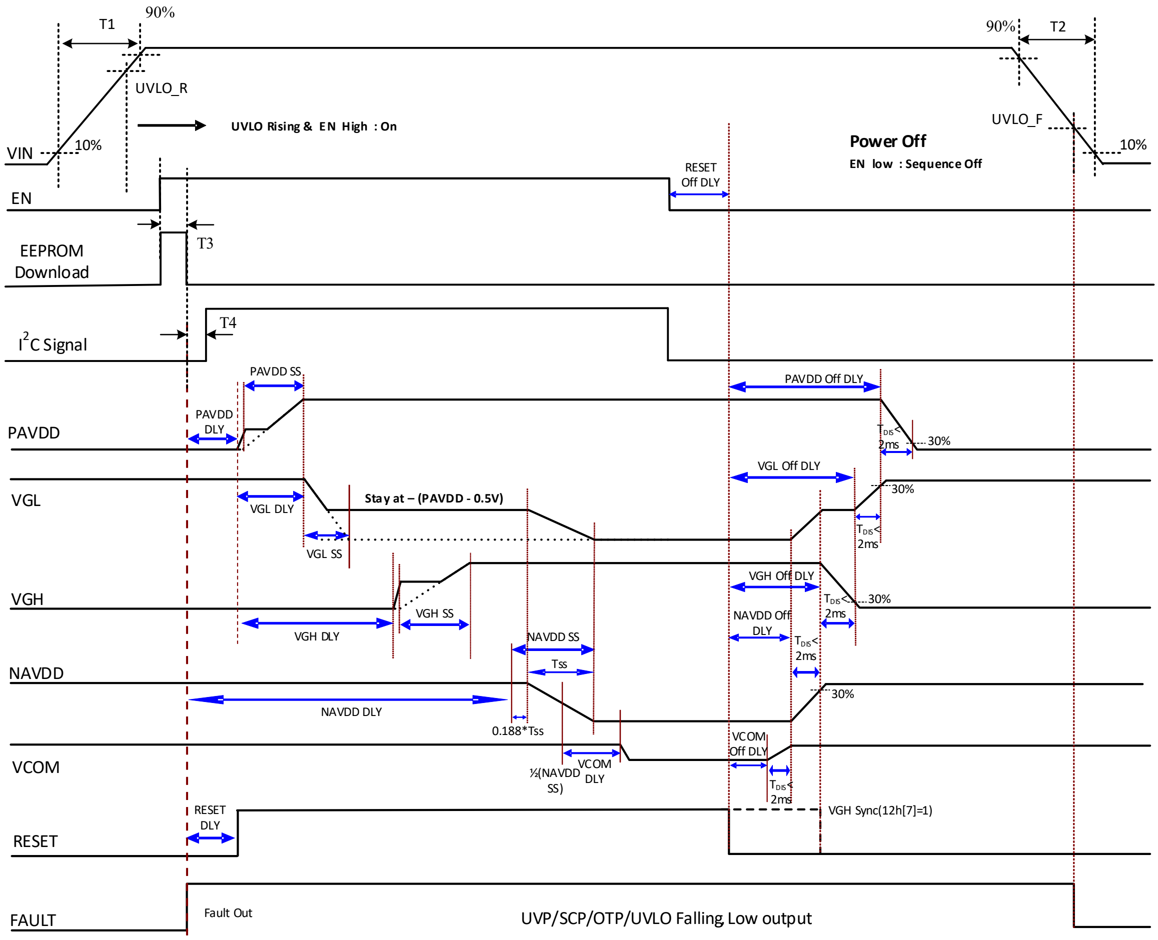


Figure 7. Power Sequence with Sequence Power-Off

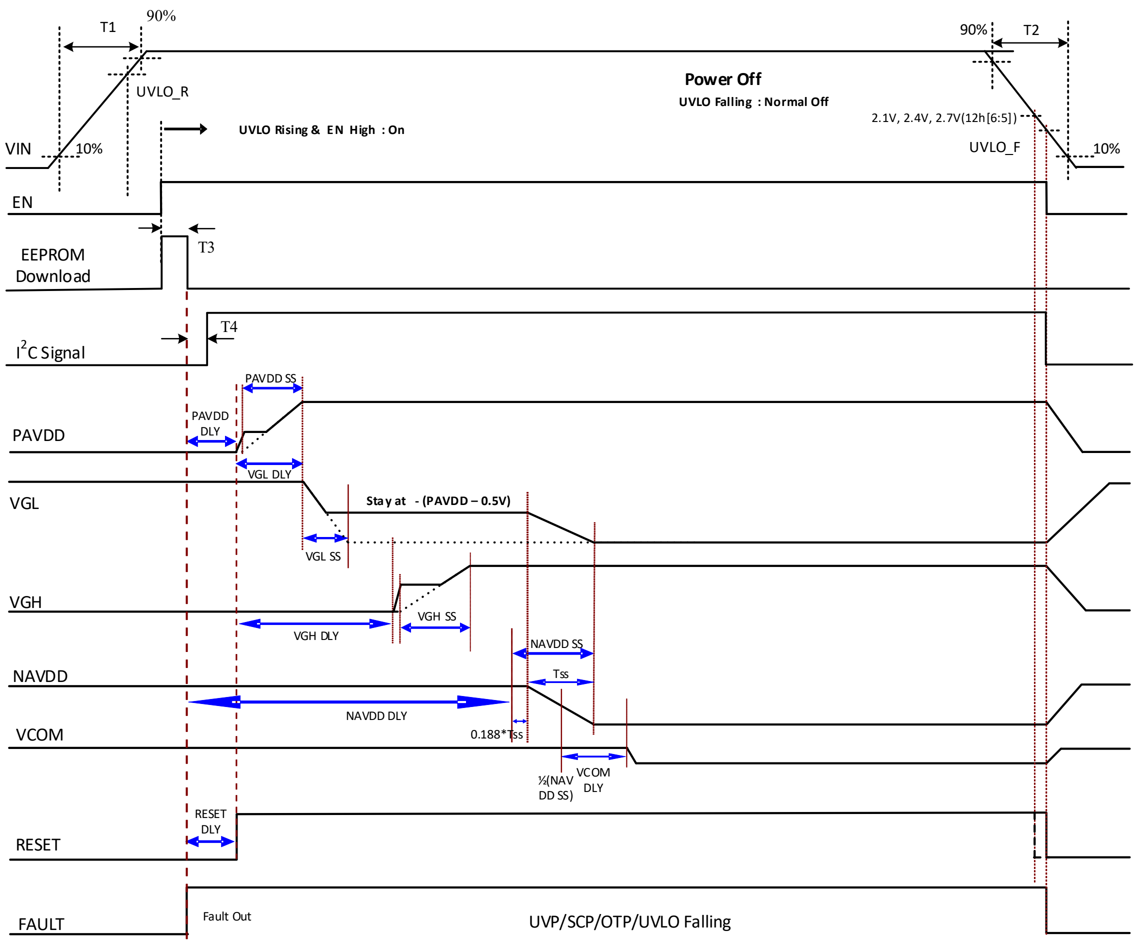


Figure 8. Power Sequence with Normal Power-Off

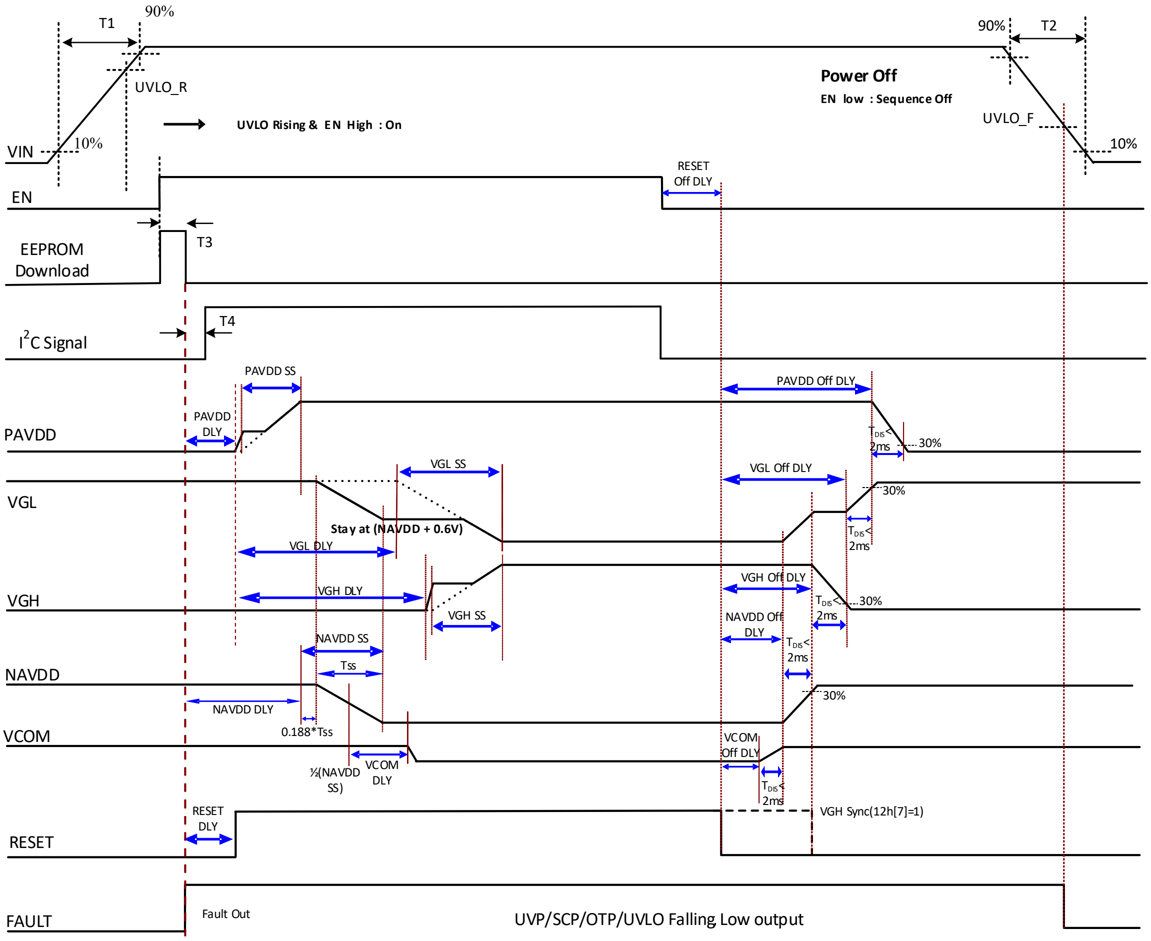


Figure 9. Power Sequence with NAVDD Leading VGL (External Topology)

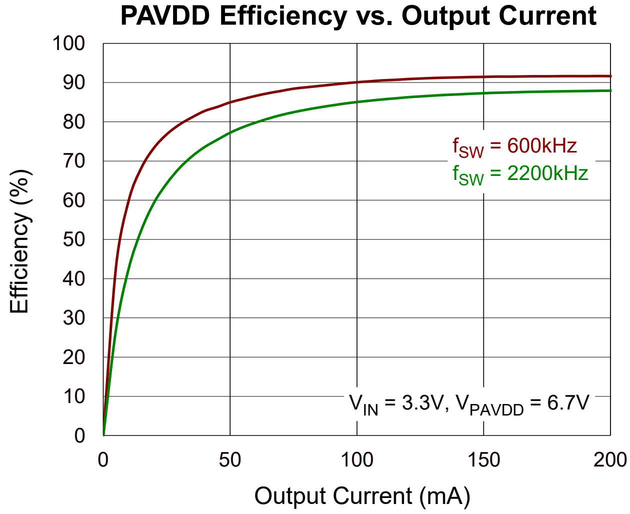
Symbol	Description	Min	Typ	Max	Unit
T1	VIN rising time	0.4	--	20	ms
T2	VIN falling time	0.5	--	3000	ms
T3	EEPROM download time	--	0.5	8 (Note 10)	ms
T4	I^{2}C setting time	--	1	--	ms

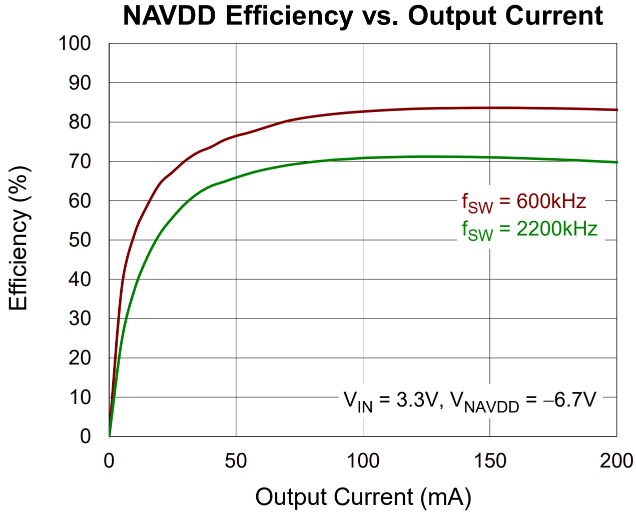
Note 9. Before IC power-up, the output voltage of each channel will be detected. If any output voltage is not below the SCP level, the IC will wait until the output voltages fall below the SCP level before powering-up in sequence.

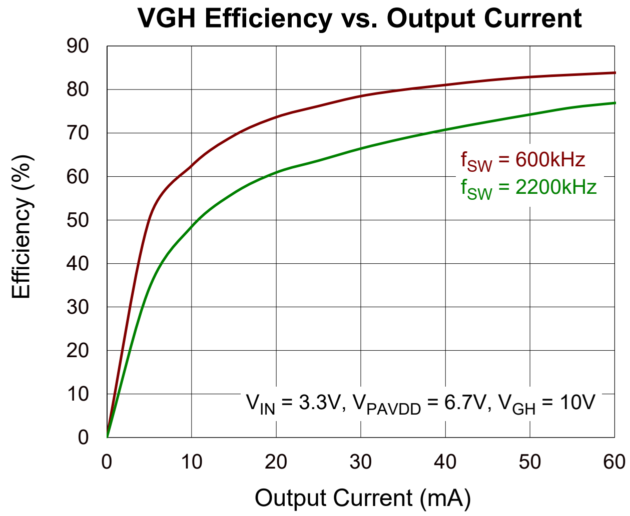
Note 10. Unstable VIN may trigger an extra delay mechanism during EEPROM download to ensure the accuracy. The maximum timeout period is 8ms.

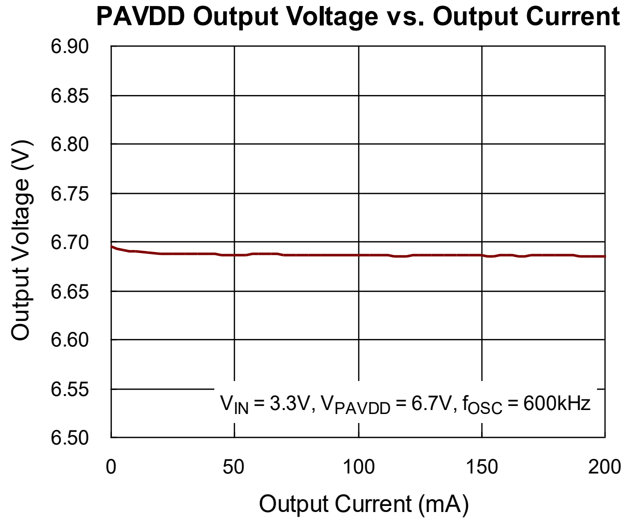
Note 11. Setting the VGH/VGL delay time to 0ms is only allowed when there is no additional load. If additional load is present, this setting may cause abnormal operation or reduce product reliability. Therefore, such configuration is not recommended.

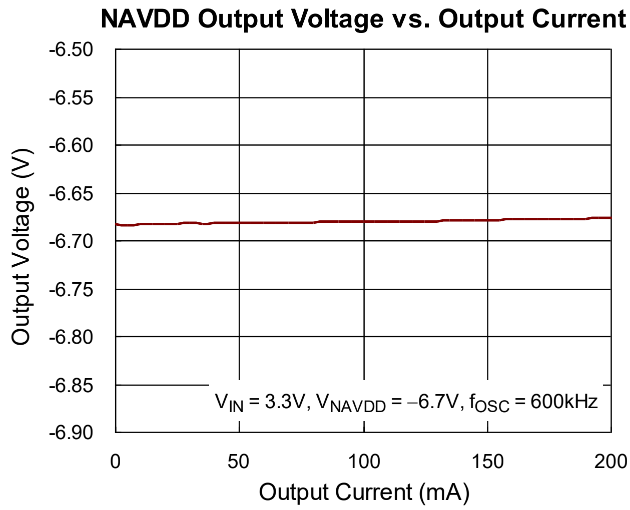
14 Typical Operating Characteristics

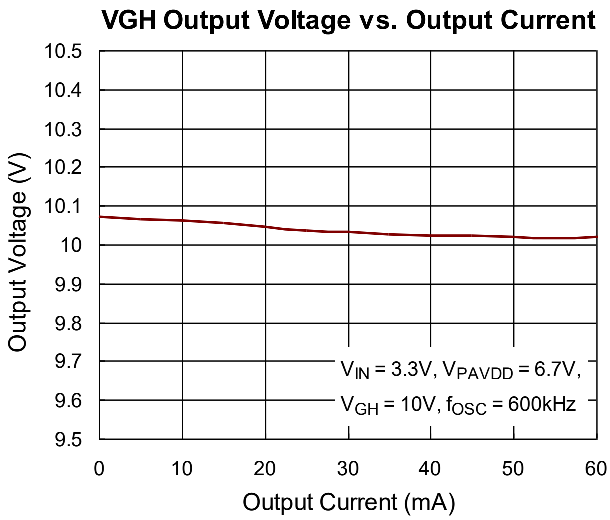




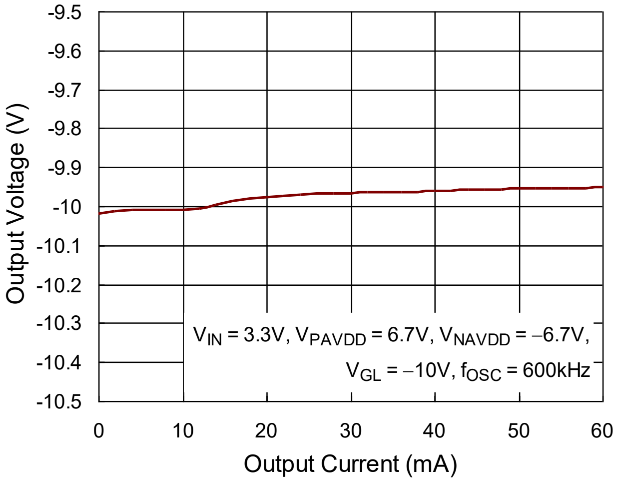




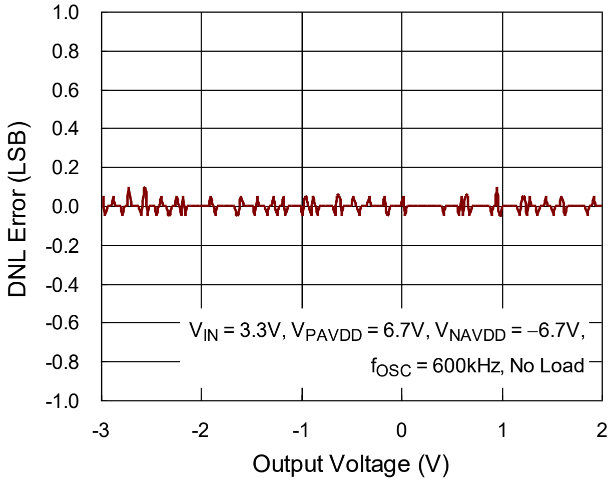




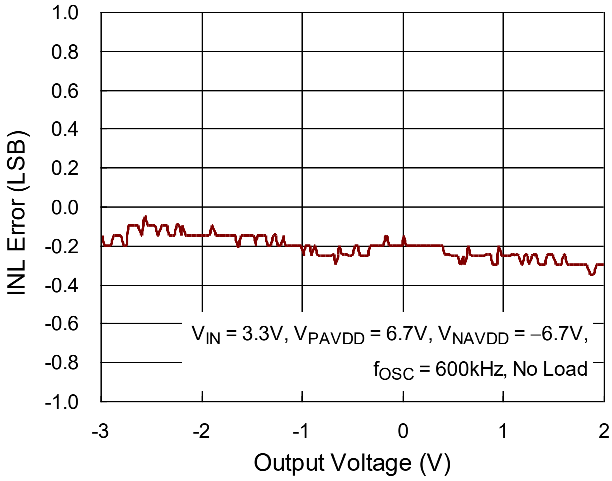
VGL Output Voltage vs. Output Current



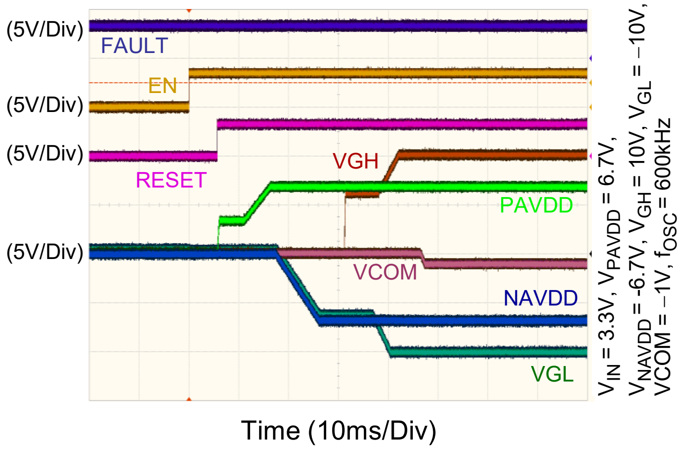
VCOM_C DNL Error vs. Output Voltage



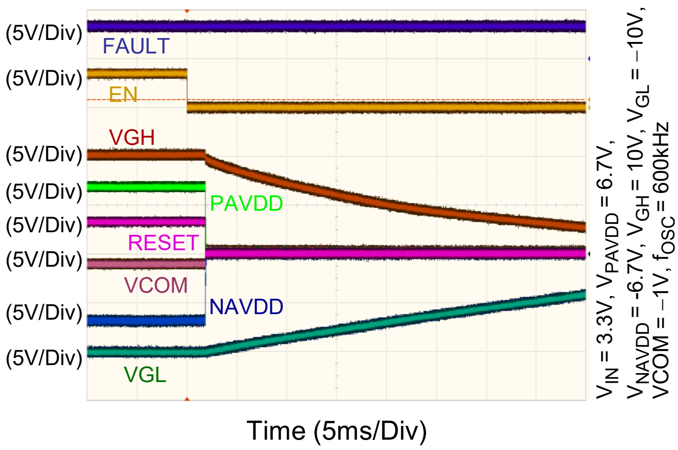
VCOM_C INL Error vs. Output Voltage



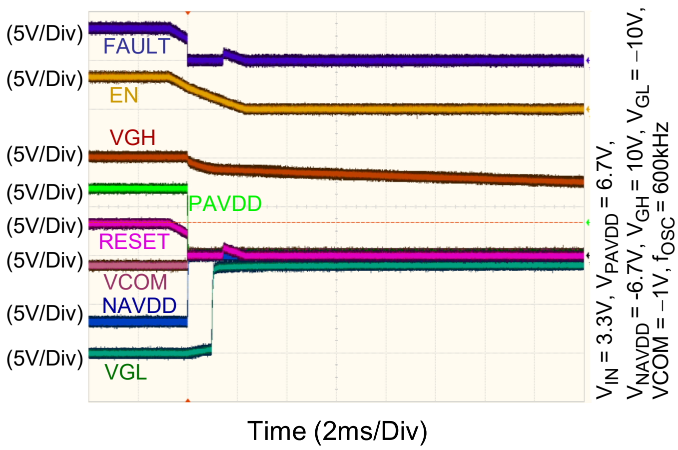
Power On



Power Off with Sequence-Off



Power Off with Normal-Off



15 Operation

The RTQ6749 is a programmable, multi-functional power solution with an I^2C interface designed for automotive TFT-LCD panels. It is versatile and can support a variety of panel applications.

The IC operates with input voltages ranging from 2.5V to 5.5V. The PAVDD boost converter is programmable from 5V to 7.3V, with a recommended compensation of 75kΩ and 470pF. The NAVDD negative buck-boost converter is programmable from −5V to −7.3V. The VGH boost converter is programmable from 7V to 30V and includes temperature compensation. The VGL negative charge pump is programmable from −6V to −18V. When setting the VGL voltage, it is important to ensure a 0.5V headroom with PAVDD, as shown in Figure 2. The VCOM operational amplifier is programmable from −3V to 2V, featuring a 8-bit programmable VCOM calibrator. The RESET voltage detector is programmable to UVLO_F/2.1V/2.4V/2.7V. The power-on delay time for all channels can be individually programmed and adjusted. The converter switching frequency can be set in four steps. Both the slew rate and frequency spread can be adjusted to improve EMI performance. The soft-start times for PAVDD, NAVDD, VGH, VGL can be configured by setting the channel delay time and soft-start time, as shown in Figure 7, Figure 8, and Figure 9. All channels can enable or disable the fast discharge function during power-off. To enable the discharge function, first refer to Table 2 to ensure successful power-on. When EN is triggered, all output voltages must be lower than SCP level; otherwise, a boot failure will occur.

16 Application Information

(Note 12)

The RTQ6749 is an integrated solution for automotive TFT-LCD panels, including PMIC and memory systems. The RTQ6749's I^2C slave address is 1101011. The PMIC (Power Management IC) provides 2 synchronous boost converters for PAVDD and VGH, one synchronous inverting converter for NAVDD, one negative charge pump for VGL, and one operational amplifier for VCOM. Power-on and power-off sequences are controlled by the EN input pin. Detailed timing sequence control is described in the “Timing Diagram”. The I^2C interface allows programming of each output channel, as well as sequence control and voltage settings.

16.1 Switching Frequency Setting

The switching frequency for each channel is set via the I^2C interface. It uses a 2-bit register with 4 selectable steps: 600kHz, 800kHz, 1MHz, and 2.2MHz. The default switching frequency is 600kHz (0x00). For more details, refer to the register map.

16.2 Undervoltage Protection (UVP)

The RTQ6749 is equipped with fault protection to shut down the IC if necessary. If any output voltage falls below 70% of its set value, an internal timer starts. If this fault condition continues for approximately 50ms, the IC will shut down. After UVLO or EN is reactivated, the fault protection is released. Protection begins after the soft-start of the output channel is complete. Output voltages must exceed the UVP threshold within 50ms after soft-start. Users can enable or disable this feature via register 14h[1]. Refer to Table 3, Table 4 and Register Map, for the location of the UVP registers for each channel.

16.3 Short Circuit Protection (SCP)

The RTQ6749 also features short circuit protection. During the power-on sequence, before each channel powers up, the output voltage of each channel must be below its respective SCP level. If not, the IC will wait until all output voltages fall below the SCP level before proceeding with the power-on sequence, as shown in Figure 11. The PAVDD_SCP_2 threshold for PAVDD is 1.26V (typical) before PAVDD soft-start. After soft-start, the SCP threshold becomes 30% of the voltage setting for PAVDD, and similar for the other channels. The determination point for output voltage below SCP is UVLO_R plus 1ms. During the PAVDD pre-charge stage, the PAVDD SCP is also checked after the PAVDD power-on delay counting is finished, plus an additional 4ms. The SCP function is active during the soft-start period. If the PAVDD voltage is below PAVDD_SCP_2 (1.26V_typical), the IC will be protected at the end of the delay counting plus 4ms, as shown at point “c” in Figure 12.

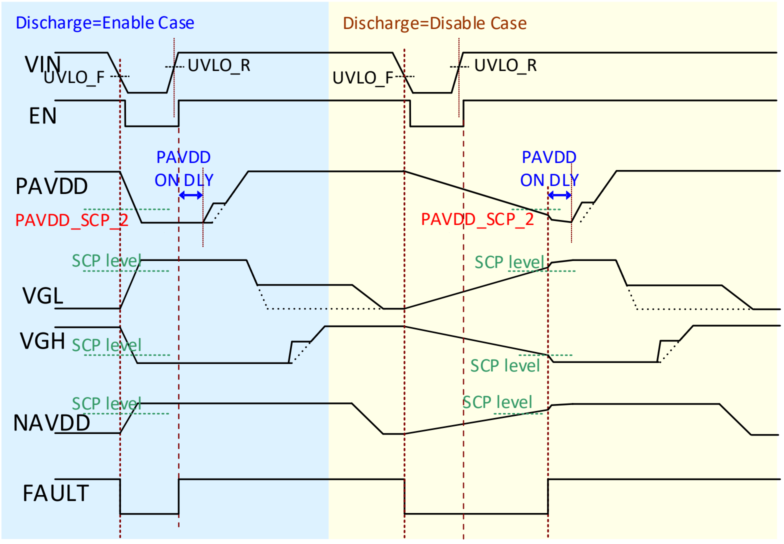


Figure 10. Power-up Limitation: Output Voltage Must Be Below the SCP Level

The completion of pre-charging is determined by monitoring the voltage difference between PAVDD and VIN. When the difference is less than 0.2V (typical), pre-charging is considered complete, and the IC will proceed to the soft-start stage. The SCP for the other channels is enabled after the soft-start of each channel is finished.

In another case, if the PAVDD voltage is above PAVDD_SCP_2 but pre-charging completion is not met, the IC will remain in the pre-charge stage until the condition is satisfied. Once the condition is met, the IC will enter the soft-start stage, as shown in Figure 13.

If the output voltage falls below 30% of the output voltage during the operation stage, the high-/low-side MOSFET will stop switching immediately, as shown at point “a” in Figure 13. The other channels will stop switching after 100μs, and the FAULT pin will go low at point “b”.

Protection is released after UVLO or EN is reactivated. Users can enable or disable this function via register 14h[0] However, the initial PAVDD_SCP_2 detection during a new power-on sequence, as shown in Figure 10, cannot be disabled by 14h[0].

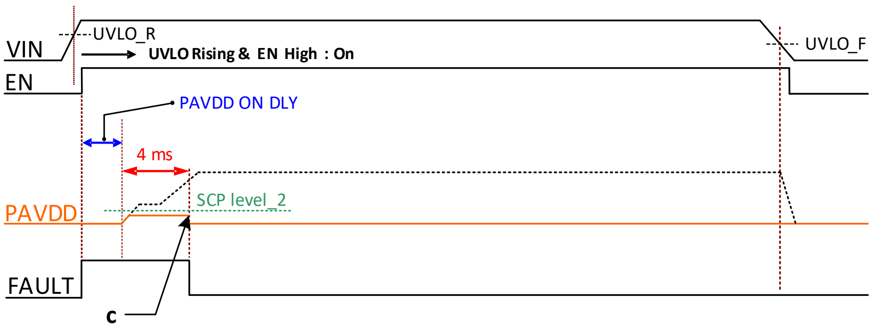


Figure 11. SCP Mechanism When PAVDD Pre-Charge Under Abnormal Heavy Load Conditions

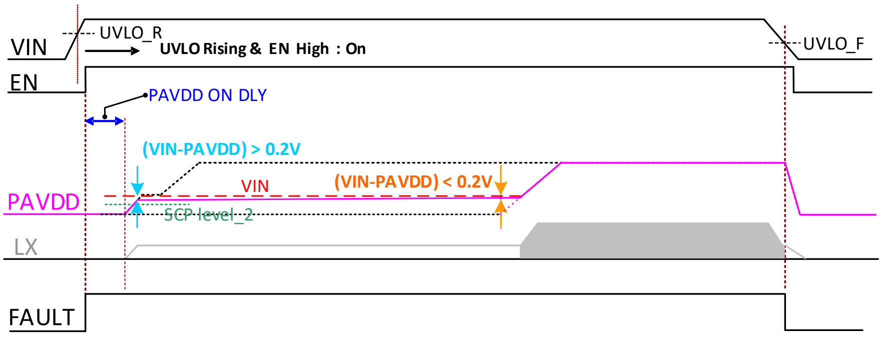


Figure 12. SCP Mechanism When PAVDD Is Between the SCP Level and Pre-Charge Completion

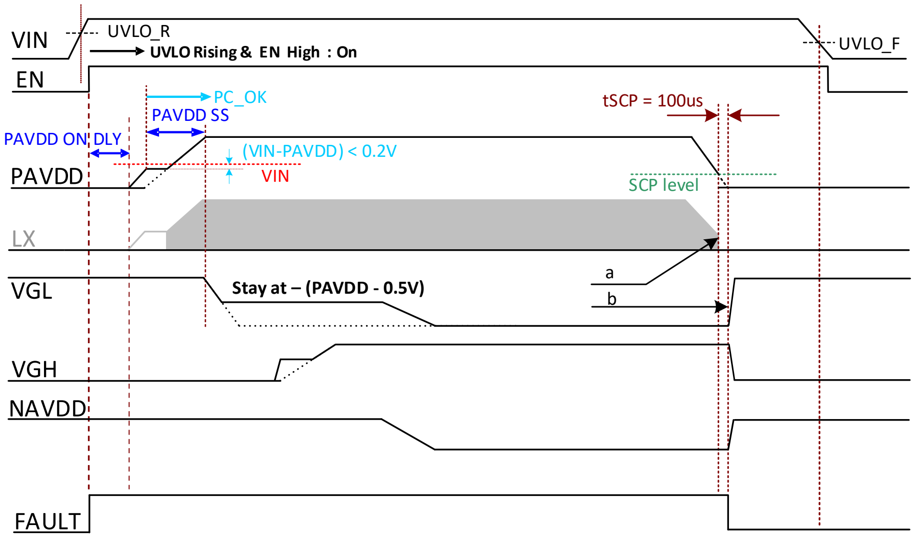


Figure 13. SCP Mechanism during Normal Operating

16.4 Over-Temperature Protection (OTP)

The RTQ6749 is equipped with over-temperature protection (OTP) to prevent excessive power dissipation and device overheating. The OTP disables switching operation when the junction temperature exceeds approximately 150°C. All output channels will resume operation once the junction temperature decreases by approximately 20°C, thereby preventing the maximum junction temperature from exceeding around 150°C and maintaining continuous operation. The OTP can be enabled or disabled by setting the register 14h[2].

16.5 PAVDD Synchronous Boost Converter

The PAVDD synchronous boost converter utilizes a high-efficiency PWM architecture with a programmable switching frequency. It provides fast transient responses to meet the requirements of source driver supplies in TFT-LCD displays. The high operating frequency minimizes interference with the AM radio band. The output voltage is adjustable via a 6-bit register, offering 47 discrete steps. The error amplifier regulates the output voltage by adjusting the COMP voltage based on feedback from the PAVDD pin.

16.5.1 PAVDD Slew Rate Setting

The falling slew rate of the PAVDD LX can be controlled via the I^2C interface to optimize efficiency and EMI performance. The adjustable options are Slowest, Slow, Normal, and Fast, with the default set to the Normal. For more details, refer to the register map.

16.5.2 PAVDD Output Voltage Setting

The PAVDD output voltage is configured via the I^2C interface. Users can write to register 00h[5:0] to set the PAVDD output voltage. This 6-bit register allows adjustment of the output voltage from 5 V to 7.3 V in approximately 50 mV steps. The default PAVDD voltage is 6.7V (0x22). For detailed instructions on adjusting the output voltage, refer to the register map.

16.5.3 PAVDD Soft-Start Time Setting

The soft-start time for PAVDD can be adjusted using the 08h[2:0] register, which consists of 3 bits and 8 selectable steps. The soft-start time setting range is from 5ms to 40ms, with each step approximately 5ms. The default soft-start time is 10ms (0x01). The soft-start mechanism follows the reference voltage, starting from the initial slope down to 0 V, and completes when the PAVDD output voltage is ready. For more details, refer to Figure 7 and the register map.

16.5.4 PAVDD Power-On Delay Time Setting

The PAVDD power-on delay time is adjustable via the I^2C interface. There are 16 steps within the 4-bit register of 07h. The delay time setting range is from 0ms to 75ms, with each step approximately 5ms. The default delay time is 5ms (0x01). The delay time is measured from the completion of MTP data loading to the start of the PAVDD output voltage rising. For more details, refer to Figure 7 and the register map.

16.5.5 PAVDD Overcurrent Protection

The RTQ6749 features peak current limiting to provide overcurrent protection. The IC senses the inductor current during the on-time, which flows into the LX pin. The minimum current limit is 1.5A. When the peak inductor current reaches the current limit threshold, the internal N-MOSFET is turned off. The output current at the current limit boundary, denoted as $I_{OUT(CL)}$, can be calculated using the following equation:

$$I_{OUT(CL)} = \eta \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{CL} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

where η is the efficiency of the PAVDD synchronous boost converter, I_{CL} is the value of the current limit, and T_S is the switching period.

16.5.6 PAVDD Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisting of R1 and C20. Select R1 to set the high-frequency integrator gain for fast transient response, and choose C20 to set the integrator zero for loop stability. The recommended values are 75kΩ for R1 and 470pF for C20 in most applications.

16.6 Synchronous Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current is typically set to 20% to 40% of the maximum input current. For example, if 40% is selected, the inductor ripple current can be calculated using the following equation:

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the synchronous boost converter, $I_{IN(MAX)}$ is the maximum input current, and I_{RIPPLE} is the inductor ripple current. The input peak current can be calculated by adding the half of the inductor ripple current to the maximum input current, as shown in the following equation:

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Ensure that the inductor's saturated current rating exceeds I_{PEAK}. The required inductance can be determined using the following equation:

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the PAVDD switching frequency. For better system performance and to minimize EMI, a shielded inductor is recommended.

16.7 Synchronous Boost Output Capacitor Selection

The output ripple voltage is a key parameter for evaluating performance. This portion consists of two parts: one is the product of $(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT})$ and the ESR of the output capacitor, and the other part is the voltage ripple caused by the charging and discharging of the output capacitor. Refer to Figure 15 to evaluate ΔV_{OUT1} using ideal energy equalization. According to the definition of Q, the Q can be calculated using the following equation:

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

where T_S is the inverse of the switching frequency and ΔI_L is the inductor ripple current. Move C_{OUT} to the left side to estimate the value of ΔV_{OUT1} using the following equation:

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

To account for ESR, the ESR-induced voltage ripple (ΔVESR) can be calculated as follows:

$$\Delta V_{ESR} = \left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D \times T_{OSC}}{2L} \right) \times R_{ESR}$$

The total output ripple voltage, ΔV_{OUT}, is the sum of ΔV_{OUT1} and ΔV_{ESR}:

$$\Delta V_{OUT} = \Delta V_{OUT1} + \Delta V_{ESR}$$

For typical applications, it is recommended to use three 10μF/X7R/1206 capacitors for the PAVDD output, ensuring a total effective output capacitance of at least 13μF. For VGH, the effective output capacitance should be at least 2.1μF. A 4.7μF/50V/X7R/1210 capacitor is recommended for general applications. To further reduce VGH ripple, a higher capacitance value may be used; however, designers should consider the worst-case input inrush current when increasing VGH capacitance, as illustrated in Figure 14.

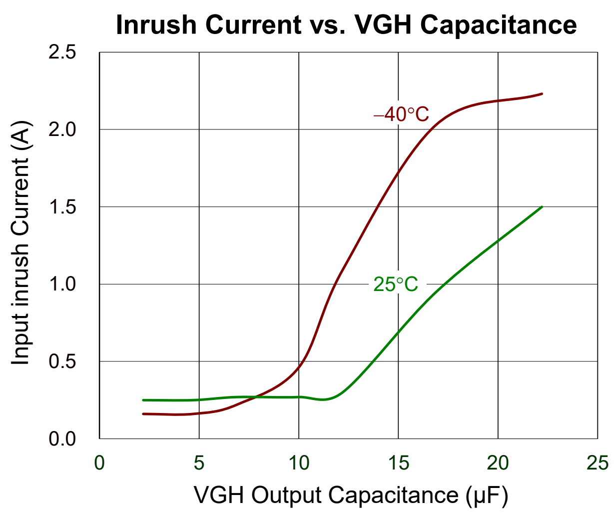


Figure 14. Inrush Current vs. VGH Capacitance

A higher inrush current, combined with increased input power trace resistance, may cause an input voltage drop sufficient to trigger the IC's input UVLO protection.

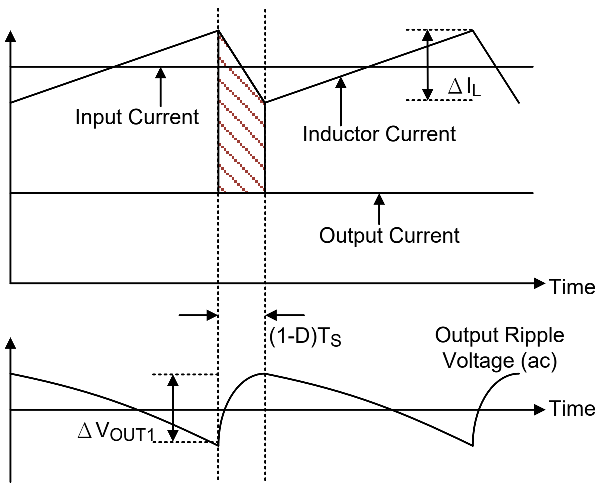


Figure 15. The Output Ripple Voltage without the Contribution of ESR

16.8 VGH Synchronous Boost Converter

The VGH synchronous boost converter features a high-efficiency PWM architecture with programmable switching frequency, output voltage, power-on delay time, and soft-start time, all configurable via the I^2C interface. The VGH integrates a GD MOSFET at the output for sequence control.

16.8.1 VGH Soft-Start Time Setting

The VGH synchronous boost converter includes an integrated soft-start function to reduce the input inrush current during power-up. The soft-start time can be set through the 0Ch[1:0] register using the I^2C interface. The 2-bit register provides four selectable soft-start times:5ms, 10ms, 15ms, and 20ms, with each step corresponding to approximately 5ms. The soft-start mechanism follows the reference voltage during startup. The soft-start begins at the initial slope and continues until the voltage crosses 0V, completing when the VGH output voltage is ready. For more details, refer to Figure 7 and the register map.

16.8.2 VGH Power-On Delay Time Setting

The VGH boost converter includes an integrated power-on delay function. The delay time can be adjusted via the I^2C interface by writing to the 0Bh[3:0] register. This 4-bit register provides 16 options, allowing the delay time to be set from 0ms to 75ms in approximately 5ms steps. The delay period is defined as the time from the start of the PAVDD soft-start to when the VGH output voltage begins to rise. If the VGH delay time is set to 0ms, the VGH will wait for the PAVDD pre-charge to finish before proceeding with its own pre-charge. For more details, refer to Figure 7 and the register map.

16.8.3 VGH Overcurrent Protection

The RTQ6749 provides peak current limiting for overcurrent protection. The IC senses the inductor current during the on-time, which flows into the LXP pin. The typical current limit is 0.7A. When the peak inductor current reaches 0.7A, the internal N-MOSFET is turned off. The output current at the current limit boundary, denoted as $I_{OUT(CL)}$, can be calculated using the following equation:

$$I_{OUT(CL)} = \eta_P \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{CL} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

where η_P is the efficiency of the VGH boost converter, I_{CL} is the current limit value, and T_S is the switching period.

16.8.4 VGH Synchronous Boost Loop Compensation

The VGH boost converter's loop compensation network is integrated within the RTQ6749, and the compensation setting is fixed.

16.8.5 VGH Voltage Setting

The VGH voltage is programmable via the I^2C interface. Users can write data into the 02h[5:0] register to set the VGH voltage. The 02h register is for the VGH voltage of TH. The TH is the temperature point of started compensated temperature. Refer to Figure 16 for clarity. The voltage setting range is from 7V to 30V. The default value of VGH is 10V (0x06). Each voltage step is approximately 0.5V. It is integrated with protection; when VGH is too close to PAVDD, VGH will automatically adjust the output voltage to maintain a difference equal to or greater than 2V between PAVDD and VGH. Refer to the register map for details.

16.8.6 VGH_LT Voltage Setting

The VGH_LT voltage is programmable via the I^2C interface. Users can write to the 05h[1:0] register to set the VGH_LT voltage, which defines the VGH voltage of TL, the temperature point where compensation stops. The VGH voltage at TL is equal to VGH+VGH_LT, and the VGH_LT setting determines only the difference. The setting range is from 2V to 8V, with each step approximately 2V. The default value is 2V (0x00). Refer to Figure 16 and the register map for details.

16.8.7 VGH Temperature Compensation

The RTQ6749 includes a temperature compensation feature for the VGH output voltage. When the temperature drops below TH, the VGH output voltage gradually transitions from the value set at TH to the value at TL. Once the temperature reaches TL, the VGH output voltage is equal to the value set for TL. Compensation is achieved by controlling the feedback voltage (V_{FBP}), which is sensed at the VGH pin through an internal divider. The VFBP can be compensated using an external thermal sensing element (R_{NTC}) and resistors (R6, R7), which determine the temperature at which the compensation starts and the compensation slope. The RNTC, R6, and R7 are shown in the "Typical Application Circuit," and the temperature compensation curve is shown in Figure 16.

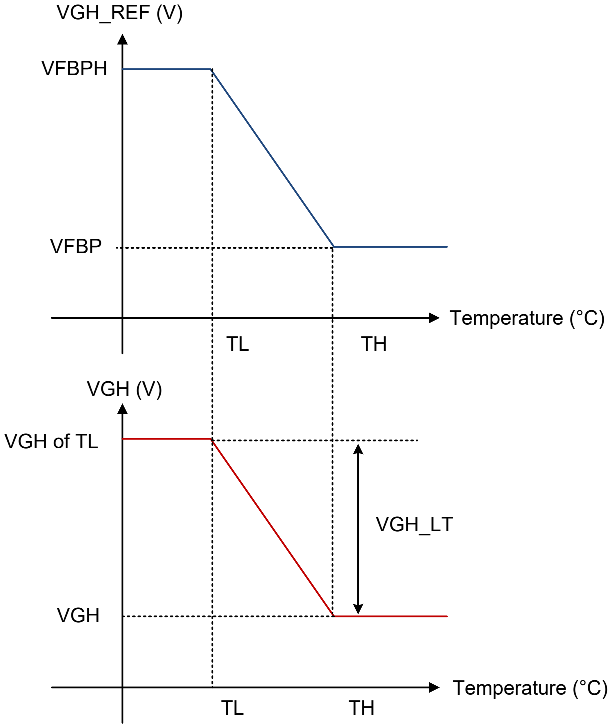


Figure 16. VGH Temperature Compensation Curve

where V_{FBPH} is the feedback voltage at TL, TH is the temperature point where compensation starts, and TL is the temperature point where compensation stops.

The NTC pin sources a current of approximately 20μA (I_{NTC}), from IC internal constant current source. The equivalent resistance of R_{NTC}, R6, and R7 (R_{ENTC}) can be calculated using the 20μA current.

$$V_{FBP} = I_{NTC} \times R_{ENTC\_H} \quad (1)$$

$$V_{FBPH} = I_{NTC} \times R_{ENTC\_L} \quad (2)$$

Based on the above-described relationship, the values of R6 and R7 can be determined using the following equation:

$$R7 = \frac{-B+\sqrt{B-4AC}}{2A}$$

$$R6 = R_{ENTC\_H} - \frac{R7 \times R_{ENTC\_H}}{R7 + R_{ENTC\_H}}$$

$$A = R_{ENTC\_H} - R_{ENTC\_L} - R_{NTC\_H} + R_{NTC\_L}$$

$$B = (R_{ENTC\_H} - R_{ENTC\_L}) \times (R_{NTC\_H} + R_{NTC\_L})$$

$$C = (R_{ENTC\_H} - R_{ENTC\_L}) \times R_{NTC\_H} \times R_{NTC\_L}$$

where R_{ENTC_H} is the equivalent resistance value of R_{NTC}, R6, and R7 at TH, R_{ENTC_L} is the equivalent resistance value of R_{NTC}, R6, and R7 at TL, R_{NTC_H} is the resistance value of R_{NTC} at TH, and R_{NTC_L} is the resistance value of R_{NTC} at TL.

16.9 VGL Negative Charge Pump Regulator

The VGL negative charge pump regulator is programmable for soft-start time, output voltage, switching frequency, and power-on delay time via the I^2C interface. It also features fault protection to prevent sudden output overload.

16.10 VGL Output Voltage Setting

The VGL output voltage is adjusted via the I^2C interface. Users can write to the 03h[5:0] register to set the VGL output voltage. This 6-bit register allows adjustment from –6V to –18V approximately –250mV steps. The default output voltage is about –10V (0x10). Refer to the register map for details.

Because the VGL voltage is derived from PAVDD and NAVDD, the maximum VGL output voltage is limited by PAVDD + |NAVDD|. The VGL regulator provides 3 configuration options: If |VGL| < PAVDD, it is recommended that the CPP should be connected to GND, as shown in Figure 2. If the NAVDD powers on before VGL (i.e., (VGL – NAVDD) ≥ 0.3 V during soft-start), use external mode (set 14h[5] = 1) and connect CPP to GND, as shown in Figure 4. If PAVDD < |VGL| < (PAVDD + |NAVDD|), the CPP should be connected to NAVDD, as shown in Figure 1. If |VGL| > (PAVDD + |NAVDD|), switch to external mode and use an external diode structure, as shown in Figure 3.

When using internal mode, ensure sufficient headroom for voltage regulation. The headroom can be calculated using the following equation:

$$\text{Headroom} \geq I_{OUT\_Max} \times 12\text{mV}$$

$$|V_{GL}| < V_{PVDD} + |V_{NVDD}| - \text{Headroom}$$

where V_{PAVDD} is the PAVDD output voltage, and V_{NAVDD} is the NAVDD output voltage.

If the |VGL| voltage is higher than PAVDD + |NAVDD|, external mode is recommended. Set register 14h[5] from 0 to 1. In this mode, the VGL output voltage is also limited by PAVDD, NAVDD, and the forward voltage (V_F) of the external diode. The V_F varies with forward current and ambient temperature; use the maximum V_F value for calculations. The VGL voltage setting should satisfy the following equation:

$$\text{Headroom} \geq I_{OUT\_Max} \times 12\text{mV}$$

$$|V_{GL}| < 2 \times V_{PVDD} + |V_{NVDD}| - \text{Headroom} - (V_{F\_max} \times 4)$$

where the V_{F_max} is maximum forward voltage of the diode.

16.11 VGL Soft-Start Time Setting

The VGL negative charge pump regulator includes an integrated soft-start function to reduce input inrush current at power-on. The soft-start time can be adjusted using register 0Ah[2:0], which provides 8 steps from 3ms to 24ms, with each step approximately 3ms. The default soft-start time is 9ms (0x02). The soft-start time period begins when the VGL voltage starts to fall and ends when the slope of the soft-start crosses the set level. Refer to Figure 7 and the register map for details.

16.12 VGL Power-On Delay Time Setting

The negative charge pump regulator includes integrated power-on sequence control. The VGL power-on delay time is adjustable via the I^2C interface, using the 4-bit register 09h[3:0]. The delay time can be set from 0ms to 75ms in approximately 5ms steps. The default setting is 25ms (0x05). The delay period is defined as the time from the start of the PAVDD soft-start to when the VGL output voltage begins to fall. If the VGL delay time is set to 0ms, the VGL soft-start will wait for the PAVDD pre-charge to finish before proceeding. Refer to Figure 7 and the register map for details.

16.13 VGL Output Capacitor Selection

For optimal output voltage filtering, low-ESR ceramic capacitors are recommended. A 4.7μF/X7R/1206 capacitor is suitable for most applications, provided the effective capacitance is at least 4μF. Additional capacitors can be added in parallel to further reduce output voltage ripple.

16.14 NAVDD Synchronous Buck-Boost Converter

The NAVDD synchronous buck-boost converter features a high-efficiency PWM architecture with a programmable switching frequency. It provides fast transient responses to meet the requirements of source driver supplies for TFT-LCD displays. The high operating frequency helps prevent interference with the AM radio band. The output voltage is controlled by a 6-bit register with 47 steps. For applications with VIN > 4V, the asynchronous topology should be used, as shown in Figure 6, to achieve better performance.

16.14.1 NAVDD Power-On Delay Time Setting

The NAVDD power-on delay time is adjustable via the I^2C interface using the 4-bit register 0Dh[3:0], which provides 16 steps. The delay time can be set from 0ms to 75ms in approximately 5ms increments. The default delay time is 15ms (0x03). The delay period is measured from the completion of MTP data loading to the point when the NAVDD output voltage begins to fall. Refer to Figure 7 and the register map for details.

16.14.2 NAVDD Soft-Start Time Setting

The NAVDD includes an internal soft-start mechanism to reduce the input inrush current. The soft-start time can be adjusted using the 3-bit register 0Eh[2:0], which provides 8 steps from 5ms to 40ms, with each step approximately 5ms. The default soft-start time is 10ms (0x01). The soft-start period begins after the NAVDD delay time has elapsed and ends when the NAVDD output voltage is ready. Refer to Figure 7 and the register map for details.

16.14.3 NAVDD Output Voltage Setting

The NAVDD output voltage is adjusted via the I^2C interface. Users can write to the 01h[5:0] register to set the output voltage. This 6-bit register allows adjustment from −5V to −7.3V in approximately −50mV steps. The default value is −6.7V (0x22). Refer to the register map for details on adjusting the output voltage.

16.14.4 NAVDD Inductor Selection

The first step in the design procedure is to verify whether the maximum possible output current of the buck-boost converter meets the application requirements. To simplify the calculation, estimate the converter efficiency using provided efficiency curves or a worst-case assumption, such as 75%. Perform the calculation at the minimum expected input voltage, where the peak switch current is the highest. The inductor and internal switch must be rated to handle this current.

- Converter duty cycle:

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + (V_{IN} \times \eta)}$$

- Maximum output current:

$$I_{OUT} = \left(I_{PEAK} - \frac{V_{IN} \times D}{2 \times f_{OSC} \times L} \right) \times (1\text{-}D)$$

- Inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{1 - D} + \frac{V_{IN} \times D}{2 \times f_{OSC} \times L}$$

To determine the appropriate inductance, identify the transition point where the converter toggles from CCM to DCM. This occurs when the inductor current ripple reaches zero, and the power switch (SW) is immediately reactivated, causing the current to ramp up again. Figure 17 illustrates the input current activity of the buck-boost converter.

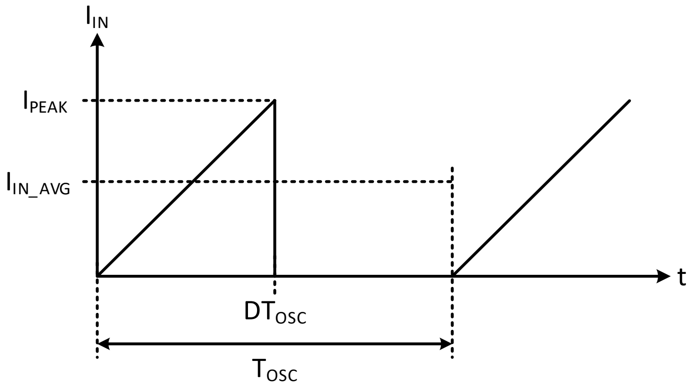


Figure 17. Buck-Boost Input Signature in BCM

The required inductance can be calculated using the following equation:

$$L_{critical} = \frac{|V_{OUT}| \times \eta}{2 \times f_{OSC} \times I_{OUT}} + \left(\frac{V_{IN}}{V_{IN} + |V_{OUT}|} \right)^2$$

16.14.5 NAVDD Output Capacitor Selection

For optimal output voltage filtering, low-ESR ceramic capacitors are recommended. Three 10μF/X7R/1206 capacitors in parallel, providing an effective capacitance of at least 13μF, are suitable for most applications. Additional capacitors can be added to further reduce output voltage ripple.

16.14.6 NAVDD Current Limit

The RTQ6749 features peak current limiting for overcurrent protection. The IC senses the inductor current during the on-time. The internal P-MOSFET will be turned off if the peak inductor current reaches a minimum of 1.5A.

16.15 Programmable VCOM

The RTQ6749 allows adjustment of the VCOM voltage via the I^2C interface to reduce LCD flicker during production testing and alignment. Two registers are provided for VCOM voltage adjustment: VCOM_C for coarse tuning and VCOM_F for fine tuning. For better stability, it is recommended to connect a 10Ω resistor between the output pin and output capacitor. In general applications, VCOM should not be set to 0V. If this channel is not used, it should be disabled.

16.16 VCOM Power-On Delay Time Setting

The VCOM includes integrated power-on sequence control. The delay time is adjustable via the I^2C interface, using the 4-bit register 0Fh[3:0]. The delay time can be set from 0ms to 75ms in approximately 5ms steps. The default value is 25ms (0x05). The delay period starts from the midpoint of the PAVDD and NAVDD soft-start to when the VCOM output voltage begins to fall. Refer to Figure 7 and the register map for details.

16.17 VCOM_C Voltage Setting

The VCOM_C voltage is adjusted using the 8-bit register 04h[7:0], providing 256 steps. The setting range is from 2V to −3V, with each step approximately 20mV. The default value is −1V (0x64). Refer to the register map for details.

16.18 VCOM_F Voltage Setting

The VCOM_F voltage is programmable via the I^2C interface, using a different slave ID (0x60) from VCOM_C. Adjustment is performed using the “VCOM_F I^2C Write Timing Sequence.” The VCOM_F also provides 256 steps and 8-bit resolution. The default value is equal to the VCOM_C setting (0x7F). Increasing the value from 0x7F raises the VCOM_F voltage above the VCOM_C setting, with each step approximately 10 mV; decreasing from 0x7F lowers the voltage. The setting range is from (VCOM_C + 1.28V) to (VCOM_C – 1.27V). Refer to the register map for details.

16.19 RESET Voltage Detector

The voltage detector monitors the VIN voltage and generates a RESET signal from the RESET pin when VIN falls below the detection level (not latched). Both the detecting level and power-on delay time are programmable via the I^2C interface. The detection level is set by register (0x12 [6:5]), with 4 options: UVLO falling, 2.1V, 2.4V, and 2.7V. The delay time is set by register (0x10[3:0]), ranging from 0ms to 75ms in 5ms steps. The delay period starts when both VIN exceeds the UVLO threshold and EN exceeds the VIH threshold, and ends when the RESET signal goes high.

Additionally, users can select whether the RESET goes low following the power-off delay time or the VGH channel turn-off, configurable via register 12h[7].

16.20 Discharge Function

The PAVDD, NAVDD, VGH, VGL, and VCOM output voltages are integrated with a discharge function. Each output voltage is rapidly discharged from 100% to 30% within 2ms at power-off, preventing residual image on the display. To discharge outputs to GND level, external discharge resistors should be added. The discharge function can be enabled or disabled individually for each channel via register 12h[4:0].

When enabled, the discharge function operates at both power-off and power-on. During power-on, discharge starts from UVLO plus 1ms until the channel's delay time elapses. If disabled, discharge does not occur at power-on or power-off, except during the period from UVLO_R to MTP_LOAD_OK (see Figure 18). If a channel is unused, its discharge function should also be disabled.

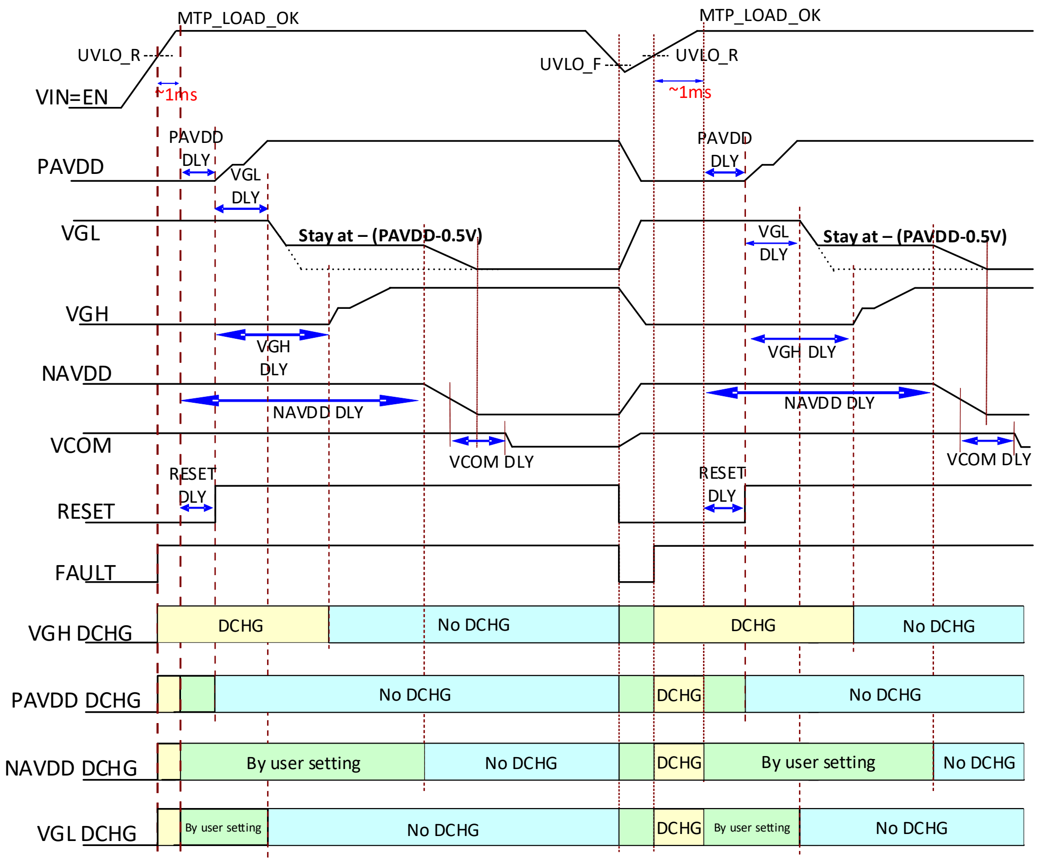


Figure 18. Discharge Function Enable Operation Mechanism

For VGL, discharge function is related to the VGL topology and the power-off sequence. When VGL discharge is enabled, it is recommended to use external mode (see Figure 5), or ensure the VGL power sequence leads NAVDD.

16.21 Slew Rate Control

The RTQ6749 provides options for adjusting the switching node slew rate via the I^{2}C interface. Register 13h[7:0] controls slew rates as follows:

13h[7:6]: PAVDD LX falling slew rate (fast, normal, slow, slowest)

13h[5:4]: NAVDD LXN rising slew rate (same options as PAVDD)

13h[3:2]: VGL CX1 slew rate control

13h[1:0]: VGH LXP falling slew rate control.

16.22 Power-Off Delay Time Setting

The power-off delay time for PAVDD (18h[2:0]), NAVDD (19h[2:0]), VGH (1Ah[2:0]), VGL (1Bh[2:0]), and VCOM (1Ch[2:0]) can be adjusted via the I^2C interface. Each channel has 8 steps within a 3-bit register, with a range from 0ms to 14ms in 2ms steps. The default value for each channel is 0ms. The delay period is from when RESET goes low to the completion of the delay count. Refer to Figure 7 and the register map for details.

16.23 Frequency Spread

The RTQ6749 integrates a frequency spread function for the switching frequency to reduce EMI. There are 3 options: disabled, 3%, and 6%. Users can configure this via register 14h[4:3].

16.24 FAULT Analysis Function

The RTQ6749 provides a fault recording register to help users quickly identify which output channel has experienced an undervoltage protection (UVP) fault. If a UVP event occurs, the fault is recorded in register 1Dh[3:0], which can be read via the I^2C interface. The register indicates the channel with the fault.

An option (1Ch[3]) allows users to clear the fault record when EN goes low or when VIN falls below the VIN1 UVLO_F.

16.25 Control Register (FFH)

The RTQ6749 provides a control register for selecting whether to write/read data to/from MTP or the register. Setting the most significant bit (MSB) of the register FFH high writes data to MTP; writing to a register does not require this. To read from MTP, set the least significant bit (LSB) of register FFH high; to read from a register, set the LSB low. Refer to the "I^2C Write/Read Timing Sequence" for details.

16.26 Auto Refresh Functions

The RTQ6749 includes an auto-recovery function for register code if they are changed abnormally. The Auto Refresh Function can be enabled or disabled via 17h[0], and the refresh interval is adjustable via 17h[2:1]. The FAULT pin behavior can also be configured via 17h[3]. Refer to the register map for details.

Table 3. Protection Behavior of Each Output Channel

Block	Protection	Work Condition	Behavior	Recovery
PAVDD	OVP	PAVDD > PAVDD x 120%	LX stop switching	Vout < OVP - Hys, Hys = 0.5V (typical), LX switch at next clk.
	UVP	PAVDD < PAVDD x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)
	SCP	PAVDD < PAVDD x 30%	LX stop switching, IC shut down and latch	1. VIN re-power up. 2. EN toggle again.
NAVDD	OVP	NAVDD x120%	LXN stop switching	Vout < OVP-Hys, Hys = 0.6V (typical), LXN switch at next clk.
	UVP	NAVDD < NAVDD x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)

Block	Protection	Work Condition	Behavior	Recovery
	SCP	NAVDD < NAVDD x 30%	LXN stop switching, IC shut down and latch	1. VIN re-power up. 2. EN toggle again.
VGH	OVP	VGH > VGH x 120% VGH = 30V > 36V	LXP stop switching	Vout < OVP-Hys, Hys = 0.3V (typical), LXP switch at next clk.
	UVP	VGH < VGH x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)
	SCP	VGH < VGH x 30%	LXP stop switching, IC shut down and latch	1. VIN re-power up. 2. EN toggle again.
VGL	UVP	VGL < VGL x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)
	SCP	VGL > VGL x 30%	CX1/CX2 stop switching, IC shut down and latch	1. VIN re-power up. 2. EN toggle again.
VCOM	OCP	VCOM source/sink current > ±350mA (typical)	Clamp the output current at OCP level	After the abnormal load is removed.

Table 4. FAULT Behavior and Protections

Block	Triggering Protection	FAULT Pin Behavior	Recovery
PAVDD	OVP	High (Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low (Fault pin toggle one time)	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hysteresis, Hysteresis = 20°C (typical)
NAVDD	OVP	High (Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hysteresis, Hysteresis = 20°C (typical)
VGH	OVP	High (Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hysteresis, Hysteresis = 20°C (typical)

Block	Triggering Protection	FAULT Pin Behavior	Recovery
VGL	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low (The short-circuit condition should persist until the IC re-power up at next time)	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hysteresis, Hysteresis = 20°C (typical)
VCOM	OCP	High (Normal state)	--
	OTP	Low	IC Temperature < OTP - Hysteresis, Hysteresis = 20°C (typical)

16.27 I^{2}C Command

16.27.1 PMIC Slave Address

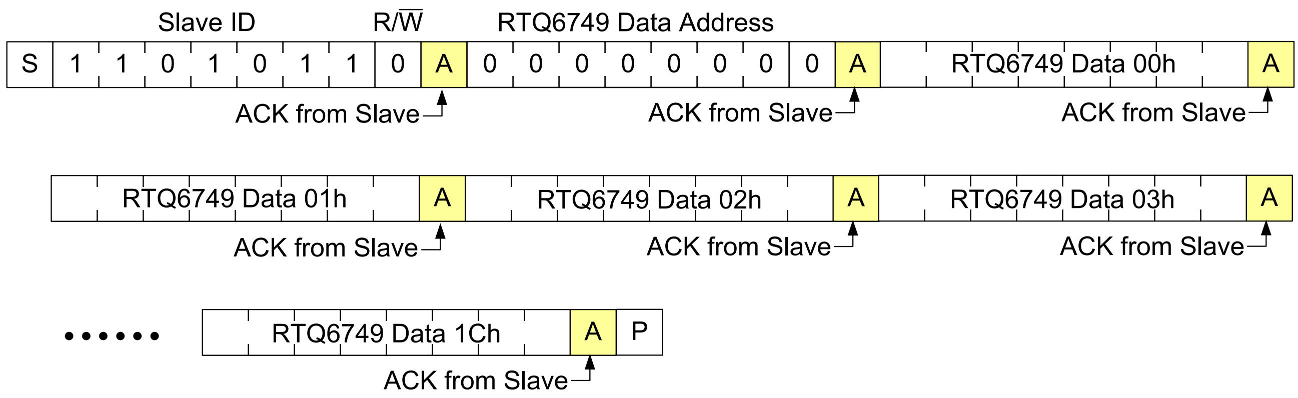
7	6	5	4	3	2	1	0 = R/W	
1	1	0	1	0	1	1	0	D6H
1	1	0	1	0	1	1	1	D7H

16.27.2 VCOM_F Slave Address

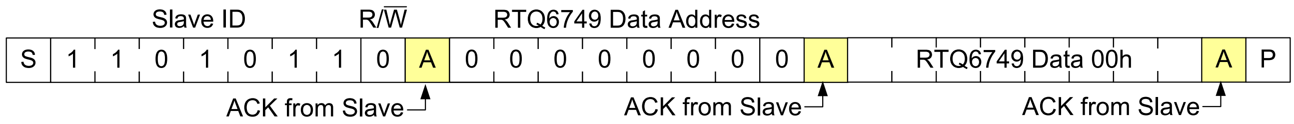
7	6	5	4	3	2	1	0 = R/W	
0	1	1	0	0	0	0	0	60H
0	1	1	0	0	0	0	1	61H

16.27.3 PMIC I^2C Write Timing Sequence (To DAC Register)

Write Multiple Data (00h~1Ch)

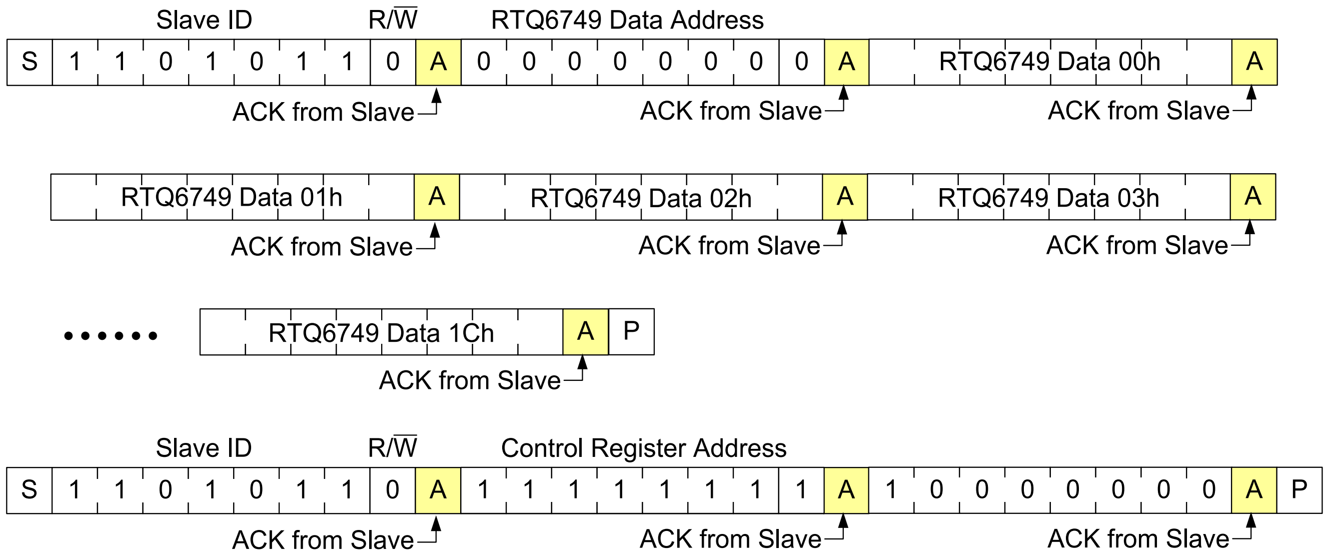


Write Single Data (00h)

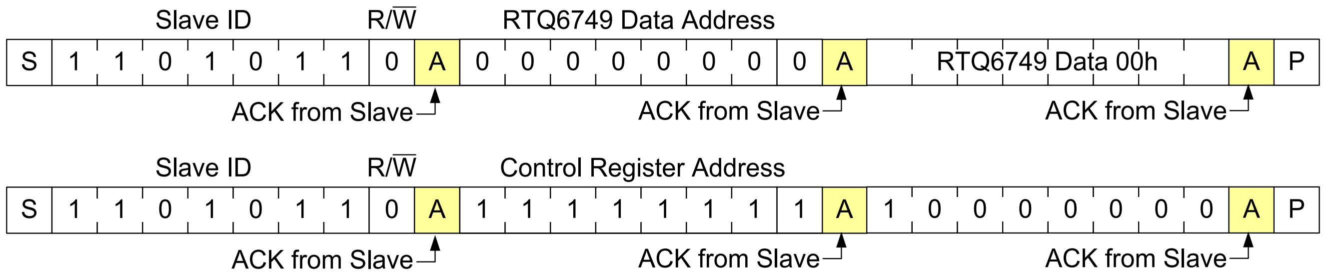


16.27.4 PMIC I^2C Write Timing Sequence (To MTP)

Write Multiple Data (00h~1Ch)

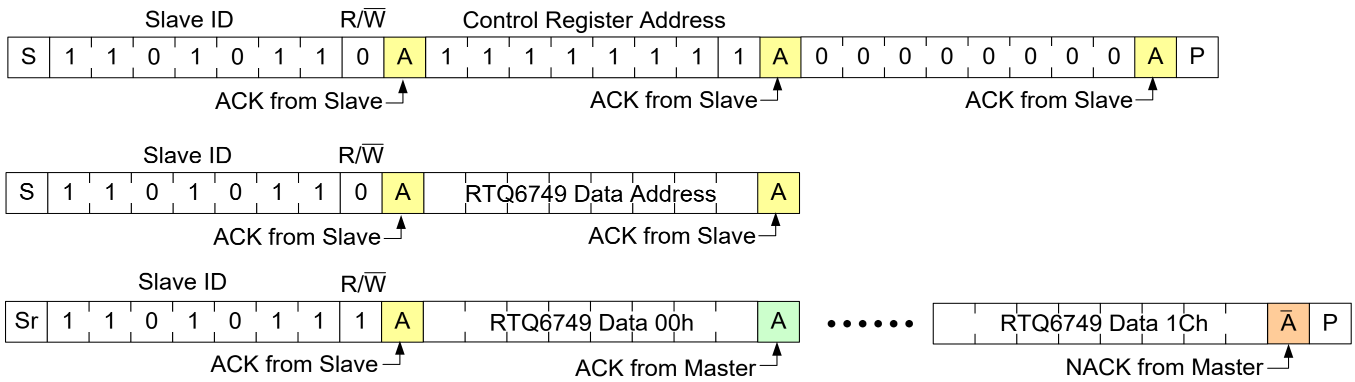


Write Single Data (00h)

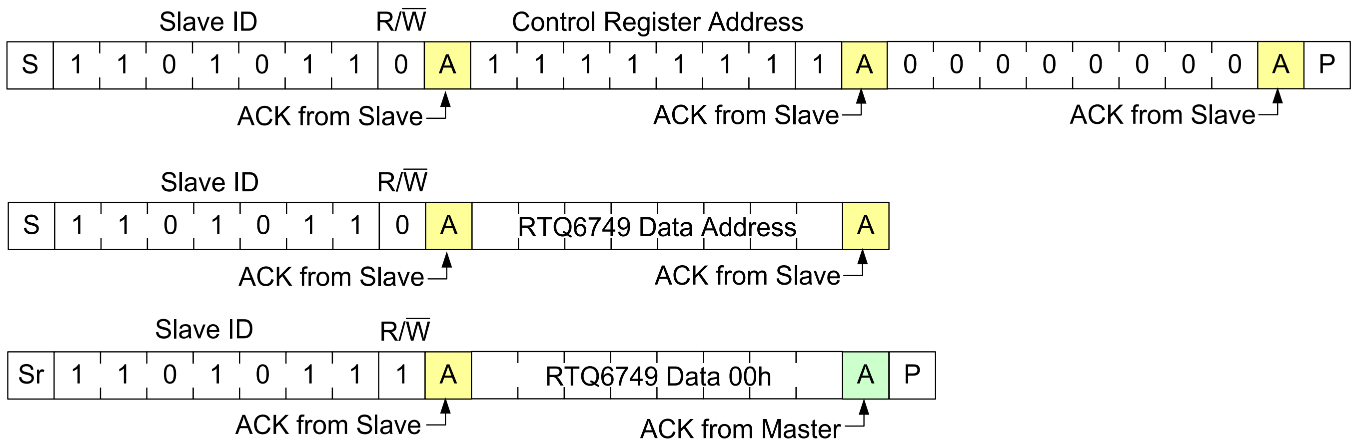


16.27.5 PMIC I²C Read Timing Sequence (From DAC Register)

Read Multiple Data (00h~1Ch)

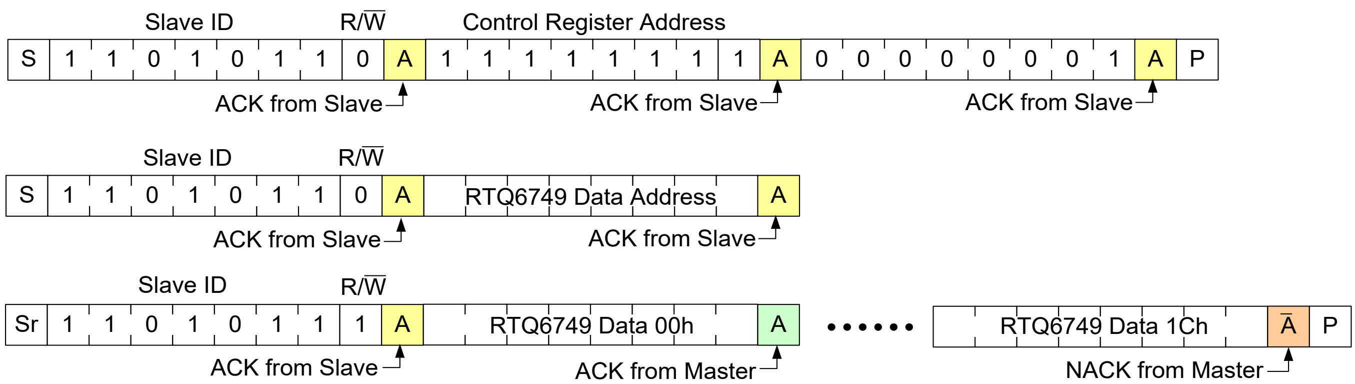


Read Single Data (00h)

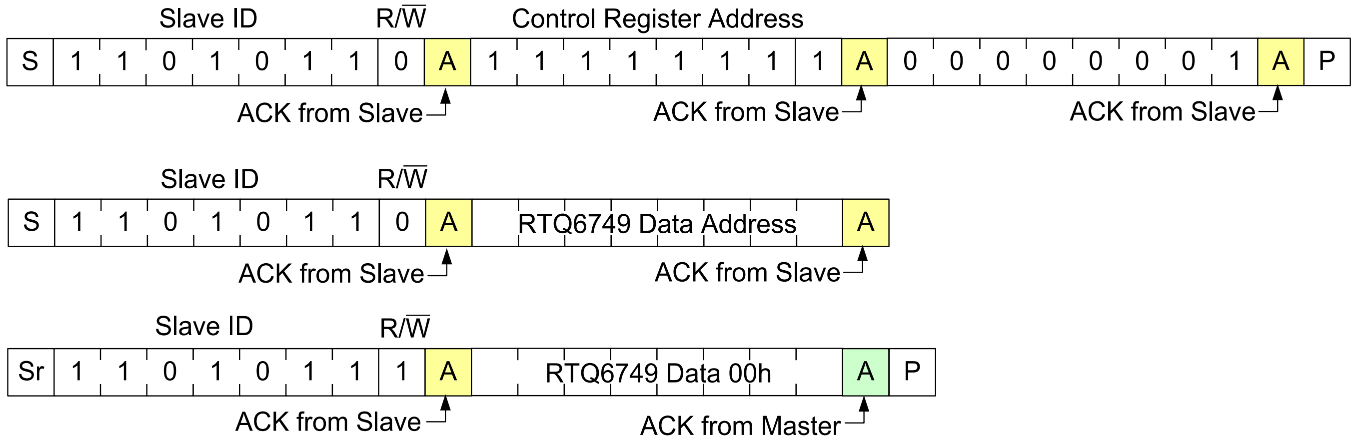


16.27.6 PMIC I²C Read Timing Sequence (From MTP)

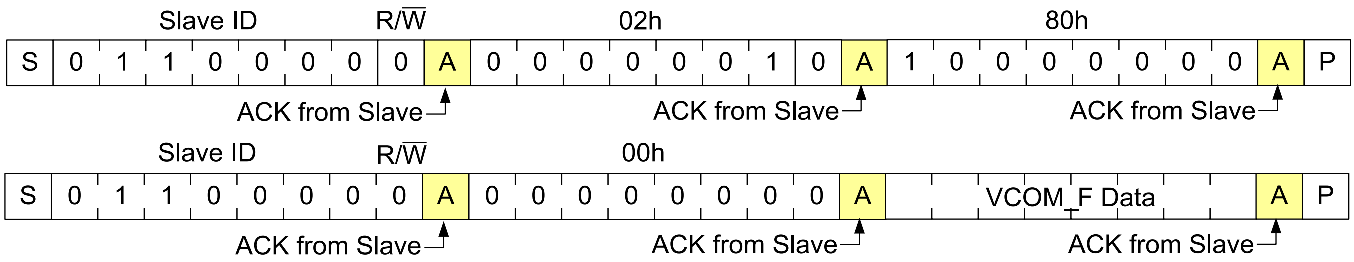
Read Multiple Data (00h~1Ch)



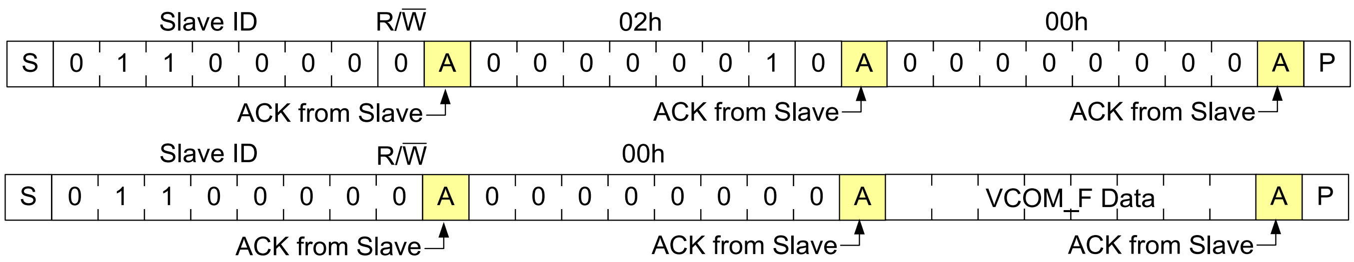
Read Single Data (00h)



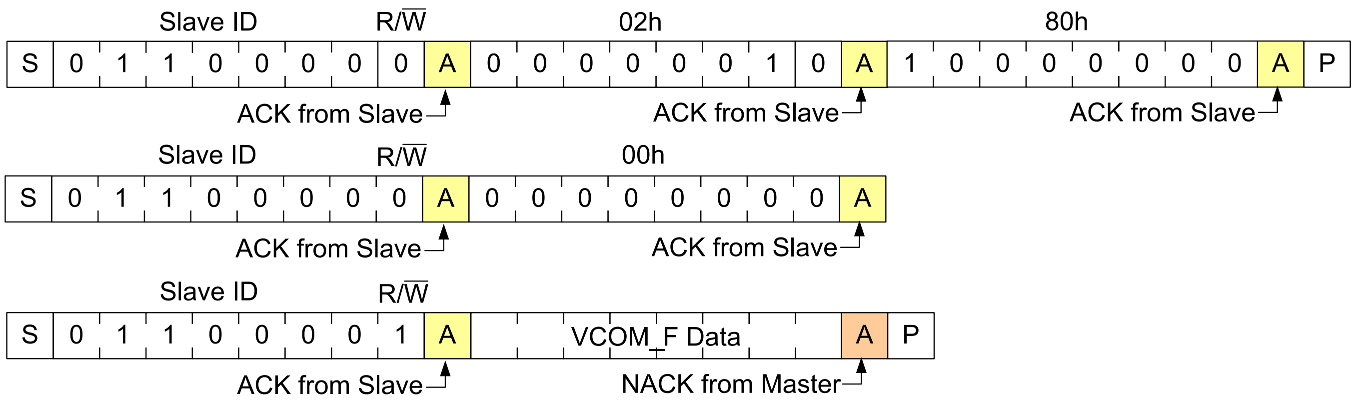
16.27.7 VCOM_F I²C Write Timing Sequence (To DAC Register)



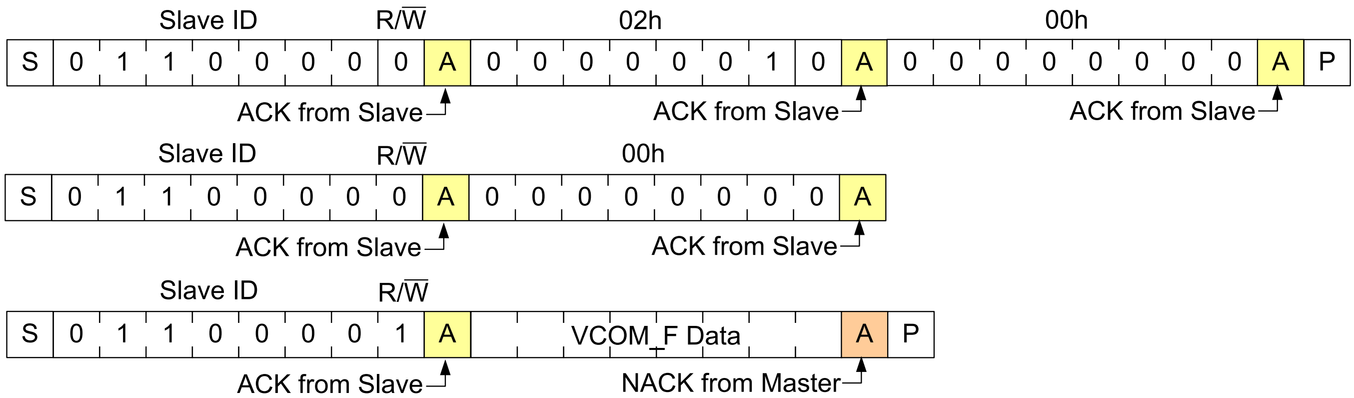
16.27.8 VCOM_F I²C Write Timing Sequence (To MTP & DAC Register)



16.27.9 VCOM_F I²C Read Timing Sequence (From DAC Register)



16.27.10 VCOM_F I²C Read Timing Sequence (From MTP)



16.28 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-32L 5x5 package, the thermal resistance, θ_{JA}, is 29.85°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C – 25°C) / 29.85°C/W) = 4.18W for a WQFN-32L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 19 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

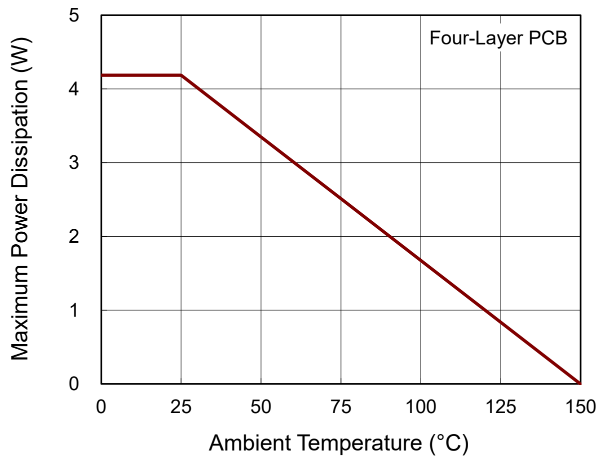


Figure 19. Derating Curve of Maximum Power Dissipation

16.29 Layout Consideration

For optimal performance of the RTQ6749-QT, follow these PCB guidelines:

- Place power components such as inductors (L1, L2, L3), flying capacitor (C14), input capacitors (C1, C2, C3, C6) and output capacitors (C4, C5, C7, C8, C9, C11, C12) as close as possible to each other to minimize the power loop area. The PCB traces between power components must be as short and wide as possible.
- Minimize the size of the LX, LXP, and LXN nodes, and keep these traces wide and short. Keep the LX, LXP, and LXN nodes away from sensitive pins such as COMP, VCOM, NTC, and analog ground to reduce noise coupling.
- The power ground (PGND1, PGND) should connect the grounds of input and output capacitors.
- Place the compensation circuit components (R1, C20) away from the power loops and shielded with a ground trace to prevent any noise coupling. Place these components as close as possible to the COMP pin.
- Connect the exposed pad of the chip to a strong ground plane to enhance thermal dissipation.

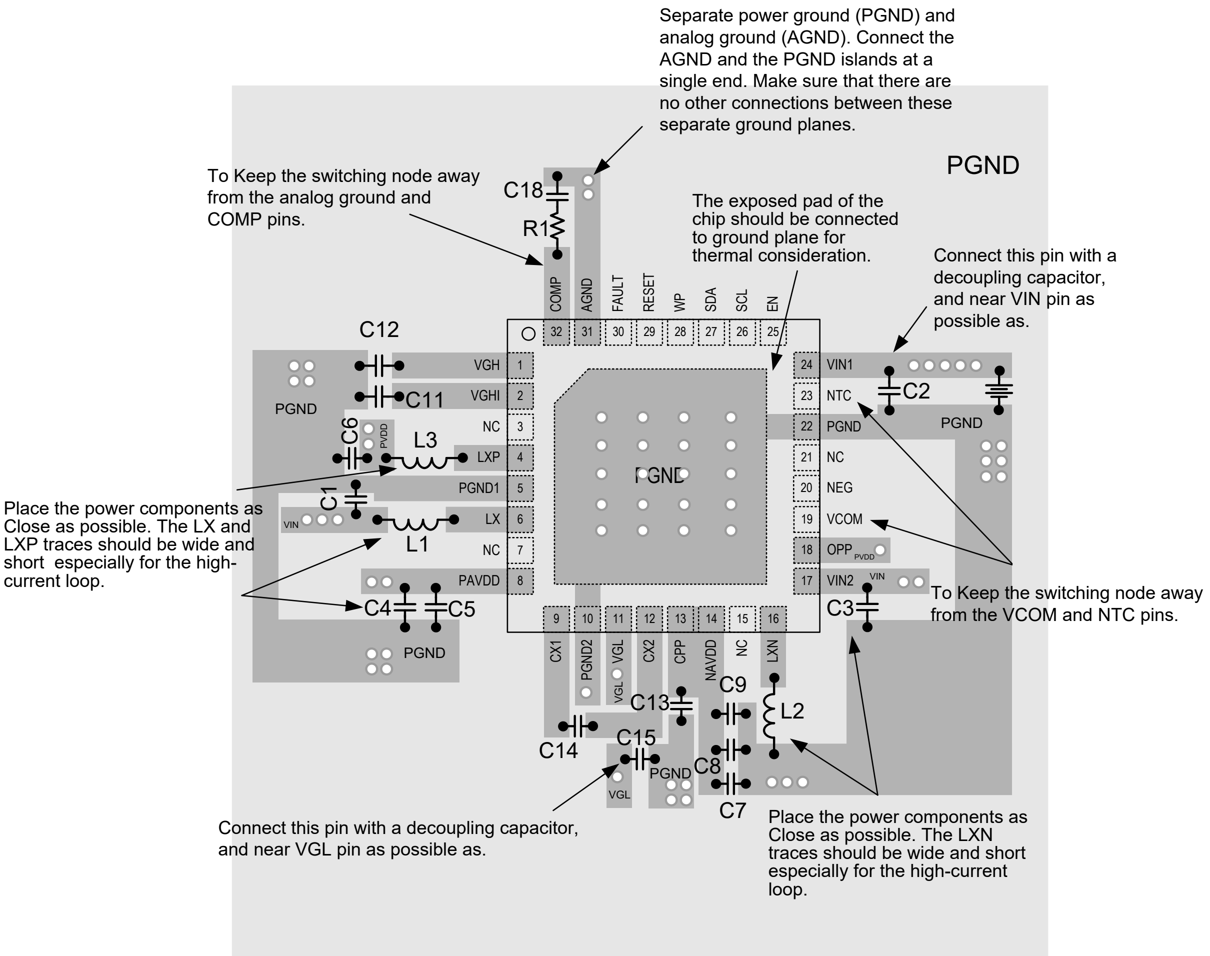


Figure 20. PCB Layout Guide

Note 12. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Functional Register Description

17.1 Register Map

Items		Register Address	Resolution	Range	Default value	Step	Bit
PMIC	PAVDD[5:0]	00h	0.05V	5.0 ~ 7.3V	6.7V	47 Step	6 Bit
	NAVDD[5:0]	01h	0.05V	–5.0 ~ –7.3V	–6.7V	47 Step	6 Bit
	VGH[5:0]	02h	0.5V	7 ~ 30V	10V	47 Step	6 Bit
	VGL[5:0]	03h	0.25V	–6V ~ –18V	–10V	49 Step	6 Bit
	VCOM_C [7:0]	04h	20mV	2V ~ –3V	–1V	251 Step	8 Bit
	VGH Low Temp. [1:0]	05h	2V	2V/4V/6V/8V	2V	4 Step	2 Bit
	SW Freq.[1:0]	06h	--	600k/800k/1M/2.2M	600kHz	4 Step	2 Bit
Power-On Sequence	PAVDD On Delay[3:0]	07h	5ms	0ms ~ 75ms	5ms	16 Step	4 Bit
	PAVDD Soft-Start[2:0]	08h	5ms	5ms ~ 40ms	10ms	8 Step	3 Bit
	VGL On Delay[3:0]	09h	5ms	0ms ~ 75ms	25ms	16 Step	4 Bit
	VGL Soft-Start[2:0]	0Ah	3ms	3ms ~ 24ms	9ms	8 Step	3 Bit
	VGH On Delay[3:0]	0Bh	5ms	0ms ~ 75ms	25ms	16 Step	4 Bit
	VGH Soft-Start[1:0]	0Ch	5ms	5/10/15/20ms	10ms	4 Step	2 Bit
	NAVDD On Delay[3:0]	0Dh	5ms	0ms ~ 75ms	15ms	16 Step	4 Bit
	NAVDD Soft-Start[2:0]	0Eh	5ms	5ms ~ 40ms	10ms	8 Step	3 Bit
	VCOM On Delay[3:0]	0Fh	5ms	0ms ~ 75ms	25ms	16 Step	4 Bit
	RESET On Delay[3:0]	10h	5ms	0ms ~ 75ms	5ms	16 Step	4 Bit
	Power-Off Delay[3:0]	11h	3ms	0ms ~ 45ms	18ms	16 Step	4 Bit
Option1	RESET Sync Option[7]	12h	--	Power-Off Delay/ VGH Sync	Power Off Delay	2 Step	1 Bit
	Vin Detection[6:5]		--	UVLO Falling /2.1V/2.4V/2.7V	UVLO Falling	4 Step	2 Bit
	PAVDD D/C Function[4]		--	On (0)/Off (1)	On	2 Step	1 Bit
	NAVDD D/C Function[3]		--	On (0)/Off (1)	On	2 Step	1 Bit
	VGH D/C Function[2]		--	On (0)/Off (1)	Off	2 Step	1 Bit
	VGL D/C Function[1]		--	On (0)/Off (1)	Off	2 Step	1 Bit
	VCOM D/C Function[0]		--	On (0)/Off (1)	On	2 Step	1 Bit

Items		Register Address	Resolution	Range	Default value	Step	Bit
Option2	PAVDD Slew Rate[7:6]	13h	--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit
	NAVDD Slew Rate[5:4]		--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit
	VGL Slew Rate[3:2]		--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit
	VGH Slew Rate[1:0]		--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit
Option3	VGL Internal/External[5]	14h	--	Internal/External	Internal	2 Step	1 Bit
	Freq. Spread Option (EMI)[4:3]		--	Off/+3%/+6%	Off	3 Step	2 Bit
	OTP On/Off[2]		--	On (0)/Off (1)	On	2 Step	1 Bit
	UVP On/Off[1]		--	On (0)/Off (1)	On	2 Step	1 Bit
	SCP On/Off[0]		--	On (0)/Off (1)	On	2 Step	1 Bit
	VCOM_F [7:0]	X	10mV	VCOM_C-1.27V~VCOM_C+1.28V	VCOM_C	256 step	8 Bit
Channel ON/OFF Option	RESET EN[5]	16h	--	On (1)/Off (0)	On	2 Step	1 Bit
	VCOM EN[4]		--	On (1)/Off (0)	On	2 Step	1 Bit
	NAVDD EN[3]		--	On (1)/Off (0)	On	2 Step	1 Bit
	VGH EN[2]		--	On (1)/Off (0)	On	2 Step	1 Bit
	VGL EN[1]		--	On (1)/Off (0)	On	2 Step	1 Bit
	PAVDD EN[0]		--	On (1)/Off (0)	On	2 Step	1 Bit
Auto Refresh Option	FAULT Behavior[3]	17h	--	Not Pull Low (0)/Pull Low (1)	Not Pull Low	2 Step	1 Bit
	Refreshing Time[2:1]		--	0.25s/0.5s/1s/2s	0.5s	4 Step	2 Bit
	AR EN[0]		--	Off (0)/On (1)	Off	2 Step	1 Bit
Power-Off Sequence	PAVDD Off Delay[2:0]	18h	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	NAVDD Off Delay[2:0]	19h	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	VGH Off Delay[2:0]	1Ah	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	VGL Off Delay[2:0]	1Bh	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	FAULT Analysis Clear Option[3]	1Ch	--	Not Clear (0)/Clear (1)	Not Clear	2 Step	1 Bit
	VCOM Off Delay[2:0]		2ms	0ms ~ 14ms	0ms	7 step	3 Bit
Fault Analysis	PAVDD Fault[3]	1Dh	--	No Fault (0)/ Fault Happen (1)	No Fault	2 Step	1 Bit
	VGL Fault[2]		--	No Fault (0)/ Fault Happen (1)	No Fault	2 Step	1 Bit
	VGH Fault[1]		--	No Fault (0)/ Fault Happen (1)	No Fault	2 Step	1 Bit
	NAVDD Fault[0]		--	No Fault (0)/ Fault Happen (1)	No Fault	2 Step	1 Bit

17.2 Register Table

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
Data Address	00h	01h	02h	03h	04h	05h	06h
Bits	[5:0]	[5:0]	[5:0]	[5:0]	[7:0]	[1:0]	[1:0]
Minimum	5V	–7.3V	7V	–18V	–3V	2V	600kHz
Maximum	7.3V	–5V	30V	–6V	2V	8V	2.2MHz
Default	22h	22h	06h	10h	64h	00h	00h
Resolution	50mV	50mV	0.5V	0.25V	20mV	2V	-
0H	5.00V	–5.00V	7.0V	–6.00V	–3.00V	2.0V	600kHz
1H	5.05V	–5.05V	7.5V	–6.25V	–2.98V	4.0V	800kHz
2H	5.10V	–5.10V	8.0V	–6.50V	–2.96V	6.0V	1MHz
3H	5.15V	–5.15V	8.5V	–6.75V	–2.94V	8.0V	2.2MHz
4H	5.20V	–5.20V	9.0V	–7.00V	–2.92V		
5H	5.25V	–5.25V	9.5V	–7.25V	–2.90V		
6H	5.30V	–5.30V	10.0V	–7.50V	–2.88V		
7H	5.35V	–5.35V	10.5V	–7.75V	–2.86V		
8H	5.40V	–5.40V	11.0V	–8.00V	–2.84V		
9H	5.45V	–5.45V	11.5V	–8.25V	–2.82V		
AH	5.50V	–5.50V	12.0V	–8.50V	–2.80V		
BH	5.55V	–5.55V	12.5V	–8.75V	–2.78V		
CH	5.60V	–5.60V	13.0V	–9.00V	–2.76V		
DH	5.65V	–5.65V	13.5V	–9.25V	–2.74V		
EH	5.70V	–5.70V	14.0V	–9.50V	–2.72V		
FH	5.75V	–5.75V	14.5V	–9.75V	–2.70V		
10H	5.80V	–5.80V	15.0V	–10.00V	–2.68V		
11H	5.85V	–5.85V	15.5V	–10.25V	–2.66V		
12H	5.90V	–5.90V	16.0V	–10.50V	–2.64V		
13H	5.95V	–5.95V	16.5V	–10.75V	–2.62V		
14H	6.00V	–6.00V	17.0V	–11.00V	–2.60V		
15H	6.05V	–6.05V	17.5V	–11.25V	–2.58V		
16H	6.10V	–6.10V	18.0V	–11.50V	–2.56V		
17H	6.15V	–6.15V	18.5V	–11.75V	–2.54V		
18H	6.20V	–6.20V	19.0V	–12.00V	–2.52V		
19H	6.25V	–6.25V	19.5V	–12.25V	–2.50V		
1AH	6.30V	–6.30V	20.0V	–12.50V	–2.48V		
1BH	6.35V	–6.35V	20.5V	–12.75V	–2.46V		
1CH	6.40V	–6.40V	21.0V	–13.00V	–2.44V		
1DH	6.45V	–6.45V	21.5V	–13.25V	–2.42V		
1EH	6.50V	–6.50V	22.0V	–13.50V	–2.40V		
1FH	6.55V	–6.55V	22.5V	–13.75V	–2.38V		
20H	6.60V	–6.60V	23.0V	–14.00V	–2.36V		
21H	6.65V	–6.65V	23.5V	–14.25V	–2.34V		
22H	6.70V	–6.70V	24.0V	–14.50V	–2.32V		
23H	6.75V	–6.75V	24.5V	–14.75V	–2.30V		
24H	6.80V	–6.80V	25.0V	–15.00V	–2.28V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
25H	6.85V	–6.85V	25.5V	–15.25V	–2.26V		
26H	6.90V	–6.90V	26.0V	–15.50V	–2.24V		
27H	6.95V	–6.95V	26.5V	–15.75V	–2.22V		
28H	7.00V	–7.00V	27.0V	–16.00V	–2.20V		
29H	7.05V	–7.05V	27.5V	–16.25V	–2.18V		
2AH	7.10V	–7.10V	28.0V	–16.50V	–2.16V		
2BH	7.15V	–7.15V	28.5V	–16.75V	–2.14V		
2CH	7.20V	–7.20V	29.0V	–17.00V	–2.12V		
2DH	7.25V	–7.25V	29.5V	–17.25V	–2.10V		
2EH	7.30V	–7.30V	30.0V	–17.50V	–2.08V		
2FH				–17.75V	–2.06V		
30H				–18.00V	–2.04V		
31H					–2.02V		
32H					–2.00V		
33H					–1.98V		
34H					–1.96V		
35H					–1.94V		
36H					–1.92V		
37H					–1.90V		
38H					–1.88V		
39H					–1.86V		
3AH					–1.84V		
3BH					–1.82V		
3CH					–1.80V		
3DH					–1.78V		
3EH					–1.76V		
3FH					–1.74V		
40H					–1.72V		
41H					–1.70V		
42H					–1.68V		
43H					–1.66V		
44H					–1.64V		
45H					–1.62V		
46H					–1.60V		
47H					–1.58V		
48H					–1.56V		
49H					–1.54V		
4AH					–1.52V		
4BH					–1.50V		
4CH					–1.48V		
4DH					–1.46V		
4EH					–1.44V		
4FH					–1.42V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
50H					–1.40V		
51H					–1.38V		
52H					–1.36V		
53H					–1.34V		
54H					–1.32V		
55H					–1.30V		
56H					–1.28V		
57H					–1.26V		
58H					–1.24V		
59H					–1.22V		
5AH					–1.20V		
5BH					–1.18V		
5CH					–1.16V		
5DH					–1.14V		
5EH					–1.12V		
5FH					–1.10V		
60H					–1.08V		
61H					–1.06V		
62H					–1.04V		
63H					–1.02V		
64H					–1.00V		
65H					–0.98V		
66H					–0.96V		
67H					–0.94V		
68H					–0.92V		
69H					–0.90V		
6AH					–0.88V		
6BH					–0.86V		
6CH					–0.84V		
6DH					–0.82V		
6EH					–0.80V		
6FH					–0.78V		
70H					–0.76V		
71H					–0.74V		
72H					–0.72V		
73H					–0.70V		
74H					–0.68V		
75H					–0.66V		
76H					–0.64V		
77H					–0.62V		
78H					–0.60V		
79H					–0.58V		
7AH					–0.56V		
7BH					–0.54V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
7CH					−0.52V		
7DH					−0.50V		
7EH					−0.48V		
7FH					−0.46V		
80H					−0.44V		
81H					−0.42V		
82H					−0.40V		
83H					−0.38V		
84H					−0.36V		
85H					−0.34V		
86H					−0.32V		
87H					−0.30V		
88H					−0.28V		
89H					−0.26V		
8AH					−0.24V		
8BH					−0.22V		
8CH					−0.20V		
8DH					−0.18V		
8EH					−0.16V		
8FH					−0.14V		
90H					−0.12V		
91H					−0.10V		
92H					−0.08V		
93H					−0.06V		
94H					−0.04V		
95H					−0.02V		
96H					0.00V		
97H					0.02V		
98H					0.04V		
99H					0.06V		
9AH					0.08V		
9BH					0.10V		
9CH					0.12V		
9DH					0.14V		
9EH					0.16V		
9FH					0.18V		
A0H					0.20V		
A1H					0.22V		
A2H					0.24V		
A3H					0.26V		
A4H					0.28V		
A5H					0.30V		
A6H					0.32V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
A7H					0.34V		
A8H					0.36V		
A9H					0.38V		
AAH					0.40V		
ABH					0.42V		
ACH					0.44V		
ADH					0.46V		
AEH					0.48V		
AFH					0.50V		
B0H					0.52V		
B1H					0.54V		
B2H					0.56V		
B3H					0.58V		
B4H					0.60V		
B5H					0.62V		
B6H					0.64V		
B7H					0.66V		
B8H					0.68V		
B9H					0.70V		
BAH					0.72V		
BBH					0.74V		
BCH					0.76V		
BDH					0.78V		
BEH					0.80V		
BFH					0.82V		
C0H					0.84V		
C1H					0.86V		
C2H					0.88V		
C3H					0.90V		
C4H					0.92V		
C5H					0.94V		
C6H					0.96V		
C7H					0.98V		
C8H					1.00V		
C9H					1.02V		
CAH					1.04V		
CBH					1.06V		
CCH					1.08V		
CDH					1.10V		
CEH					1.12V		
CFH					1.14V		
D0H					1.16V		
D1H					1.18V		
D2H					1.20V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
D3H					1.22V		
D4H					1.24V		
D5H					1.26V		
D6H					1.28V		
D7H					1.30V		
D8H					1.32V		
D9H					1.34V		
DAH					1.36V		
DBH					1.38V		
DCH					1.40V		
DDH					1.42V		
DEH					1.44V		
DFH					1.46V		
E0H					1.48V		
E1H					1.50V		
E2H					1.52V		
E3H					1.54V		
E4H					1.56V		
E5H					1.58V		
E6H					1.60V		
E7H					1.62V		
E8H					1.64V		
E9H					1.66V		
EAH					1.68V		
EBH					1.70V		
ECH					1.72V		
EDH					1.74V		
EEH					1.76V		
EFH					1.78V		
F0H					1.80V		
F1H					1.82V		
F2H					1.84V		
F3H					1.86V		
F4H					1.88V		
F5H					1.90V		
F6H					1.92V		
F7H					1.94V		
F8H					1.96V		
F9H					1.98V		
FAH					2.00V		

	Power-On Sequence										
	PAVDD On Delay Time	PAVDD Soft-start Time	VGL On Delay Time	VGL Soft-start Time	VGH On Delay Time	VGH Soft-start Time	NAVDD On Delay Time	NAVDD Soft-start Time	VCOM On Delay Time	RESET On Delay Time	Power-Off Delay Time
Data Address	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h
Bits	[3:0]	[2:0]	[3:0]	[2:0]	[3:0]	[1:0]	[3:0]	[2:0]	[3:0]	[3:0]	[3:0]
Minimum	0ms	5ms	0ms	3ms	0ms	5ms	0ms	5ms	0ms	0ms	0ms
Maximum	75ms	40ms	75ms	24ms	75ms	20ms	75ms	40ms	75ms	75ms	45ms
Default	01h	01h	05h	02h	05h	01h	03h	01h	05h	01h	06h
Resolution	5ms	5ms	5ms	3ms	5ms	5ms	5ms	5ms	5ms	5ms	3ms
0H	0ms	5ms	0ms	3ms	0ms	5ms	0ms	5ms	0ms	0ms	0ms
1H	5ms	10ms	5ms	6ms	5ms	10ms	5ms	10ms	5ms	5ms	3ms
2H	10ms	15ms	10ms	9ms	10ms	15ms	10ms	15ms	10ms	10ms	6ms
3H	15ms	20ms	15ms	12ms	15ms	20ms	15ms	20ms	15ms	15ms	9ms
4H	20ms	25ms	20ms	15ms	20ms		20ms	25ms	20ms	20ms	12ms
5H	25ms	30ms	25ms	18ms	25ms		25ms	30ms	25ms	25ms	15ms
6H	30ms	35ms	30ms	21ms	30ms		30ms	35ms	30ms	30ms	18ms
7H	35ms	40ms	35ms	24ms	35ms		35ms	40ms	35ms	35ms	21ms
8H	40ms		40ms		40ms		40ms		40ms	40ms	24ms
9H	45ms		45ms		45ms		45ms		45ms	45ms	27ms
AH	50ms		50ms		50ms		50ms		50ms	50ms	30ms
BH	55ms		55ms		55ms		55ms		55ms	55ms	33ms
CH	60ms		60ms		60ms		60ms		60ms	60ms	36ms
DH	65ms		65ms		65ms		65ms		65ms	65ms	39ms
EH	70ms		70ms		70ms		70ms		70ms	70ms	42ms
FH	75ms		75ms		75ms		75ms		75ms	75ms	45ms

	Option 1						
	RESET Sync Option	VIN Detection	PAVDD Discharge Function	NAVDD Discharge Function	VGH Discharge Function	VGL Discharge Function	VCOM Discharge Function
Data Address	12h						
Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Minimum	-	-	-	-	-	-	-
Maximum	-	-	-	-	-	-	-
Default	00h	00h	00h	00h	01h	01h	00h
Resolution	-	-	-	-	-	-	-
0H	Power-Off Delay	UVLO Falling	On	On	On	On	On
1H	VGH Sync	2.1V	Off	Off	Off	Off	Off
2H		2.4V					
3H		2.7V					

	Option 2				Option 3				
	PAVDD Slew Rate	**NAVDD Slew Rate**	**VGL Slew Rate**	**VGH Slew Rate**	**VGL Internal/External Option**	**Freq. Spread Option (EMI)**	**OTP**	**UVP**	**SCP**
Data Address	13h				14h				
Bits	[7:6]	[5:4]	[3:2]	[1:0]	[5]	[4:3]	[2]	[1]	[0]
Minimum	Slowest	Slowest	Slowest	Slowest	-	Off	-	-	-
Maximum	Fast	Fast	Fast	Fast	-	6%	-	-	-
Default	01h	01h	01h	01h	00h	00h	00h	00h	00h
Resolution	-	-	-	-	-	3%	-	-	-
0H	Fast	Fast	Fast	Fast	Internal	Off	On	On	On
1H	Normal	Normal	Normal	Normal	External	3%	Off	Off	Off
2H	Slow	Slow	Slow	Slow		6%			
3H	Slowest	Slowest	Slowest	Slowest					

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	**RESET EN**	**VCOM EN**	**NAVDD EN**	**VGH EN**	**VGL EN**	**PAVDD EN**	**FAULT Behavior**	**Refreshing Time**	**AR EN**
Data Address	X	16h						17h		
Bits	[7:0]	[5]	[4]	[3]	[2]	[1]	[0]	[3]	[2:1]	[0]
Minimum	VCOM_C-1.27V	-	-	-	-	-	-	-	-	-
Maximum	VCOM_C+1.28V	-	-	-	-	-	-	-	-	-
Default	7Fh	01h	01h	01h	01h	01h	01h	00h	01h	00h
Resolution	10mV	-	-	-	-	-	-	-	-	-
0H	VCOM_C-1.27V	Off	Off	Off	Off	Off	Off	FAULT not pull low	0.25s	Off
1H	VCOM_C-1.26V	On	On	On	On	On	On	FAULT pull low	0.50s	On
2H	VCOM_C-1.25V								1.00s	
3H	VCOM_C-1.24V								2.00s	
4H	VCOM_C-1.23V									
5H	VCOM_C-1.22V									
6H	VCOM_C-1.21V									
7H	VCOM_C-1.20V									
8H	VCOM_C-1.19V									
9H	VCOM_C-1.18V									
AH	VCOM_C-1.17V									
BH	VCOM_C-1.16V									
CH	VCOM_C-1.15V									
DH	VCOM_C-1.14V									
EH	VCOM_C-1.13V									

	VCOM_F	Channel ON/OFF Option						Auto Refresh Option		
		RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
FH	VCOM_C-1.12V									
10H	VCOM_C-1.11V									
11H	VCOM_C-1.10V									
12H	VCOM_C-1.09V									
13H	VCOM_C-1.08V									
14H	VCOM_C-1.07V									
15H	VCOM_C-1.06V									
16H	VCOM_C-1.05V									
17H	VCOM_C-1.04V									
18H	VCOM_C-1.03V									
19H	VCOM_C-1.02V									
1AH	VCOM_C-1.01V									
1BH	VCOM_C-1.00V									
1CH	VCOM_C-0.99V									
1DH	VCOM_C-0.98V									
1EH	VCOM_C-0.97V									
1FH	VCOM_C-0.96V									
20H	VCOM_C-0.95V									
21H	VCOM_C-0.94V									
22H	VCOM_C-0.93V									
23H	VCOM_C-0.92V									
24H	VCOM_C-0.91V									
25H	VCOM_C-0.90V									
26H	VCOM_C-0.89V									
27H	VCOM_C-0.88V									
28H	VCOM_C-0.87V									
29H	VCOM_C-0.86V									
2AH	VCOM_C-0.85V									
2BH	VCOM_C-0.84V									
2CH	VCOM_C-0.83V									
2DH	VCOM_C-0.82V									
2EH	VCOM_C-0.81V									
2FH	VCOM_C-0.80V									
30H	VCOM_C-0.79V									
31H	VCOM_C-0.78V									
32H	VCOM_C-0.77V									
33H	VCOM_C-0.76V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
34H	VCOM_C-0.75V									
35H	VCOM_C-0.74V									
36H	VCOM_C-0.73V									
37H	VCOM_C-0.72V									
38H	VCOM_C-0.71V									
39H	VCOM_C-0.70V									
3AH	VCOM_C-0.69V									
3BH	VCOM_C-0.68V									
3CH	VCOM_C-0.67V									
3DH	VCOM_C-0.66V									
3EH	VCOM_C-0.65V									
3FH	VCOM_C-0.64V									
40H	VCOM_C-0.63V									
41H	VCOM_C-0.62V									
42H	VCOM_C-0.61V									
43H	VCOM_C-0.60V									
44H	VCOM_C-0.59V									
45H	VCOM_C-0.58V									
46H	VCOM_C-0.57V									
47H	VCOM_C-0.56V									
48H	VCOM_C-0.55V									
49H	VCOM_C-0.54V									
4AH	VCOM_C-0.53V									
4BH	VCOM_C-0.52V									
4CH	VCOM_C-0.51V									
4DH	VCOM_C-0.50V									
4EH	VCOM_C-0.49V									
4FH	VCOM_C-0.48V									
50H	VCOM_C-0.47V									
51H	VCOM_C-0.46V									
52H	VCOM_C-0.45V									
53H	VCOM_C-0.44V									
54H	VCOM_C-0.43V									
55H	VCOM_C-0.42V									
56H	VCOM_C-0.41V									
57H	VCOM_C-0.40V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
58H	VCOM_C-0.39V									
59H	VCOM_C-0.38V									
5AH	VCOM_C-0.37V									
5BH	VCOM_C-0.36V									
5CH	VCOM_C-0.35V									
5DH	VCOM_C-0.34V									
5EH	VCOM_C-0.33V									
5FH	VCOM_C-0.32V									
60H	VCOM_C-0.31V									
61H	VCOM_C-0.30V									
62H	VCOM_C-0.29V									
63H	VCOM_C-0.28V									
64H	VCOM_C-0.27V									
65H	VCOM_C-0.26V									
66H	VCOM_C-0.25V									
67H	VCOM_C-0.24V									
68H	VCOM_C-0.23V									
69H	VCOM_C-0.22V									
6AH	VCOM_C-0.21V									
6BH	VCOM_C-0.20V									
6CH	VCOM_C-0.19V									
6DH	VCOM_C-0.18V									
6EH	VCOM_C-0.17V									
6FH	VCOM_C-0.16V									
70H	VCOM_C-0.15V									
71H	VCOM_C-0.14V									
72H	VCOM_C-0.13V									
73H	VCOM_C-0.12V									
74H	VCOM_C-0.11V									
75H	VCOM_C-0.10V									
76H	VCOM_C-0.09V									
77H	VCOM_C-0.08V									
78H	VCOM_C-0.07V									
79H	VCOM_C-0.06V									
7AH	VCOM_C-0.05V									
7BH	VCOM_C-0.04V									
7CH	VCOM_C-0.03V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
7DH	VCOM_C-0.02V									
7EH	VCOM_C-0.01V									
7FH	VCOM_C									
80H	VCOM_C+0.01V									
81H	VCOM_C+0.02V									
82H	VCOM_C+0.03V									
83H	VCOM_C+0.04V									
84H	VCOM_C+0.05V									
85H	VCOM_C+0.06V									
86H	VCOM_C+0.07V									
87H	VCOM_C+0.08V									
88H	VCOM_C+0.09V									
89H	VCOM_C+0.10V									
8AH	VCOM_C+0.11V									
8BH	VCOM_C+0.12V									
8CH	VCOM_C+0.13V									
8DH	VCOM_C+0.14V									
8EH	VCOM_C+0.15V									
8FH	VCOM_C+0.16V									
90H	VCOM_C+0.17V									
91H	VCOM_C+0.18V									
92H	VCOM_C+0.19V									
93H	VCOM_C+0.20V									
94H	VCOM_C+0.21V									
95H	VCOM_C+0.22V									
96H	VCOM_C+0.23V									
97H	VCOM_C+0.24V									
98H	VCOM_C+0.25V									
99H	VCOM_C+0.26V									
9AH	VCOM_C+0.27V									
9BH	VCOM_C+0.28V									
9CH	VCOM_C+0.29V									
9DH	VCOM_C+0.30V									
9EH	VCOM_C+0.31V									
9FH	VCOM_C+0.32V									
A0H	VCOM_C+0.33V									

	VCOM_F	Channel ON/OFF Option						Auto Refresh Option		
		RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
A1H	VCOM_C+0.34V									
A2H	VCOM_C+0.35V									
A3H	VCOM_C+0.36V									
A4H	VCOM_C+0.37V									
A5H	VCOM_C+0.38V									
A6H	VCOM_C+0.39V									
A7H	VCOM_C+0.40V									
A8H	VCOM_C+0.41V									
A9H	VCOM_C+0.42V									
AAH	VCOM_C+0.43V									
ABH	VCOM_C+0.44V									
ACH	VCOM_C+0.45V									
ADH	VCOM_C+0.46V									
AEH	VCOM_C+0.47V									
AFH	VCOM_C+0.48V									
B0H	VCOM_C+0.49V									
B1H	VCOM_C+0.50V									
B2H	VCOM_C+0.51V									
B3H	VCOM_C+0.52V									
B4H	VCOM_C+0.53V									
B5H	VCOM_C+0.54V									
B6H	VCOM_C+0.55V									
B7H	VCOM_C+0.56V									
B8H	VCOM_C+0.57V									
B9H	VCOM_C+0.58V									
BAH	VCOM_C+0.59V									
BBH	VCOM_C+0.60V									
BCH	VCOM_C+0.61V									
BDH	VCOM_C+0.62V									
BEH	VCOM_C+0.63V									
BFH	VCOM_C+0.64V									
C0H	VCOM_C+0.65V									
C1H	VCOM_C+0.66V									
C2H	VCOM_C+0.67V									
C3H	VCOM_C+0.68V									
C4H	VCOM_C+0.69V									
C5H	VCOM_C+0.70V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
C6H	VCOM_C+0.71V									
C7H	VCOM_C+0.72V									
C8H	VCOM_C+0.73V									
C9H	VCOM_C+0.74V									
CAH	VCOM_C+0.75V									
CBH	VCOM_C+0.76V									
CCH	VCOM_C+0.77V									
CDH	VCOM_C+0.78V									
CEH	VCOM_C+0.79V									
CFH	VCOM_C+0.80V									
D0H	VCOM_C+0.81V									
D1H	VCOM_C+0.82V									
D2H	VCOM_C+0.83V									
D3H	VCOM_C+0.84V									
D4H	VCOM_C+0.85V									
D5H	VCOM_C+0.86V									
D6H	VCOM_C+0.87V									
D7H	VCOM_C+0.88V									
D8H	VCOM_C+0.89V									
D9H	VCOM_C+0.90V									
DAH	VCOM_C+0.91V									
DBH	VCOM_C+0.92V									
DCH	VCOM_C+0.93V									
DDH	VCOM_C+0.94V									
DEH	VCOM_C+0.95V									
DFH	VCOM_C+0.96V									
E0H	VCOM_C+0.97V									
E1H	VCOM_C+0.98V									
E2H	VCOM_C+0.99V									
E3H	VCOM_C+1.00V									
E4H	VCOM_C+1.01V									
E5H	VCOM_C+1.02V									
E6H	VCOM_C+1.03V									
E7H	VCOM_C+1.04V									
E8H	VCOM_C+1.05V									
E9H	VCOM_C+1.06V									

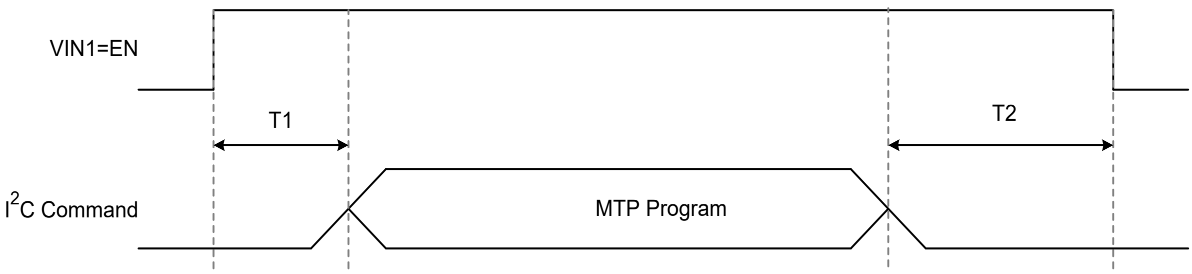
	VCOM_F	Channel ON/OFF Option						Auto Refresh Option		
		RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
EAH	VCOM_C+1.07V									
EBH	VCOM_C+1.08V									
ECH	VCOM_C+1.09V									
EDH	VCOM_C+1.10V									
EEH	VCOM_C+1.11V									
EFH	VCOM_C+1.12V									
F0H	VCOM_C+1.13V									
F1H	VCOM_C+1.14V									
F2H	VCOM_C+1.15V									
F3H	VCOM_C+1.16V									
F4H	VCOM_C+1.17V									
F5H	VCOM_C+1.18V									
F6H	VCOM_C+1.19V									
F7H	VCOM_C+1.20V									
F8H	VCOM_C+1.21V									
F9H	VCOM_C+1.22V									
FAH	VCOM_C+1.23V									
FBH	VCOM_C+1.24V									
FCH	VCOM_C+1.25V									
FDH	VCOM_C+1.26V									
FEH	VCOM_C+1.27V									
FFH	VCOM_C+1.28V									

	Power-Off Sequence					
	PAVDD Off Delay Time	**NAVDD Off Delay Time**	**VGH Off Delay Time**	**VGL Off Delay Time**	**FAULT Analysis Clear Option**	**VCOM Off Delay Time**
Data Address	18h	19h	1Ah	1Bh	1Ch	
Bits	[2:0]	[2:0]	[2:0]	[2:0]	[3]	[2:0]
Minimum	0ms	0ms	0ms	0ms	-	0ms
Maximum	14ms	14ms	14ms	14ms	-	14ms
Default	00h	00h	00h	00h	00h	00h
Resolution	2ms	2ms	2ms	2ms	-	2ms
0H	0ms	0ms	0ms	0ms	Not Clear	0ms
1H	2ms	2ms	2ms	2ms	Clear	2ms
2H	4ms	4ms	4ms	4ms		4ms
3H	6ms	6ms	6ms	6ms		6ms
4H	8ms	8ms	8ms	8ms		8ms
5H	10ms	10ms	10ms	10ms		10ms
6H	12ms	12ms	12ms	12ms		12ms
7H	14ms	14ms	14ms	14ms		14ms

	FAULT Analysis (DAC)			
	PAVDD FAULT	**VGL FAULT**	**VGH FAULT**	**NAVDD FAULT**
Data Address	1Dh			
Bits	[3]	[2]	[1]	[0]
Minimum	-	-	-	-
Maximum	-	-	-	-
Default	00h	00h	00h	00h
Resolution	-	-	-	-
0H	No Fault	No Fault	No Fault	No Fault
1H	Happen	Happen	Happen	Happen

17.3 MTP Program Sequence for Single Chip

MTP program timing sequence



Write Timing:

T1 = 50ms, T2 = 500ms

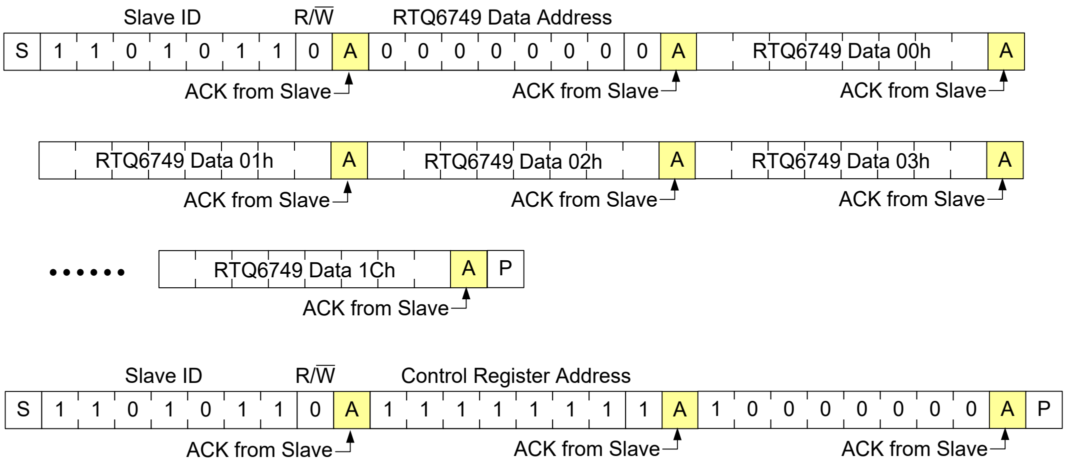
Read Timing:

T1 = 50ms, T2 = 10ms

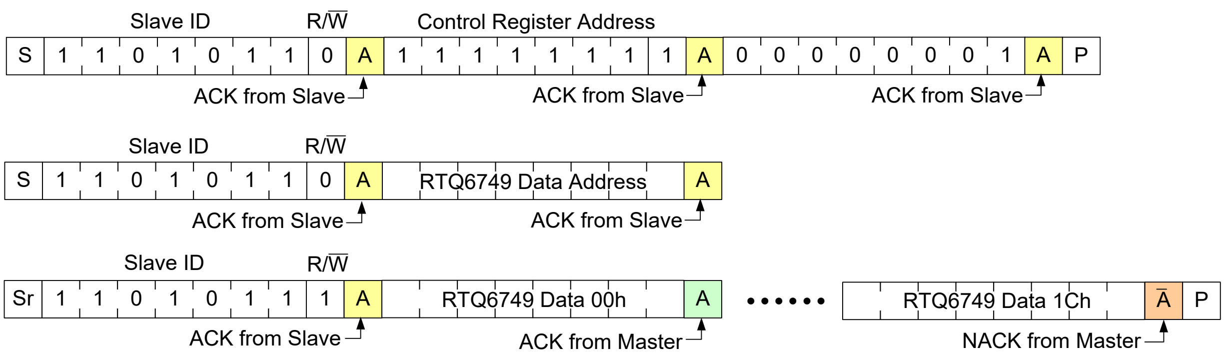
f_{SCL} = 400kHz

17.4 I²C Protocol for MTP Program

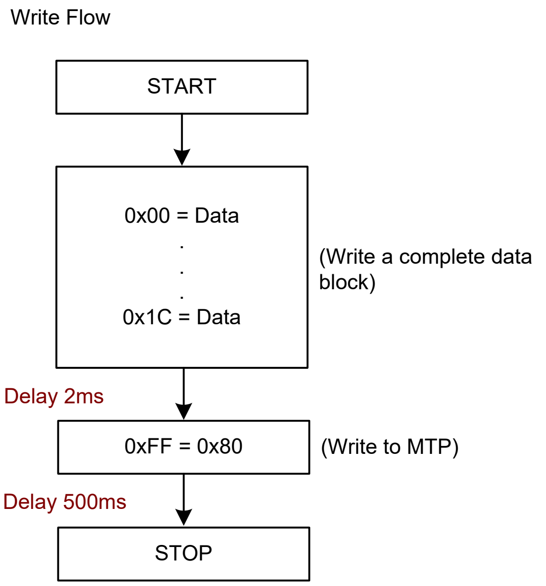
17.4.1 I²C Write Timing Sequence

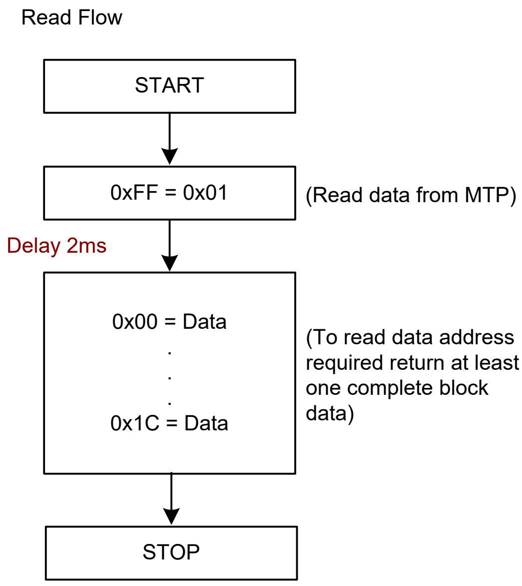


17.4.2 I²C Read Timing Sequence

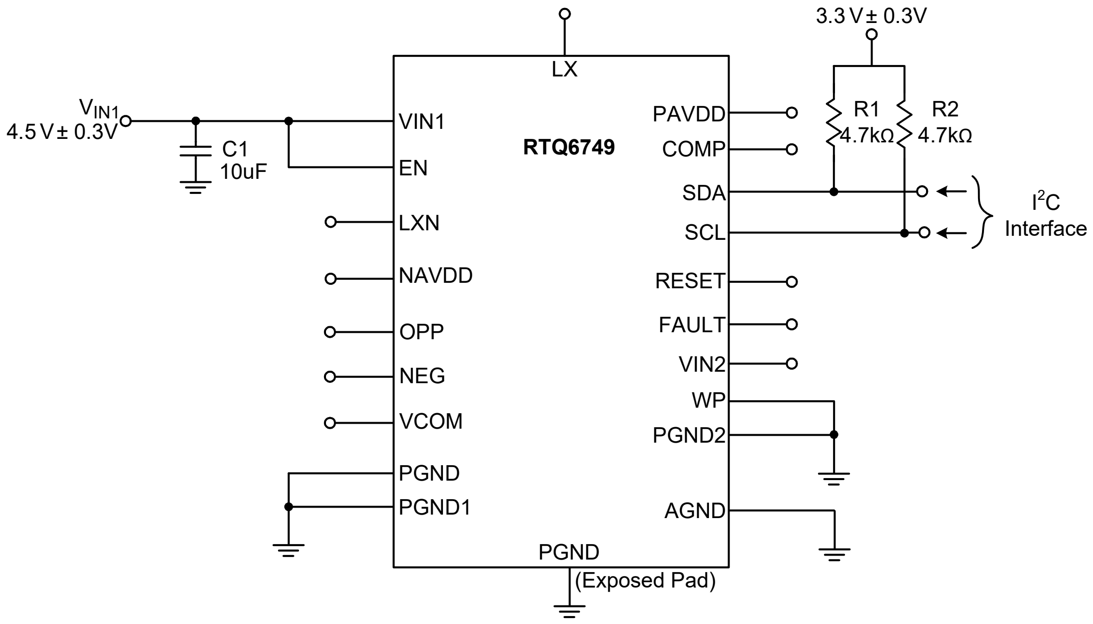


17.5 I²C Read/Write Flow Chat



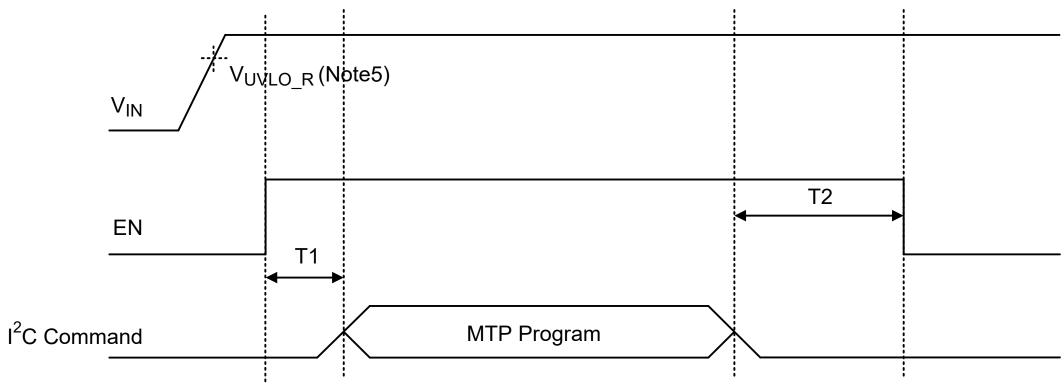


17.6 MTP Program Application Circuit for Single Chip



17.7 MTP Program Sequence on Board

17.7.1 MTP Program Timing Sequence



17.7.2 I²C Writing Conditions

(Note 13)

1. VIN = 3.3V ± 0.3V
2. EN = H
3. WP = L
4. All of output power are ready (Note 14)

17.7.3 Write Timing

VCOM_F: T1 = 60ms (Default code), T2 = 15ms (a 15ms wait time is required regardless of the number of rewrite bits.) (Note 15)

00h~1Ch: T1 = 60ms (Default code), T2 > 150ms (a 150ms wait time is required regardless of the number of rewrite bits.) (Note 15)

17.7.4 Read Timing

T1 = 60ms, T2 = 10ms

17.7.5 MTP Program Function

(Note 16)

Program time

1 page = 4 bytes

MTP page program = 1 * ERASE (4 bytes) + 2 * PROGRAM (2 bytes) = 5ms + 2 * 5ms = 15ms

VCOM_F = 1 page: 1 * 15ms = 15ms

0x00~0x1C = 10 pages: 10 * 15ms = 150ms (Note 18)

Note 13. At startup, the RTQ6749 reads default data from its internal memory (MTP) and begins operation. The customer can change the data in the internal memory via external I^2C communication; however, I^2C communication is not available until both VIN exceeds the UVLO_R threshold and EN is set high (EN = H).
Once the following conditions are met— VIN exceeds UVLO_R, EN = H, all output power rails are ready, and the T1 wait time has elapsed—settings such as output voltage and delay time can be changed via I^2C.

Note 14. Once the power-on sequence is changed, the T1 waiting time should be changed to be PAVDD_DLY + PAVDD_SS + VGL_DLY + VGL_SS + VGH_DLY + VGH_SS + NAVDD_DLY + NAVDD_SS + VCOM_DLY + VCOM_SS (5ms).

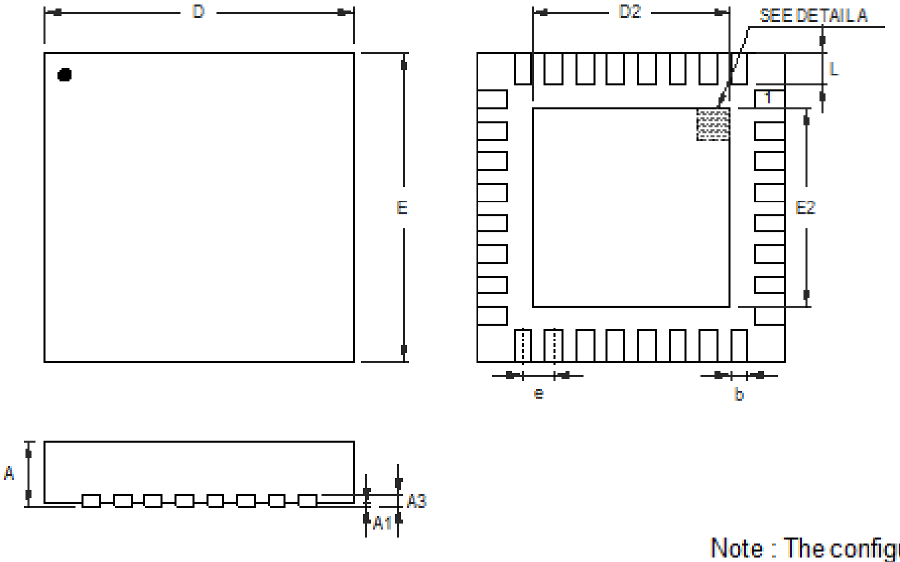
Note 15. T2: Add a margin according to the writing environment.

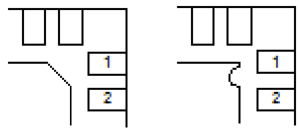
Note 16. If the setting conditions are fixed, an IC with the setting conditions written to the MTP can be provided.

Note 17. UVLO_R = UVLO_F + UVLO_H

Note 18. All data in the DAC register (existing data and rewritten data) is written to the MTP by the control register (FFH) command, so a 150ms wait time is required.

18 Outline Dimension





DETAIL A

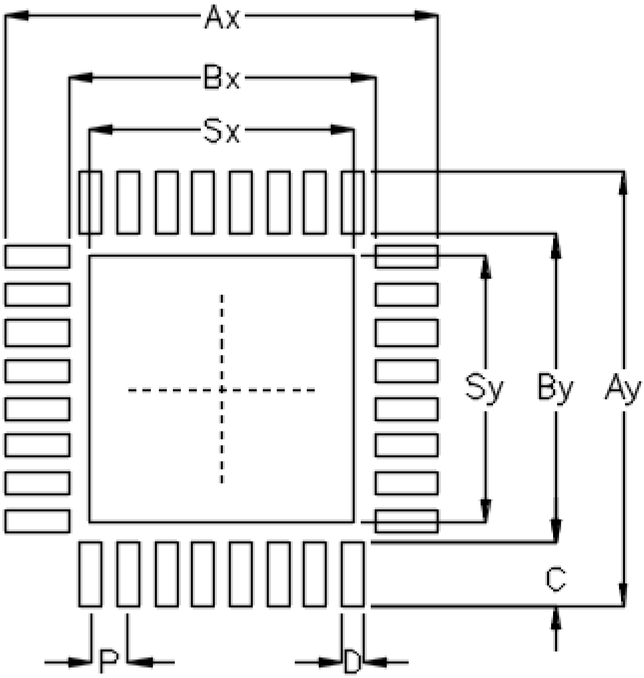
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package

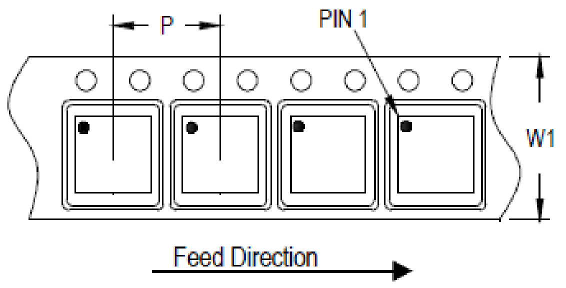
19 Footprint Information

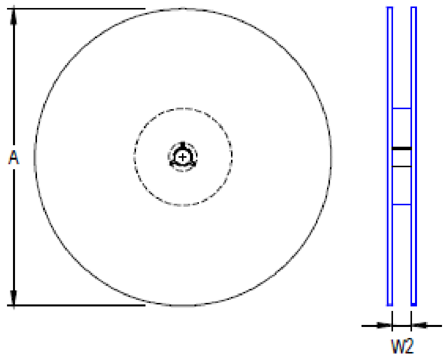


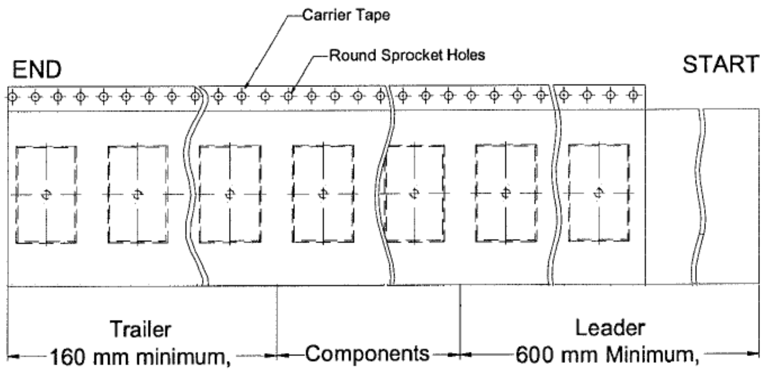
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-32	32	0.50	5.80	5.80	4.10	4.10	0.85	0.30	3.55	3.55	±0.05

20 Packing Information

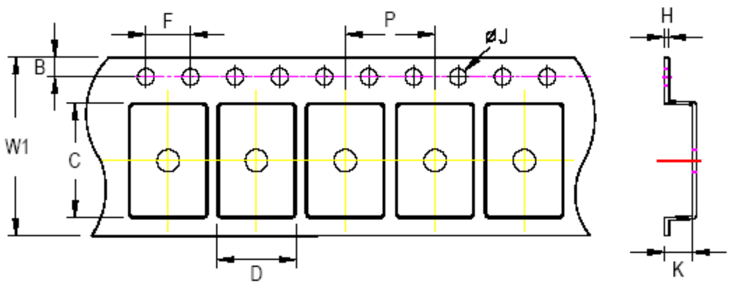
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 5x5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
03	2023/9/19	Modify General Description on P1 Features on P1 Ordering Information on P1 Recommended Operating Conditions on P13 Packing Information on P60, P61, P62
04	2024/10/28	Modify General Description on P1 Ordering Information on P1 Functional Pin Description on P3, 4 Absolute Maximum Ratings on P6 Typical Application Circuit on P11 to 16 Typical Operating Characteristics on P20 Operation on P22 Application Information on P23 to 36, 45, 46, 47, 48 Functional Register Description on P49 Packing Information on P68, 69
05	2026/03/17	Pin Configuration - Updated descriptions of pin name WP Typical Application Circuit - Modified pin name XON to RESET - Updated information on VGL Conditions PAVDD < |VGL| < 2 x PAVDD for VIN 4V~5.5V (5V) in Table 2 Absolute Maximum Ratings - Modified PGND1, PGND2, AGND to PGND descriptions - Modified CX1 to PGND2 descriptions Timing Diagram - Modified VGH_LT Voltage Setting - Modified descriptions Layout Consideration - Modified descriptions Register Map - Modified Power-On Sequence descriptions - Modified Power-Off Sequence descriptions