RICHTEK® **RTQ7892B-QT**

USB Type-C PD and PWM Buck-Boost Converter with Integrated Low-Side MOSFETs, AnyPower and PD Safe Features

1 General Description

The RTQ7892B-QT is a USB Type-C Power Delivery (USBC PD) and PWM buck-boost converter with integrated low-side MOSFETs, offering highly integrated functions and flexibility for USB PD provider applications. The IC features an embedded ARM Cortex-M0 MCU, which handles various functions such as communication protocol, smart control of the PWM converter, firmware-based protections, and customized functions. The IC also features hardware-based protections, such as inductor peak current limit, VBUS overvoltage protection (VBUS OVP), VIN undervoltage protection (VIN UVP), VIN overvoltage protection (VIN OVP), VO undervoltage protection (VO UVP), and VCONN overcurrent protection, so that the protections have faster responses and can still function even when the MCU is not activated. The RTQ7892B-QT provides an excellent USB PD solution for USB-PD provider applications with minimal external components and a simple PCB layout.

The RTQ7892B-QT is available in a WQFN7x7-62 package. The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 125°C.

2 Applications

- Automotive USB Type-C Power Delivery Chargers

3 Features

- **AEC-Q100 Grade 1 Qualified**
- **Protocol Support**
  - **USB PD3.2 SPR, PPS, and AVS (TID 14462)**
  - **UFCS**
- **Operating Ambient Temperature: –40°C to 125°C**
- **Type-C, USB PD and Communication Protocols**
  - **Compliant with USB PD 3.2 Specification, USB Type-C Cable and Connector Specification 2.4**
  - **V_{CONN} Output 100mW**
  - **Support Alternate Mode**
  - **Support Other Proprietary Communication Protocols through Internal MCU, DP, and DM Pins**
- **Integrated PWM Buck-Boost Converter**
  - **Wide Input Voltage Range: 4.5V to 30V**
  - **Wide Output Voltage Range: 3.3V to 21V**
  - **Peak-Current Mode PWM Operation**
  - **Internal Compensation for Constant Voltage (CV) and Constant Current (CC)**
  - **Programmable PWM Switching Frequency (200kHz to 600kHz)**
  - **Pulse-Skipping Mode for Light-Load Efficiency; Selectable Forced CCM Operation**
  - **Integrated Internal 2 Low-Side N-channel MOSFETs**
- **AnyPower for Constant Voltage Output and Constant Current Output**
- **PD Safe**
  - **Adjustable Converter Input Overcurrent Protection (INOC)**
  - **Fast Response VIN OVP/UVP Detection**
  - **Programmable VBUS OVP and VO UVP**
  - **Fast Response OVP for CC1/2 and D+/D- Pins**
  - **Adjustable External OTP/Internal OTP**
  - **CC1/2 Output Current Limit**
  - **CC1/2, D+/D- 25V Tolerant**
- **Cable Voltage Drop Compensation for VBUS**
- **Switching Frequency Synchronization for Better EMI**
- **Adjustable Gate Drive Current for Better EMI**
- **Firmware-Based Functions**
  - **VIN De-Rating and Power Sharing**
- **Master and Slave I^{2}C Interfaces, LED Control, GPIOs**
- **EN Control for Power Saving**
- **Built-In Output Bleeders for Quick VBUS Discharge**
- **Built-In Charge Pump for Driving Cost-Effective N-MOSFETs**
- **Built-In Internal LDO**
- **Online Firmware Update via Slave I^{2}C Interface**

or CC1/2 Interface

- **Available in a WQFN7x7-62 Package**
- **Junction Temperature Range: –40°C to 150°C**
- **Ambient Temperature Range: –40°C to 125°C**

4 Ordering Information

RTQ7892B□-□□□

- **Packing**
  A: Standard
- **Customized Firmware Code AABBX**(1)
  AA: Firmware Application Code
  BB: Hardware Model Code
  X: Firmware Version Code
- **Grade**
  QT: AEC-Q100 Qualified
- **Package Type**(2)
  N: WQFN7x7-62

Note 1.

- Marked with (1) indicates if the firmware code is empty, this field will be removed.
- Marked with (2) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5 Marking Information

RTQ7892
BNQT
YMDAN

RTQ7892BN: Product Code
QT: Automotive Product Grade
YMDAN: Date Code

6 Simplified Application Circuit

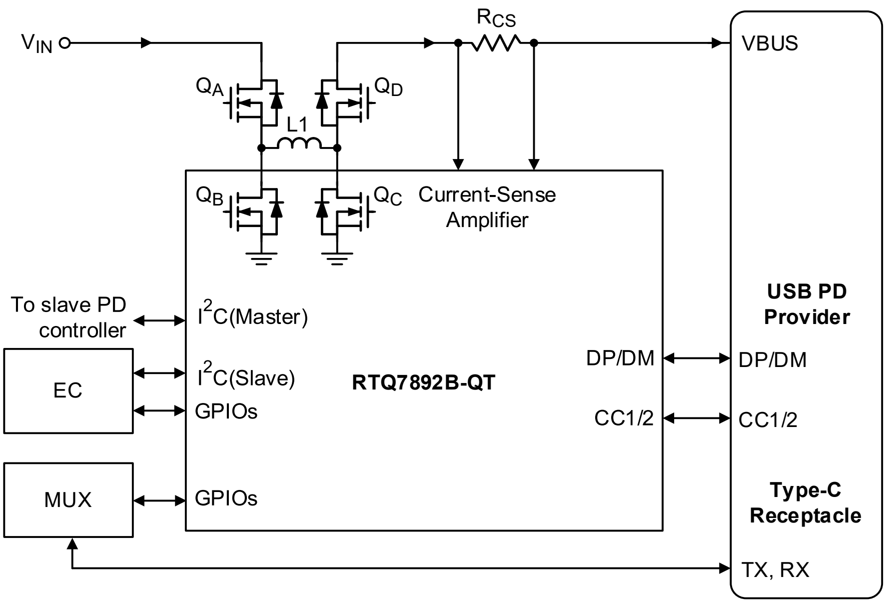
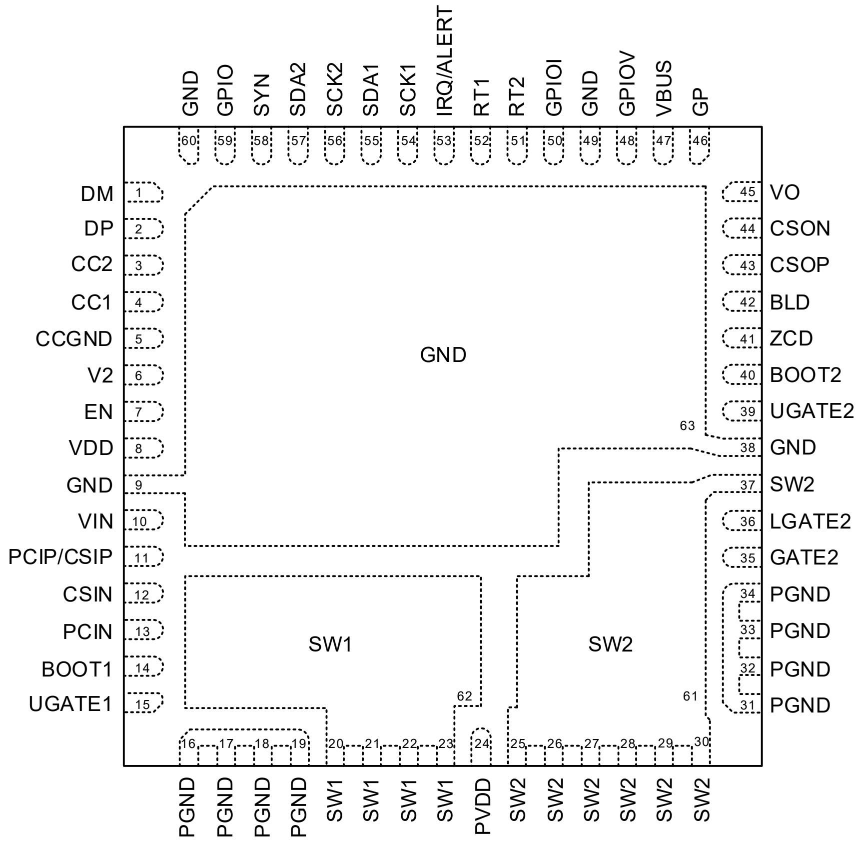


Table of Contents

7 Pin Configuration

(TOP VIEW)



WQFN7x7-62

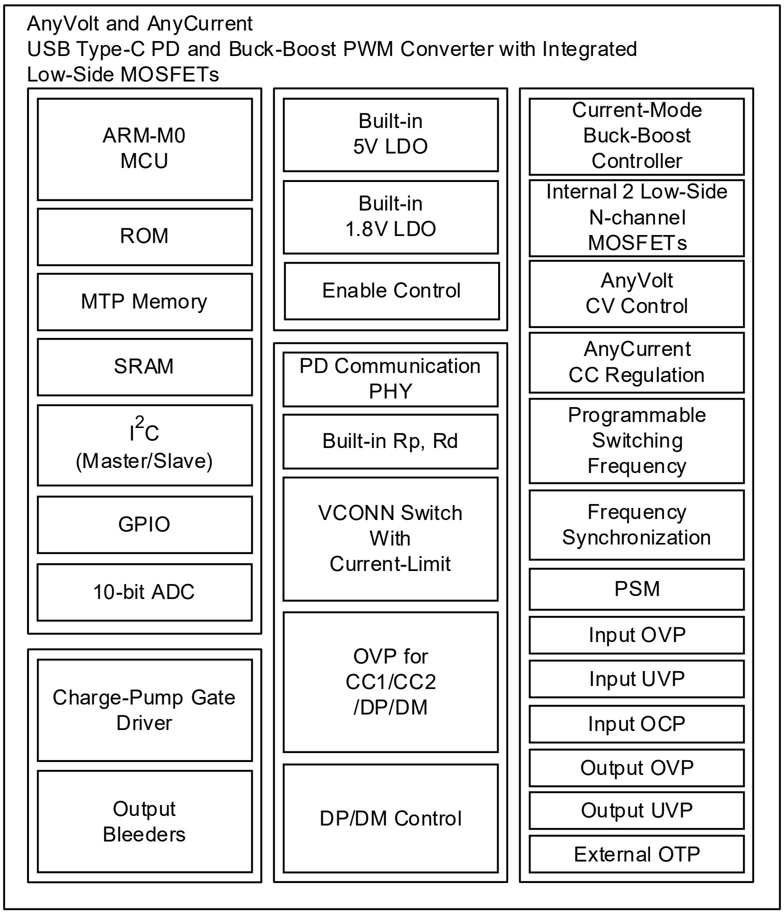
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	DM	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D- pin of a USB connector. This pin can be configured as an open-drain or push-pull GPIO pin.
2	DP	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D+ pin of a USB connector. This pin can be configured as an open-drain or push-pull GPIO pin.
3	CC2	Type-C connector Configuration Channel (CC) 2. Generally, this input/output pin is connected to USB Type-C connector CC2 terminal.
4	CC1	Type-C connector Configuration Channel (CC) 1. Generally, this input/output pin is connected to USB Type-C connector CC1 terminal.
5	CCGND	Analog ground.
6	V2	Internal 1.8V linear regulator output to supply power for internal circuitry. An MLCC (1μF typ. or greater) must be connected from this pin to ground.
7	EN	Enable control input with internal pull high source. Keep floating for normal operation. A logic-low voltage to disable the IC for power saving.

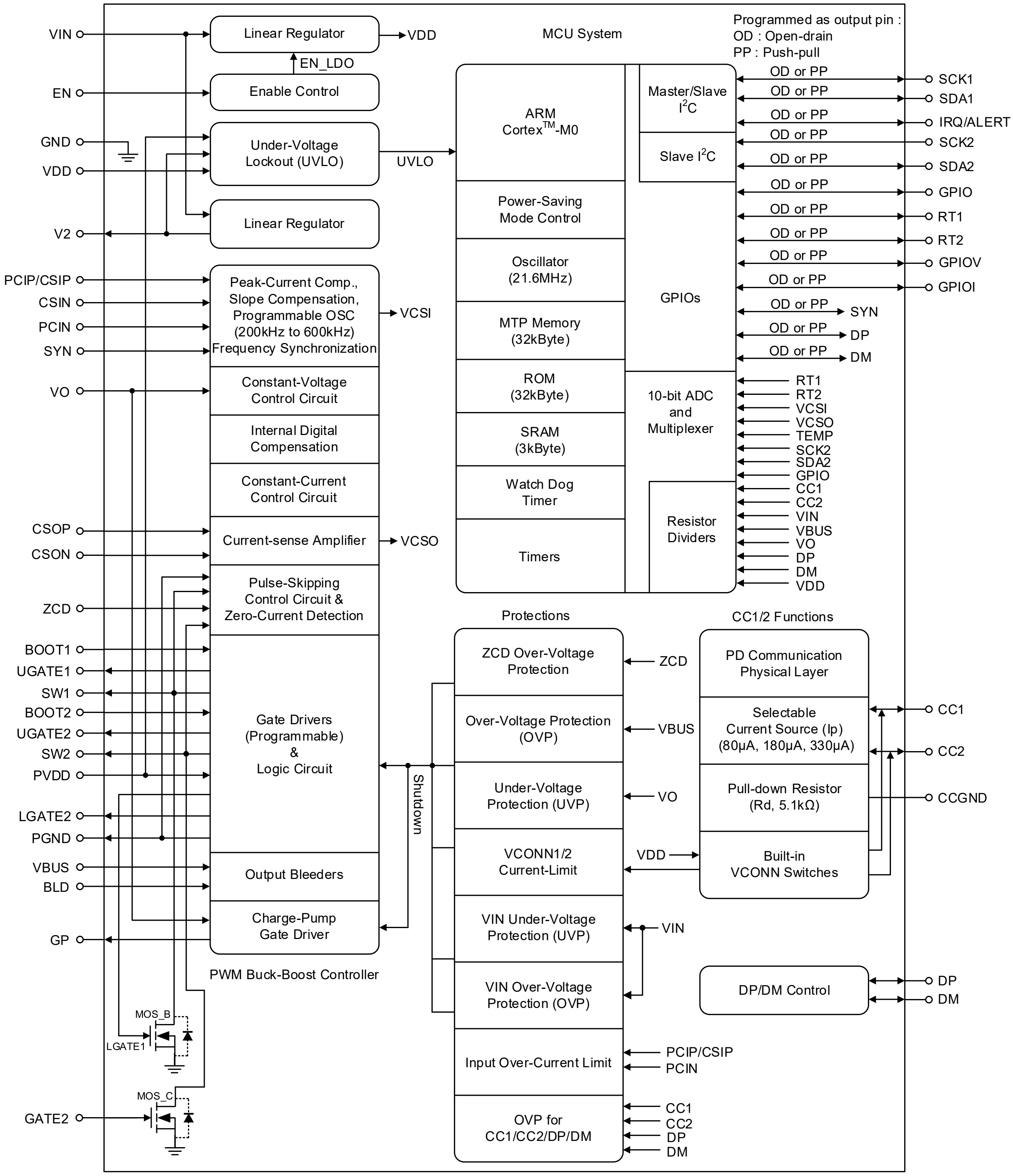
Pin No.	Pin Name	Pin Function
8	VDD	Output pin of the VIN-to-VDD linear regulator. An external MLCC (at least 4.7μF, 0805/X7R/25V) and a 5.6V Zener diode (tolerance 5.6V±2%) must be connected from this pin to GND pin. It is not recommended to connect VDD to supply other rails.
9, 38, 49, 60	GND	Analog ground.
10	VIN	Input voltage to the converter and the IC. An aluminum hybrid polymer capacitor (at least 68μF) must be connected from converter VIN to ground.
11	PCIP/CSIP	Positive peak-current signal input pin and positive average-current signal input pin.
12	CSIN	Negative average-current signal input pin.
13	PCIN	Negative peak-current signal input pin.
14	BOOT1	Bootstrap capacitor connection node. Connect a 0.1μF ceramic capacitor from this pin and the SW1 pin to power the internal 1st high-side gate driver.
15	UGATE1	1st high-side gate driver output.
16, 17, 18, 19	PGND	Internally PGND is connected to the source of the low-side switching MOSFET (QB). Ground of the low-side gate drivers and one input pin of zero-current detection at the MOSFET(QB).
20, 21, 22, 23	SW1	Internally SW1 is connected to the drain of the low-side switching MOSFET (QB). Negative power-rail pin of the 1st high-side gate driver.
24	PVDD	Bias voltage (5V typical) supply for the low-side gate drivers. It is recommended to connect an external MLCC (1μF) from this pin to PGND pin.
25, 26, 27, 28, 29, 30, 37	SW2	Internally SW2 is connected to the drain of the low-side switching MOSFET (QC). Negative power-rail pin of the 2nd high-side gate driver.
31, 32, 33, 34	PGND	Internally PGND is connected to the source of the low-side switching MOSFET (QC).
35	GATE2	Gate of the low-side switching MOSFET (QC).
36	LGATE2	2nd low-side gate driver output.
39	UGATE2	2nd high-side gate driver output.
40	BOOT2	Bootstrap capacitor connection node. Connect a 0.1μF ceramic capacitor from this pin and the SW2 pin to power the internal 2nd high-side gate driver.
41	ZCD	One input pin of zero-current detection (at the MOSFET controlled by UGATE2) and output overvoltage protection input pin.
42	BLD	Bleeder connection node. An output bleeder, comprising a pull-low NMOS, is built-in to provide another path to discharge the output capacitor of the PWM converter. Connect this pin to the converter output through an external resistor.
43	CSOP	Positive input of a current-sense amplifier to sense the output current for constant current regulation and also through an ADC to the MCU. Connect this pin to the positive terminal of output current-sense resistor via an RC filter.
44	CSON	Negative input of a current-sense amplifier for output constant-current regulation and output current detection. Connect this pin to the negative terminal of output current-sense resistor via an RC filter.
45	VO	Input of feedback voltage from converter output. The voltage is monitored for output undervoltage protection.
46	GP	Charge-pump gate diver output. It drives N-channel power MOSFET(s) to turn on/off the output power path.
47	VBUS	USB-C VBUS voltage input. The voltage at this pin is monitored for USB-C VBUS overvoltage protection with an 8-bit programmable threshold voltage.
48	GPIOV	General-purpose input/output.
50	GPIOI	General-purpose input/output.

Pin No.	Pin Name	Pin Function
51	RT2	Open-drain/push-pull GPIO, analog input or external over-temperature protection (EOTP)input pin. Connect an NTC from this pin to GND pin for the EOTP.
52	RT1	Open-drain/push-pull GPIO, analog input or external over-temperature protection (EOTP)input pin. Connect an NTC from this pin to GND pin for the EOTP.
53	IRQ/ALERT	Interrupt input/output pin. The RTQ7892B-QT can do emergency control when it receives a low-level signal via this pin. An external MCU can check the slave I^2C registers to do emergency control when it receives a low-level signal via this pin. This pin can be configured as an open-drain or push-pull GPIO pin.
54	SCK1	Open-drain clock signal input/output pin of the Slave/Master I^2C interface. This pin can be configured as an open-drain or push-pull GPIO pin.
55	SDA1	Open-drain data signal input/output pin of the Slave/Master I^2C interface. This pin can be configured as an open-drain or push-pull GPIO pin.
56	SCK2	Open-drain clock signal input/output pin of the Slave I^2C interface. This pin can be configured as an open-drain or push-pull GPIO pin.
57	SDA2	Open-drain data signal input/output pin of the Slave I^2C interface. This pin can be configured as an open-drain or push-pull GPIO pin.
58	SYN	Switching frequency synchronization in two port applications.
59	GPIO	General-purpose input/output.
61 (Exposed Pad)	SW2	Internally SW2 is connected to the drain of the low-side switching MOSFET (QC). Negative power-rail pin of the 2^{nd} high-side gate driver.
62 (Exposed Pad)	SW1	Internally SW1 is connected to the drain of the low-side switching MOSFET (QB). Negative power-rail pin of the 1^{st} high-side gate driver.
63 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Simplified Functional Diagram



10 Functional Block Diagram



11 Absolute Maximum Ratings

(Note 2)

- V2 to GND ---------- –0.3V to 2.5V
- VDD, PVDD to GND ---------- –0.3V to 6.5V
- GPIOV, GPIOI to GND ---------- –0.3V to 6.5V
- VBUS, CSOP, CSON, VO, BLD, ZCD to GND ---------- –0.3V to 25V
- CSOP to CSON Voltage ($V_{CSOP-CSON}$) ---------- –5V to 5V
- GP to GND ---------- –0.3V to 33V
- VIN, PCIN, PCIP/CSIP, CSIN to GND ---------- –0.3V to 36V
- ZCD to CSOP ($V_{ZCD-CSOP}$) and
  ZCD to CSON Voltage ($V_{ZCD-CSON}$) ---------- –0.3V to 6.5V
- PCIP/CSIP to CSIN Voltage ($V_{PCIP/CSIP-CSIN}$) ---------- –5V to 5V
- VIN to PCIP/CSIP ($V_{VIN-PCIP/CSIP}$) and
  VIN to PCIN Voltage ($V_{VIN-PCIN}$) and
  VIN to CSIN Voltage ($V_{VIN-CSIN}$) ---------- –0.3V to 6.5V
- PCIP/CSIP to PCIN Voltage ($V_{PCIP/CSIP-PCIN}$) ---------- –5V to 5V
- EN to GND ---------- –0.3V to 6.5V
- I^2C Pins (SCK1, SDA1, IRQ/ALERT, SCK2, SDA2) to GND ---------- –0.3V to 6.5V
- GPIO Pins (SYN, GPIO, RT1, RT2) to GND ---------- –0.3V to 6.5V
- DP, DM to GND ---------- –0.3V to 25V
- CC1, CC2 to GND ---------- –0.3V to 25V
- BOOT1/2 to SW1/2 ($V_{BOOT-SW}$) ---------- –0.3V to 6.5V
- UGATE1/2 to SW1/2 ---------- –0.3V to $V_{BOOT-SW}$ + 0.3V
- SW1 to GND (DC) ---------- –0.3V to 30V
  (< 20ns) ---------- –5V to 36V
- SW2 to GND (DC) ---------- –0.3V to 25V
  (< 20ns) ---------- –5V to 30V
- LGATE2, GATE2 to PGND ---------- –0.3V to V_{PVDD} + 0.3V
- PGND, CCGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN7x7-62 ---------- 3.26W
- Package Thermal Resistance (Note 3)
  WQFN7x7-62, θ_{JA} ---------- 38.37°C/W
  WQFN7x7-62, θ_{JC} ---------- 2.8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Mode) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- PWM Converter Input Voltage, V_{IN} --- 4.5V to 30V
- PWM Converter Output Voltage, V_{OUT} -- 3V to 22V
- VDD Output Voltage/PVDD Supply Voltage --- 4.5V to 5.5V
- Junction Temperature Range --- –40°C to 150°C
- Ambient Temperature Range --- –40°C to 125°C
- Minimum MTP Memory Write/Erase Cycles -- 100cycles at 25°C

Note 5. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(V_{DD} = V_{PVDD} = 5V, T_J = –40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD and V2 Linear Regulators (VDD LDO and V2 LDO), Undervoltage-Lockout (UVLO) and Enable Control						
VDD Output Voltage (5.0V Normal/4.3V DGM)	V_{VDD_REG}	In normal mode, V_{IN} = 12V, Io = 0mA, C_{VDD} = 4.7μF	4.7	5	5.3	V
		In deep-green mode, V_{IN} = 12V, Io = 0mA, C_{VDD} = 4.7μF	3.9	4.2	4.5	
VDD Load Regulation Drop Voltage (5.0V Normal)	V_{VDD_DROP12}	V_{IN} = 12V, Io = 100mA, C_{VDD} = 4.7μF	--	0.3	--	V
	V_{VDD_DROP5}	V_{IN} = 5V, Io = 100mA, C_{VDD} = 4.7μF	--	0.3	--	V
VDD Short Current	I_{VDD_SHORT}	V_{IN} = 12V, V_{DD} = 3V short to GND	--	150	--	mA
VIN Normal Operating Current	I_{VIN_OP}	V_{IN} = 12V, PWM = MCU = on, digital output pins = open	--	10	--	mA
VIN Operating Current in Deep Green-Mode (DGM)	I_{VIN_DGM}	V_{IN} = 12V, PWM = off, MCU = off, no load current, CC1/CC2 RX detection	--	0.5	--	mA
VIN Operating Current in Deep Green-Mode (DGM_LQ)	$I_{VIN\_DGM\_LQ}$	V_{IN} = 12V, PWM = MCU = off, CC1/CC2 falling detection only	--	120	--	μA
VIN Operation Current in EN Reset-Mode	I_{VIN_RST}	V_{IN} = 12V, EN = 0, PWM = MCU = off, digital output pins = open, VDD off	--	10	50	μA
V2 Output Voltage	V_{V2_REG}	In normal mode I_{V2} = 20mA load, C_{V2} = 1μF	1.62	1.8	1.98	V
V2 Short-Circuit Current	I_{V2_SHORT}	V_{IN} =12V, V_{DD} = 5V V2 short to GND	--	50	--	mA
VDD POR Voltage Threshold	$V_{VDD\_POR\_R}$	V_{DD} rising	3.8	4	4.2	V
VDD UVLO Voltage Hysteresis	$V_{VDD\_UVLO\_HYS}$	V_{DD} falling	--	0.225	--	V
PVDD POR Threshold	$V_{PVDD\_POR\_R}$	V_{PVDD} rising	3.8	4	4.2	V
PVDD UVLO Hysteresis	$V_{PVDD\_UVLO\_HYS}$	V_{PVDD} falling	--	0.2	--	V
PVDD Input Current in PWM Shutdown	$I_{PVDD\_PWM\_SD}$	V_{IN} = 12V, V_{DD} = 5V, V_{PVDD} = 5V, PVDD_EN = off, PWM = off	--	--	3	μA
EN Internal Pull-High Voltage	V_{EN_PH}	V_{IN} = 12V, V_{DD} = 5V, EN open	3	--	5	V
EN Internal Pull-High Resistor	R_{EN_PH}	V_{IN} = 12V, V_{DD} = 5V, EN = 0	--	1200	--	kΩ
EN Threshold Voltage	V_{IH_EN}	V_{IN} = 12V, V_{DD} = 5V	1.5	--	VDD	V
	V_{IL_EN}	V_{IN} = 12V, V_{DD} = 5V	0	--	0.4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller – Programmable Oscillator						
PWM Frequency Range	f_{PWM}	Programmable	200	--	600	kHz
PWM Frequency Accuracy	f_{PWM_ACC}	f_{PWM} = 300kHz/400kHz	–10	--	10	%
MCU Section						
MCU Clock Frequency	f_{MCU}		19.4	21.6	23.8	MHz
OSC 80k Frequency in Deep Green-Mode	f_{DGM_80k}		--	80	--	kHz
PWM Controller – Constant-Voltage (CV) Control Loop						
CV Regulated Voltage Range at VO Pin	V_{VO_REG}	Programmable (11-bit), 9.93mV/step	3	--	22	V
CV Regulated Voltage Accuracy at VO Pin (CVDAC_11bit)	$V_{VO\_REG\_ACC1}$	V_{OUT} = 3.3V/5V/9V	–120	--	120	mV
CV Regulated Voltage Accuracy at VO Pin (CVDAC_11bit)	$V_{VO\_REG\_ACC2}$	V_{OUT} = 12V/15V/20V	–200	--	200	mV
PWM Controller – Constant-Current (CC) Control Loop and Output						
CSON and CSOP Operating Voltage Range	V_{CSOPN_OP}		3	--	22	V
CC Regulated Voltage Range between the CSOP and CSON Pins (CCDAC_10bit)	V_{REF_CC}	CSAgain = 40, programmable (10-bit), 0.0625mV/step (typ.), V_{CSON} and V_{CSOP} > 3V	5	--	35	mV
CC Regulated Voltage Accuracy between the CSOP and CSON Pins	$V_{REF\_CC\_ACC}$	CSAgain = 40, nominal V_{REF_CC} = 5mV/15mV/25mV	–1	--	1	mV
CSOP/CSON Input Current	I_{CSOPN}	PWM bias = on	--	--	50	μA
		PWM bias = off	--	--	1	
CSA Detection Voltage Range between the CSIP and CSIN Pins	V_{CSIPN}	CSAgain = 40	5	--	35	mV
CSIP/CSIN Input Current in VinCSA	I_{CSIPN}	PWM bias = on	--	--	50	μA
		PWM bias = off	--	--	1	
PWM Controller – Input Current Comparison, Slope Compensation						
Maximum Input Overcurrent Protection (INOC) Voltage Threshold Range	V_{TH_CSMAX}	Programmable	30	--	150	mV
Maximum Input Overcurrent Protection (INOC) Voltage Threshold Accuracy	$V_{TH\_CSMAX\_ACC}$	V_{TH_CSMAX} = 30mV, 120mV	–10	--	10	mV
Voltage Rate Range of Slope Compensation	$Rate_{SC}$	Programmable	0	--	80	mV/μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PCIP/CSIP Input Current in INOC	I_{PCIPN_INOC}	In PSM, V_{CSIP} = 24V	--	--	50	μA
		PWM bias = off, V_{CSIP} = 24V	--	--	3	
PCIN Input Current	I_{PCIN}	In PSM, V_{CSIN} = 24V	--	--	30	μA
		PWM bias = off, V_{CSIN} = 24V	--	--	3	
PWM Controller – Zero-Current Detection (ZCD)						
MOS-D ZCD Voltage Threshold between SW2 and ZCD Pins	V_{TH_ZCDD}	To compare the SW2-to-ZCD voltage	--	4	--	mV
MOS-B ZCD Current Threshold between PGND and SW1 Pins	I_{TH_ZCDB}	To compare the PGND-to-SW1 current	--	300	--	mA
ZCD Input Current	I_{ZCD}	In PSM, V_{ZCD} = 20V	--	--	300	μA
		PWM bias = off, V_{ZCD} = 20V	--	--	90	
PWM Controller – Gate Drivers and Internal MOSFET						
UGATE1/2 Pull-High Resistance	$R_{UGATE1/2\_PH}$	Programmable, $V_{BOOT1/2}$ – $V_{SW1/2}$ = 5V, $V_{BOOT1/2}$ – $V_{UGATE1/2}$ = 0.1V	--	1.7	--	Ω
			--	5	--	
			--	10	--	
			--	20	--	
UGATE1/2 Pull-Low Resistance	$R_{UGATE1/2\_PL}$	$V_{UGATE1/2}$ – $V_{SW1/2}$ = 0.1V	--	0.8	--	Ω
LGATE1/2 Pull-High Resistance	$R_{LGATE1/2\_PH}$	Programmable, V_{PVDD} – $V_{LGATE1/2}$ = 0.1V	--	1.7	--	Ω
			--	5	--	
			--	10	--	
			--	20	--	
LGATE1/2 Pull-Low Resistance	$R_{LGATE1/2\_PL}$	$V_{LGATE1/2}$ = 0.1V	--	0.8	--	Ω
Dead-Time at LGATE1/2 Falling Edge	$t_{LGATE1/2\_F\_DEAD}$		--	40	--	ns
Dead-Time after UGATE1/2 Falling Edge	$t_{UGATE1/2\_F\_DEAD}$		--	40	--	ns
QB Buck Low-Side MOSFET On-Resistance	R_{DSON_QB}	PVDD = 5V, PGND = 0, IDS = 1A, SW1-to-PGND	--	30	--	mΩ
QC Boost Low-Side MOSFET On-Resistance	R_{DSON_QC}	PVDD = 5V, PGND = 0, IDS = 1A, SW2-to-PGND	--	10	--	mΩ
System Protections – Overvoltage, Undervoltage, and Overcurrent Protections (OVP, UVP, and OCP)						
VIN UVP Voltage Threshold Range	V_{VIN_UVP}	Programmable, (8-bit), 125mV/step (typ.)	4	--	27	V
VIN UVP Voltage Threshold Accuracy	$V_{VIN\_UVP\_ACC}$	Setting of V_{TH_VINUVP} = 5V/10V/15V	–5	--	5	%
VIN OVP Voltage Threshold Range	V_{VIN_OVP}	Programmable, (8-bit), 125mV/step (typ.)	4	--	30	V
VIN OVP Voltage Threshold Accuracy	$V_{VIN\_OVP\_ACC}$	Setting of V_{TH_VINOVP} = 19V/26V	–5	--	5	%

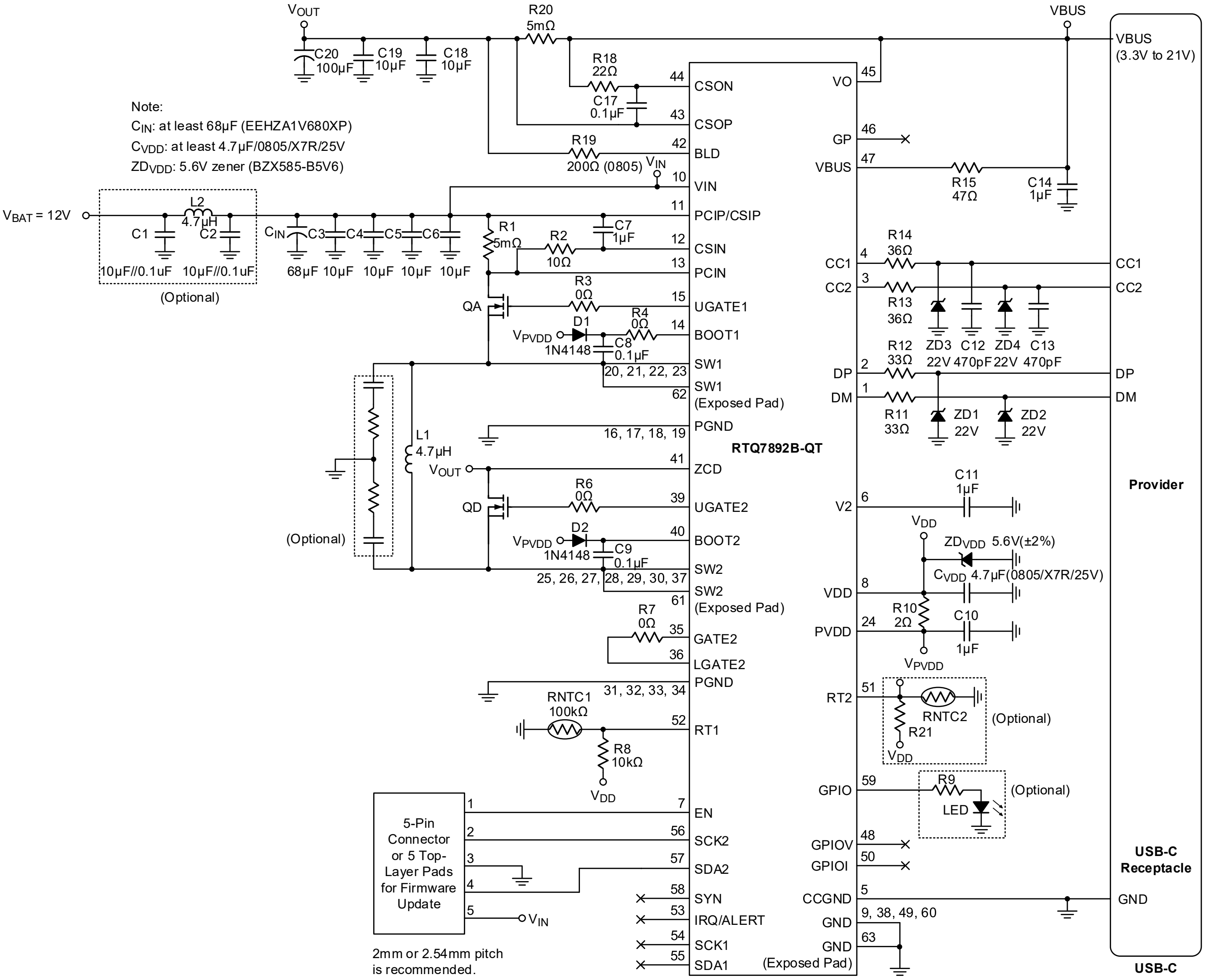
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS OVP Voltage Threshold Range	V_{VBUS_OVP}	Programmable, (8-bit), 100mV/step (typ.)	3.3	--	24	V
VBUS OVP Voltage Threshold Accuracy	$V_{VBUS\_OVP\_ACC1}$	Setting of V_{TH_VBUSOV} = 12V/20V	–5	--	5	%
VBUS OVP Voltage Threshold Accuracy	$V_{VBUS\_OVP\_ACC2}$	Setting of V_{TH_VBUSOV} = 3.3V/5V	–0.3	--	0.3	V
ZCD Pin OVP Voltage Threshold (VO Pin Open, OVP)	V_{ZCD_OVP}		–7	125	7	%
VO UVP Voltage Threshold Range	V_{VO_UVP}	Programmable, (8-bit), 100mV/step (typ.)	3	--	20	V
VO UVP Voltage Threshold Accuracy	$V_{VO\_UVP\_ACC1}$	Setting of V_{TH_VOUV} = 5V/12V/20V	–5	--	5	%
VO UVP Voltage Threshold Accuracy	$V_{VO\_UVP\_ACC2}$	Setting of V_{TH_VOUV} = 3V	–0.2	--	0.2	V
USB PD Controller – CC1/2 Voltage Detections, BMC Transmitter/Receiver and VCONN Switches						
CC1/2 Pull-Up Current Source – 1	Ip1	For default USB power	64	80	96	μA
CC1/2 Pull-Up Current Source – 2	Ip2	For 1.5A and 5V	165.6	180	194.4	μA
CC1/2 Pull-Up Current Source – 3	Ip3	For 3A and 5V	303.6	330	356.4	μA
CC1/2 Open-Loop Clamping Voltage for pull-up Source	V_{CC_CLAMP}	V_{DD} = 5V @ pull-up Current 330μA	2.9	3.25	--	V
CC1/2 Pull-Down Resistor	Rd	V_{DD} = 5V @ pull-up 56kΩ	4.6	5.1	5.6	kΩ
Transmitter High-Level Output Voltage Range	$V_{OH\_CC1/2}$		1.05	1.125	1.2	V
Transmitter Low-Level Output Voltage Range	$V_{OL\_CC1/2}$		0	--	75	mV
Rising Time of the Transmitter Output Voltage	t_{RISE}	From 10% to 90%, CL=200pF to 600pF	300	--	--	ns
Falling Time of the Transmitter Output Voltage	t_{FALL}	From 90% to 10%, CL= 200pF to 600pF	300	--	--	ns
Receiver High-Level Input Voltage Range	$V_{IH\_CC1/2}$		--	0.8	--	V
			--	0.7	--	
			--	0.6	--	
			--	0.5	--	
Receiver Low-Level Input Voltage Range	$V_{IL\_CC1/2}$		--	0.5	--	V
			--	0.4	--	
			--	0.3	--	
			--	0.2	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCONN On-Resistance of VDD-to-CC1/2 MOSFET	R_{ON_VCONN}	V_{DD} = 5V, output current = 20mA	--	10	15	Ω
VCONN Output Voltage Drop VDD-to-CC1/2 MOSFET	V_{VCONN_DROP}	V_{DD} = 5V, output current = 20mA	--	0.2	0.3	V
VCONN Current-Limit Threshold	V_{VCONN_LIM}	CC1/CC2 = GND	--	50	--	mA
CC1/CC2 Short to VBUS Protection	$V_{CC1/2\_OVP}$		5.7	6	6.3	V
DPDM Interfaces in Source Role Operation						
On-Resistance of DP-to-DM MOSFET	R_{ON_DPDM}		--	--	40	Ω
DP/DM High-Level Output Voltage	V_{OH_DPDM}	Sourcing current = 2mA	--	3.3	--	V
			--	1.8	--	
DP/DM Low-Level Output Voltage	V_{OL_DPDM}	Sinking current = 2mA	--	--	0.3	V
DP/DM Voltage Falling Threshold for Plug-Out Detection	V_{REF1_DPDM}		--	0.3	--	V
			--	0.4	--	
			--	0.5	--	
			--	0.6	--	
Input Voltage Offset Selection V_{REF2H_DPDM}, V_{REF2L_DPDM}	V_{IN_LEV}		--	0	--	V
			--	0.4	--	
RX Upper Input Voltage Threshold	V_{REF2H_DPDM}	V_{IN_LEV} = 0V	--	0.8	--	V
			--	1.3	--	
			--	1.9	--	
			--	2.05	--	
		V_{IN_LEV} = 0.4V	--	1.2	--	
			--	1.7	--	
			--	2.3	--	
			--	2.45	--	
RX Lower Input Voltage Threshold	V_{REF2L_DPDM}	V_{IN_LEV} = 0V	--	0.6	--	V
			--	1.1	--	
			--	1.8	--	
			--	1.95	--	
		V_{IN_LEV} = 0.4V	--	1	--	
			--	1.5	--	
			--	2.2	--	
			--	2.35	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DP/DM Internal Pull-Low Resistance	R_{DWN_DPDM}		16	20	24	kΩ
DP/DM Output Voltage for Divider Mode	V_{DPDM}		1.13	1.2	1.27	V
			1.88	2	2.12	
			2.57	2.7	2.84	
			3.14	3.3	3.47	
Output Resistance DP/DM for Divider Mode 2.0/2.7/3.3	R_{DPDM}		--	30	--	kΩ
Output Resistance DP/DM for Divider Mode 1.2	$R_{DPDM\_1.2V}$		--	100	--	kΩ
DP/DM Output Voltage-1 for SRC	V_{SRC1_DPDM}		--	0.6	--	V
DP/DM Output Voltage-2 for SRC	V_{SRC2_DPDM}		--	3.3	--	V
DP/DM Short to VBUS Protection	V_{DPDM_OVP}		5.415	5.7	5.985	V
Charge-Pump Gate Drivers and Bleeders						
GP On-Resistance of Pull-Low MOSFET	R_{GP_PL}	Pull-low NMOS is on, sinking I_{GP} = 10mA, V_{DD} = 5V	--	--	200	Ω
Maximum GP Voltage	V_{GP_MAX}	V_{VO} = 20V, $R_{GP\text{-}to\text{-}GND}$ = 667kΩ	V_{VO} + 4V	V_{VO} + 4.5V	V_{VO} + 10V	V
BLD On-Resistance of Pull-Low MOSFET	R_{BLD_PL}	Pull-low NMOS is on, sinking I_{BLD} = 10mA, V_{DD} = 5V	--	20	40	Ω
BLD Leakage Current	I_{BLD_LK}	V_{BLD} = 20V, pull-low NMOS is off V_{DD} = 5V	--	--	1	μA
VBUS Bleeder Resistor	R_{VBUS_BLD}	Pull-low NMOS is on V_{DD} = 5.0V & V_{BUS} = 23V	--	1.2	--	kΩ
Digital Input and Output – I²C Pins (IRQ/ALERT, SCK1, SDA1, SCK2 and SDA2) and GPIO Pins (IRQ/ALERT, SCK1, SDA1, SCK2, SDA2, GPIOV, GPIOI, SYN, GPIO, RT1 and RT2)						
I²C/GPIO High-Level Input Voltage Range	$V_{IH\_I2C/GPIO}$	For the pins configured as input pins	1.5	--	--	V
I²C/GPIO Low-Level Input Voltage Range	$V_{IL\_I2C/GPIO}$	For the pins configured as input pins	--	--	0.4	V
I²C/GPIO High-Level Output Voltage	$V_{OH\_I2C/GPIO}$	Sourcing current = 2mA, for the pins configured as push-pull output pins	VDD – 1.5V	VDD – 0.8V	--	V
I²C/GPIO Low-Level Output Voltage	$V_{OL\_I2C/GPIO}$	Sinking current = 2mA	--	--	0.3	V
I²C/GPIO Leakage Current	$I_{I2C/GPIO\_LK}$	Pin input voltage = 5V	--	--	1	μA
RT1/2 Current Source	I_{RT1}	$V_{RT1/2}$ < 2.7V	92	100	108	μA

14 Typical Application Circuit

14.1 Without VBUS Blocking MOSFET



14.2 With VBUS Blocking MOSFET

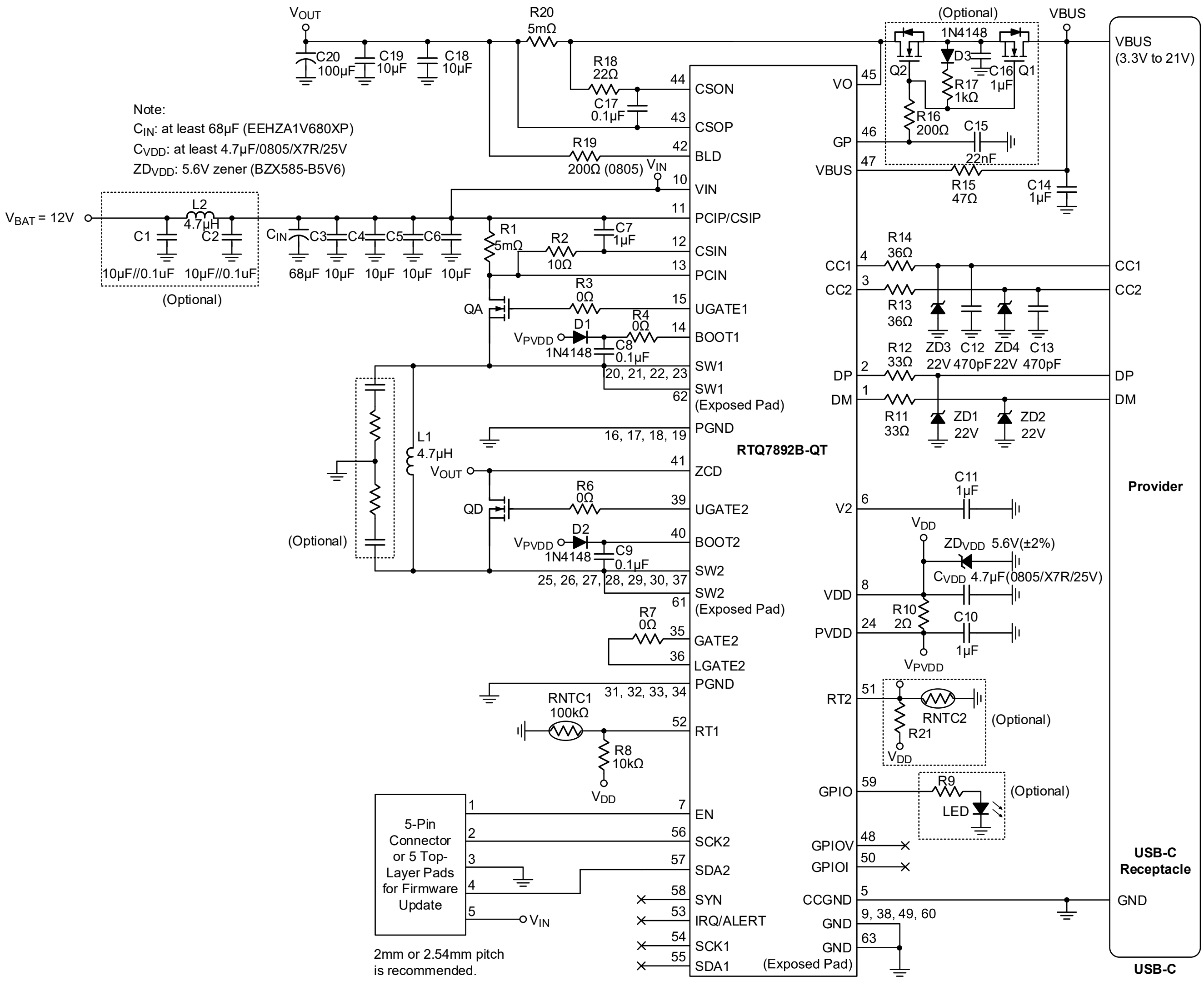
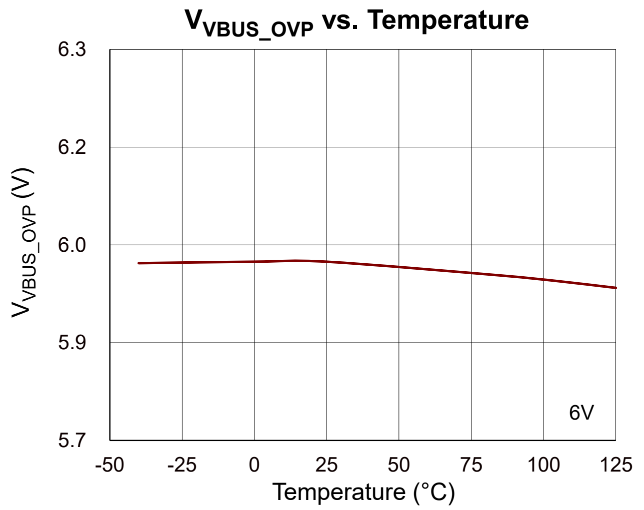
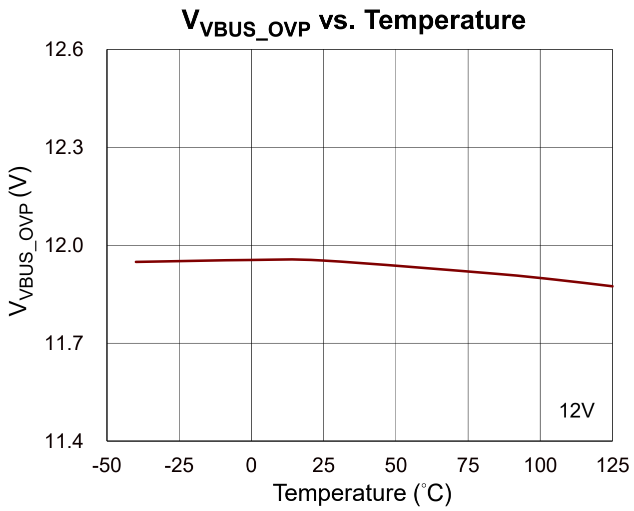


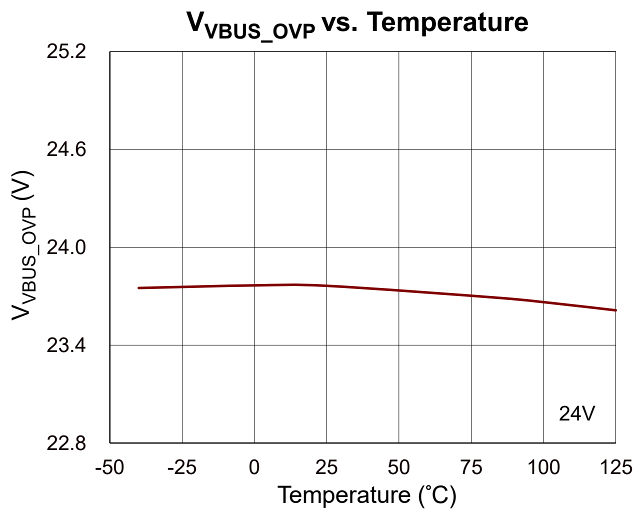
Table 1.

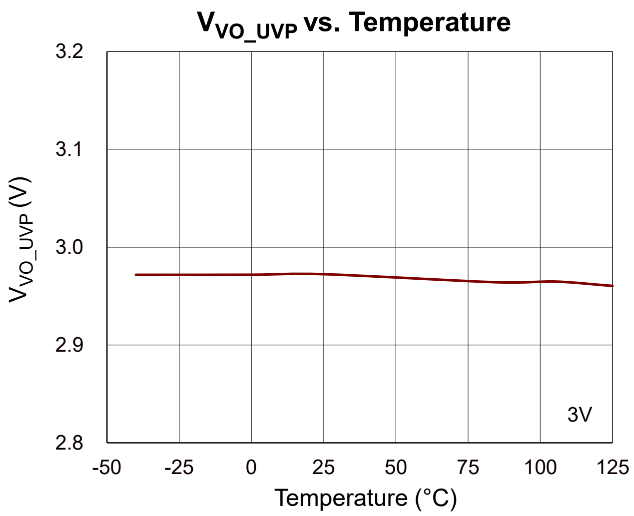
VBUS Blocking MOSFET		Note
Q2	Q1	
Y	Y	The safe VBUS protection circuit.
Y	N	To prevent current from VIN to VBUS.
N	Y	To prevent current from VBUS to VIN.
N	N	VBUS does not have any protection circuit.

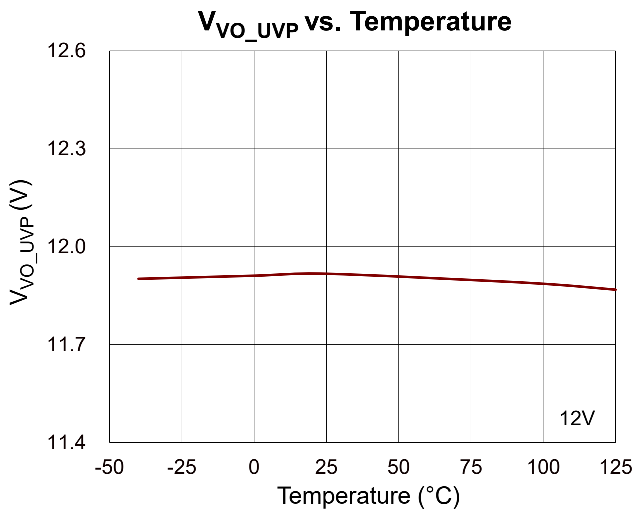
15 Typical Operating Characteristics

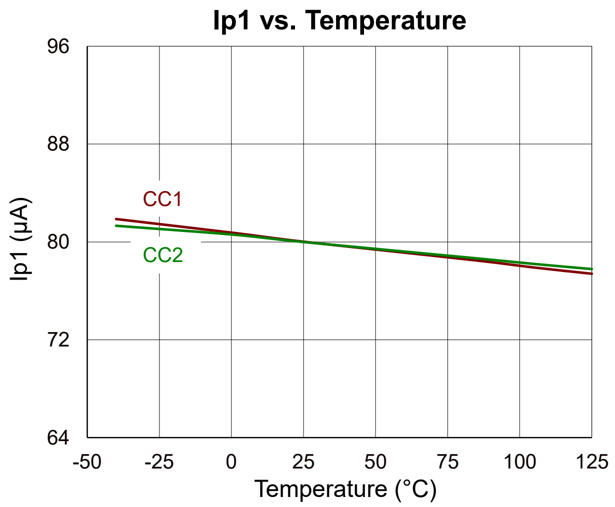


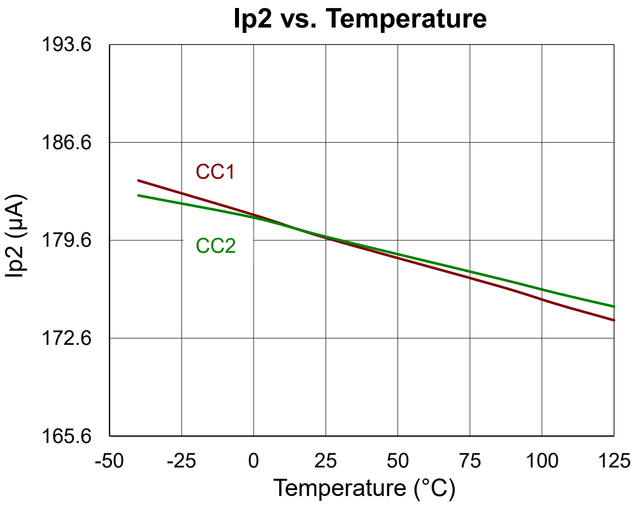


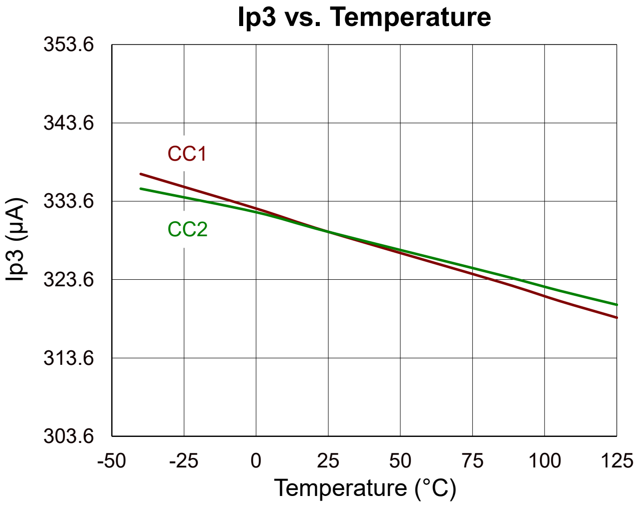


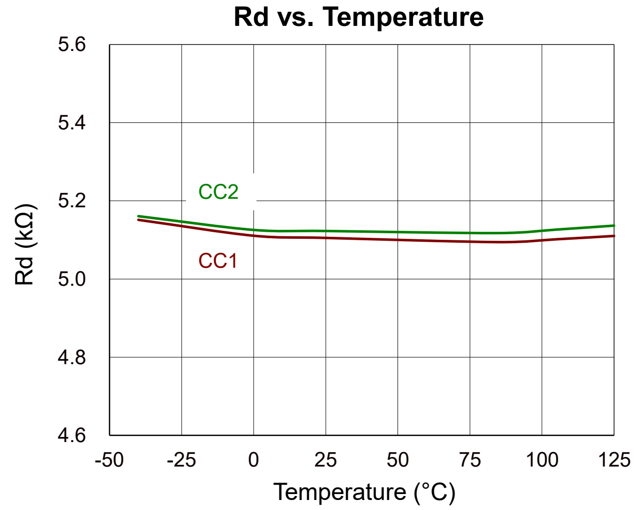


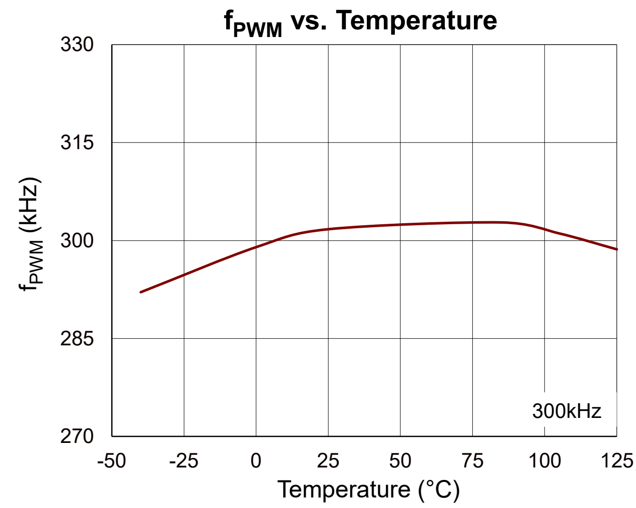


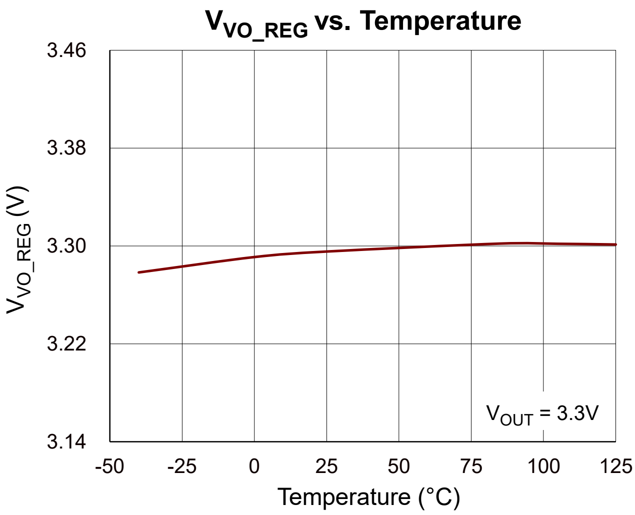


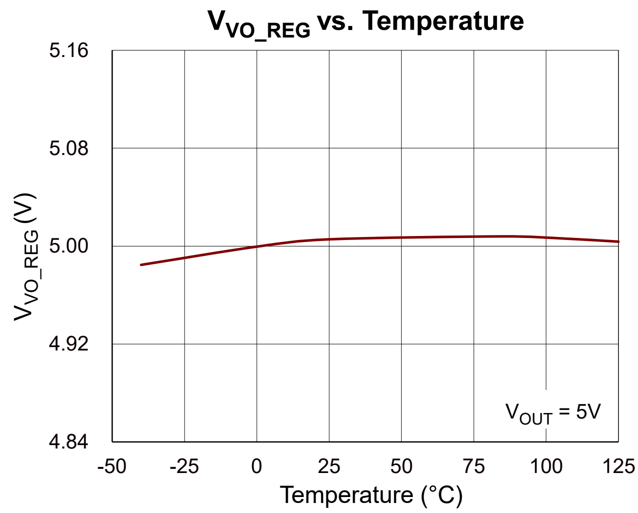

Ip2 vs. Temperature
193.6
186.6
179.6
172.6
165.6
Ip2 (μA)
CC1
CC2
-50 -25 0 25 50 75 100 125
Temperature (°C)

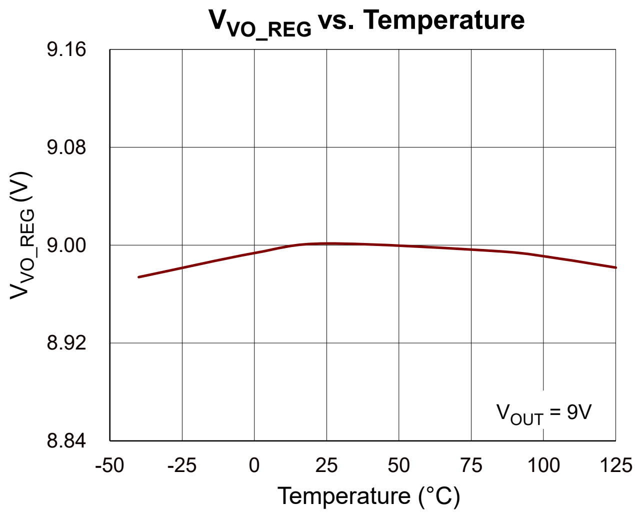

Ip3 vs. Temperature
353.6
343.6
333.6
323.6
313.6
303.6
Ip3 (μA)
CC1
CC2
-50 -25 0 25 50 75 100 125
Temperature (°C)

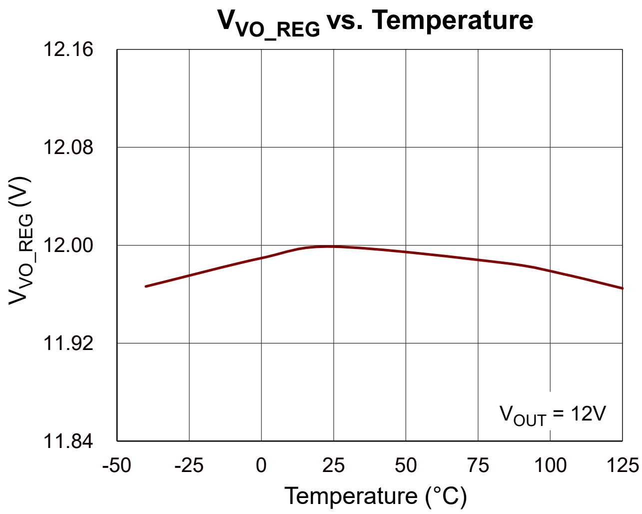

Rd vs. Temperature
5.6
5.4
5.2
5.0
4.8
4.6
Rd (kΩ)
CC2
CC1
-50 -25 0 25 50 75 100 125
Temperature (°C)

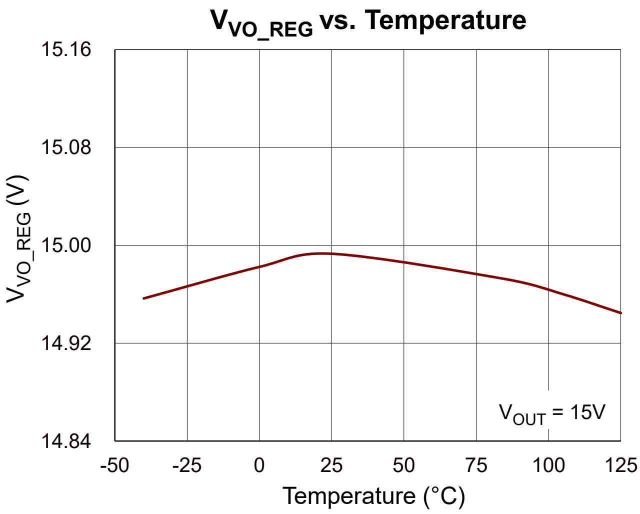

fPWM vs. Temperature
330
315
300
285
270
fPWM (kHz)
300kHz
-50 -25 0 25 50 75 100 125
Temperature (°C)

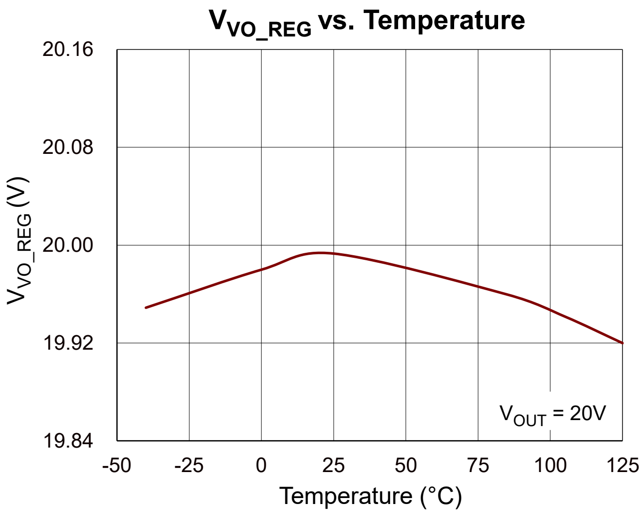

VVO_REG vs. Temperature
3.46
3.38
3.30
3.22
3.14
VVO_REG (V)
VOUT = 3.3V
-50 -25 0 25 50 75 100 125
Temperature (°C)

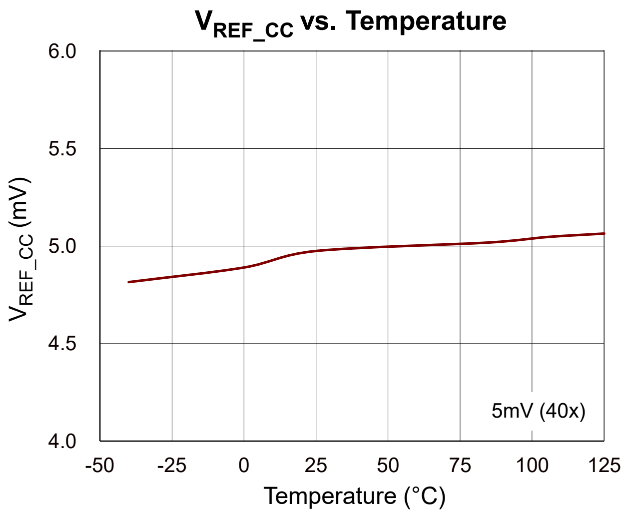

VVO_REG vs. Temperature
5.16
5.08
5.00
4.92
4.84
VVO_REG (V)
VOUT = 5V
-50 -25 0 25 50 75 100 125
Temperature (°C)

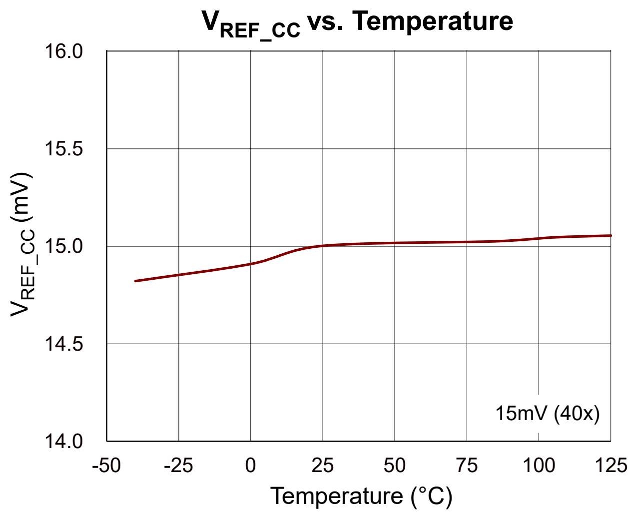

V_{VO_REG} vs. Temperature
9.16
9.08
9.00
8.92
8.84
V_{VO_REG} (V)
V_{OUT} = 9V
-50 -25 0 25 50 75 100 125
Temperature (°C)

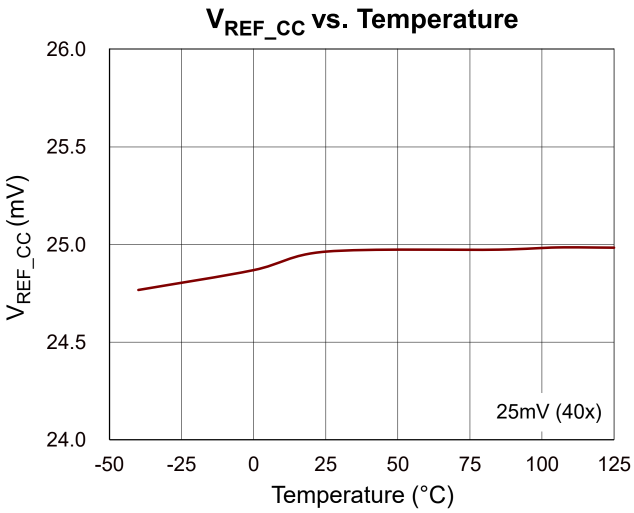

V_{VO_REG} vs. Temperature
12.16
12.08
12.00
11.92
11.84
V_{VO_REG} (V)
V_{OUT} = 12V
-50 -25 0 25 50 75 100 125
Temperature (°C)

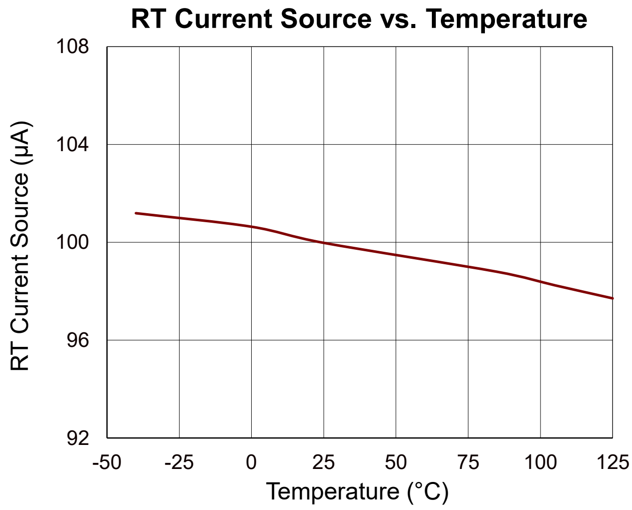

V_{VO_REG} vs. Temperature
15.16
15.08
15.00
14.92
14.84
V_{VO_REG} (V)
V_{OUT} = 15V
-50 -25 0 25 50 75 100 125
Temperature (°C)


V_{VO_REG} vs. Temperature
20.16
20.08
20.00
19.92
19.84
V_{VO_REG} (V)
V_{OUT} = 20V
-50 -25 0 25 50 75 100 125
Temperature (°C)


V_{REF_CC} vs. Temperature
6.0
5.5
5.0
4.5
4.0
V_{REF_CC} (mV)
5mV (40x)
-50 -25 0 25 50 75 100 125
Temperature (°C)


V_{REF_CC} vs. Temperature
16.0
15.5
15.0
14.5
14.0
V_{REF_CC} (mV)
15mV (40x)
-50 -25 0 25 50 75 100 125
Temperature (°C)


V_{REF_CC} vs. Temperature
26.0
25.5
25.0
24.5
24.0
V_{REF_CC} (mV)
-50
-25
0
25
50
75
100
125
Temperature (°C)
25mV (40x)


RT Current Source vs. Temperature
108
104
100
96
92
RT Current Source (μA)
-50
-25
0
25
50
75
100
125
Temperature (°C)

16 Operation

The RTQ7892B-QT is a versatile USB Type-C Power Delivery (USB-C PD) and PWM buck-boost converter with integrated low-side MOSFETs designed especially for applications as Providers. It is a highly integrated solution with the following main functional blocks: MCU System, PWM buck-boost controller, protections and CC1/2 functions as presented in the Functional Block Diagram.

The MCU system embeds an ARM Cortex-M0 MCU, a multi-time programming (MTP) memory, a ROM, a SRAM, a 10-bit ADC (analog to digital converter), two I^2C interfaces (slave and master), and GPIO (general purpose input or output) pins. The MCU system is programmed to perform power controls, customized functions, as a policy engine and a device policy manager. This MCU reports the operating status of PD operation, such as present input/output voltage, output current and external temperature to an EC (embedded controller) or AP (application processor) and receives commands from the EC/AP, acting as a system policy manager, via the slave I^2C interface. The GPIO pins can be used to control high-speed multiplexers or other customized functions.

The PWM buck-boost controller consists of an AnyVolt constant-voltage (CV) control circuit (9.93mV/step, typical), an AnyCurrent constant-current (CC) control circuit, an output current-sense amplifier (7.8mA to 12.5mA/step, depending on the current-sense resistor), built-in gate drivers, one charge-pump gate driver and output bleeders (at BLD and VBUS pins). Either the CV or the CC control circuit regulates the output voltage or current through peak-current mode PWM operation. Diode emulation function and pulse-skipping mode (PSM) are built in to improve power efficiency at light loads. The output current-sense amplifier (OCS-AMP) allows current-sense resistors as low as 5mΩ to reduce power loss. Moreover, the charge-pump driver adopts N-channel MOSFETs for on/off control of output power-path, instead of P-channel MOSFETs, which have higher costs. In operation the output bleeders at BLD and VBUS pins can be turned on to discharge the output voltage (VBUS) during the VBUS negative transition, in the hard reset process, or after the removal of the USB-C connector.

The PD Safe power delivery operation consists of overvoltage protection (OVP) at the VBUS pin, undervoltage protection at the VO pin, output CC regulation and VCONN1/2 output current-limit function. With the PD Safe feature, trip levels of the OVP and UVP can be set dynamically for each output voltage target. The CC regulation level is also adaptively programmed according to the current level in full load.

The “CC1/2 Functions” block consists of the physical layer, three selectable levels of the pull-up current sources Ip (instead of resistors Rp), a controllable pull-down resistor Rd and programmable V_{CONN} power-path switches.

16.1 Undervoltage-Lockout (UVLO)

The RTQ7892B-QT UVLO function continuously monitors bias voltages at the VDD and V2 pins. When both supply voltages (V_{DD} and V_{V2}) rise above the respective rising UVLO thresholds, the internal UVLO signals will go low to activate the MCU. In addition, the IC also monitors the bias voltage at the PVDD pin for UVLO function. The PWM buck-boost controller will only be activated when all UVLO signals go low; otherwise, the MCU or PWM controllers will be kept in the undervoltage-lockout state to prevent any undesirable operation.

16.2 Pulse-Skipping Mode (PSM) with Diode Emulation

When a switch-mode converter operates in light load conditions, most power loss is caused by switching losses. To reduce switching loss in light load conditions, the switching frequency needs to be reduced by entering the pulse-skipping mode (PSM) and the discontinuous conduction mode (DCM). In this operation, an internal compensation voltage V_{COMP} is compared by a PSM comparator, which has a programmable PSM threshold.

When the internal compensation voltage V_{COMP} is above the PSM threshold, the converter operates in normal fixed-frequency PWM mode. As soon as the V_{COMP} drops below the PSM threshold, the converter enters the pulse-skipping mode to reduce switching frequency and thus diminish switching losses. The PSM threshold also defines the minimum inductor peak current in PSM operation. Setting a higher PSM threshold will result in a higher minimum peak current which in turn result in a lower switching frequency at light load for better light load efficiency, albeit with increased output voltage ripple. Conversely, a lower PSM threshold results in lower peak current and lower PSM ripple at the cost of reduced light load efficiency.

16.3 Diode Emulation Mode

A Diode Emulation Mode (DEM) is also a necessary function to avoid delivering energy from converter output to converter input during dynamic output voltage control. The DEM function is equipped with two zero-current detection (ZCD) circuits for the low-side and high-side MOSFETs controlled by the LGATE1(internal) and UGATE2 pins. The source-to-drain voltage (V_{SDB}, detected via the PGND and SW1 pins) of the low-side MOSFET is compared with a zero-current threshold (V_{TH_ZCDB}). When the V_{SDB} drops below the V_{TH_ZCDB} voltage, the RTQ7892B-QT turns off the low-side MOSFET thereby avoiding reverse inductor current. In DEM operation, the behavior of the low-side MOSFET resembles a diode. The second ZCD circuit compares the source-to-drain voltage (V_{SDD}, detected via SW2 and ZCD pins) of the high-side MOSFET with a zero-current threshold (V_{TH_ZCDD}) to achieve the DEM function.

16.4 Cable Voltage Drop Compensation (CDC)

In a power delivery system with both a provider and a consumer, the provider with the RTQ7892B-QT AnyVolt feature can slightly adjust its CV output voltage to compensate voltage drop across the USB cable. A PD controller of the consumer can request a higher VBUS voltage from the provider through PD communication to achieve an accurate application voltage.

There is another method to implement the CDC function without PD communication. The RTQ7892B-QT can use the ADC to detect the output current-sense voltage (V_{CSO}) between CSOP and CSON pins and adaptively add a proper output voltage offset (V_{CDC}) to compensate for the cable voltage drop. The output voltage offset (V_{CDC}) is gradually added by adjusting the CV regulated output voltage (V_{REG_VO}) and is approximately proportional to the converter output current (I_{OUT}). V_{CDC} is approximately determined by the following equation:

$$V_{CDC} = I_{OUT} \times R_{CABLE}$$

where:

R_{CABLE} is a preset value of representing the parasitic resistance of USB cable.

16.5 VBUS Overvoltage Protection (VBUS OVP)

In Figure 1, the VBUS OVP function is a hardware-based protection which monitors the voltage at the VBUS pin via a built-in resistor-divider. When the VBUS voltage exceeds its OVP threshold, the output of the OVP comparator goes high and starts the debounce time counting. At the end of the debounce time counting, the signal VBUS OVP goes high to turn off the PWM controller. The OVP trip voltage is programmable from 3.3V to 24V (8-bit, 100mV/step typical) and its debounce time is also selectable to meet various application requirements.

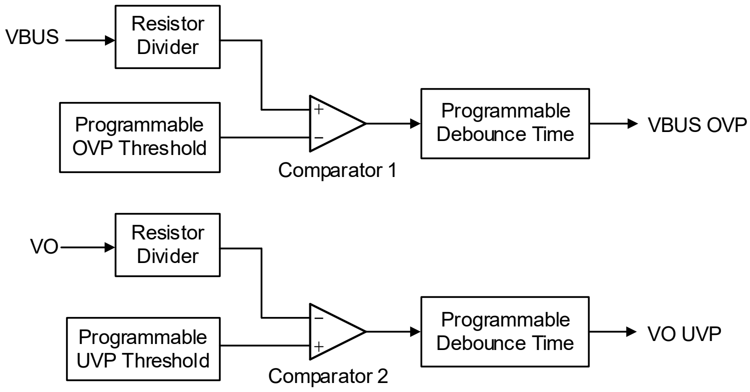


Figure 1. Functional Diagram of VBUS OVP and VO UVP

16.6 VO Undervoltage Protection (VO UVP)

In Figure 1, the VO UVP function is a hardware-based protection which monitors the voltage at the VO pin via a built-in resistor-divider. When the VO voltage falls below its UVP threshold, the output of the UVP comparator goes high and starts the debounce time counting. At end of the debounce time, the signal VO UVP goes high to turn off the PWM controller. The UVP trip voltage is programmable from 3V to 20V (8-bit, 100mV/step typical) and its debounce time is also selectable to avoid false triggering and to meet various application requirements.

16.7 AnyCurrent Constant-Current (CC) Regulation

It is noted that a robust system is very important in USB PD operations. The AnyCurrent CC regulation allows setting the most suitable CC level for a negotiated PD system.

The RTQ7892B-QT integrates a current-sense amplifier to sense output current for CC regulation and also through an ADC to the MCU for the output current to be recorded. The amplifier accurately senses the current-sense voltage (i.e., V_{CS} = output current x current-sense resistor) between the CSOP and CSON pins. The recommended current-sense voltage range for CC regulation is from 5mV to 35mV which is programmed by an internal 10-bit DAC (digital-to analog converter) with 0.0625mV/step resolution.

16.8 Power-Path Gate Driver for Driving N-Channel MOSFETs

The RTQ7892B-QT integrates a power-path gate driver to control external output blocking MOSFETs between the output of the PWM converter and the USB-C VBUS terminal. A built-in charge pump is included to supply the gate driver, enabling the external N-channel power MOSFETs, which allows for more cost-effective power systems compared to the counterpart, P-channel power MOSFETs.

16.9 Online Firmware Update via Slave I^{2}C or CC1/CC2 Interface

The embedded MTP memory allows the RTQ7892B-QT's firmware to be updated by an EC (Embedded Controller) or AP (Application Processor) through the I^{2}C slave interface. The RTQ7892B-QT provides some firmware-programmable design features, which greatly eases the design efforts during product development stage. Users are also allowed to update the firmware through CC1/CC2.

17 Application Information

(Note 6)

17.1 Calculating Output Discharge Time

Figure 2 shows the functional block diagram of two built-in output bleeders at VBUS and BLD pins. The VBUS bleeder consists of an internal resistor (1.2kΩ typical) and a pull-low MOSFET (Q_{BLD2}) for discharging the capacitors on the VBUS side; the BLD bleeder consists of an external resistor (R_{BLD_EXT}) and a pull-low MOSFET (Q_{BLD1}) for discharging the capacitors at the output of the PWM converter. If the blocking MOSFETs (Q1A and Q1B) are turned on during discharging, the BLD bleeder with larger current capability dominates the discharge time. If the blocking MOSFETs are turned off, the discharge time (t_{DIS_CVBUS}) of the capacitor connected to the VBUS pin can be calculated using the following equation:

$$t_{DIS\_CVBUS} = R_{BLD\_INT} \times C_{VBUS} \times \ln\left(\frac{V_{BUS\_INI}}{V_{BUS\_FINAL}}\right)$$

where:

- R_{BLD_INT} is the total internal resistance during on-state of the internal MOSFET Q_{BLD2}.
- C_{VBUS} is the total capacitance, coupled to the VBUS pin.
- V_{BUS_INI} is the initial bus voltage before discharging.
- V_{BUS_FINAL} is the final bus voltage at the end of discharging.

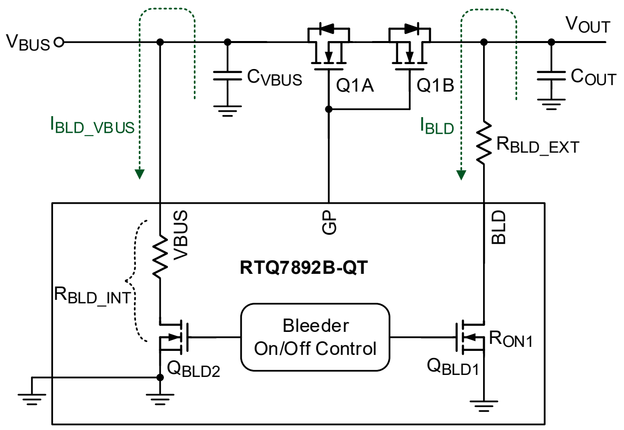


Figure 2. Functional Diagram of the Output Bleeders

Similar to the operation of the VBUS bleeder, the discharge time (t_{DIS_COUT}) of the capacitor connected to the output of the PWM converter is determined by the following equation:

$$t_{DIS\_COUT} = \left(R_{BLD\_EXT} + R_{ON1}\right) \times C_{OUT} \times \ln\left(\frac{V_{OUT\_INI}}{V_{OUT\_FINAL}}\right)$$

where:

- R_{BLD_EXT} is the resistance of the external resistor.
- R_{ON1} is the on-resistance of the internal MOSFET Q_{BLD1}.
- C_{OUT} is the total capacitance connected to the output of the PWM converter.
- V_{OUT_INI} is the initial voltage of the PWM converter output before discharging.
- V_{OUT_FINAL} is the final voltage of the PWM converter output at the end of discharging.

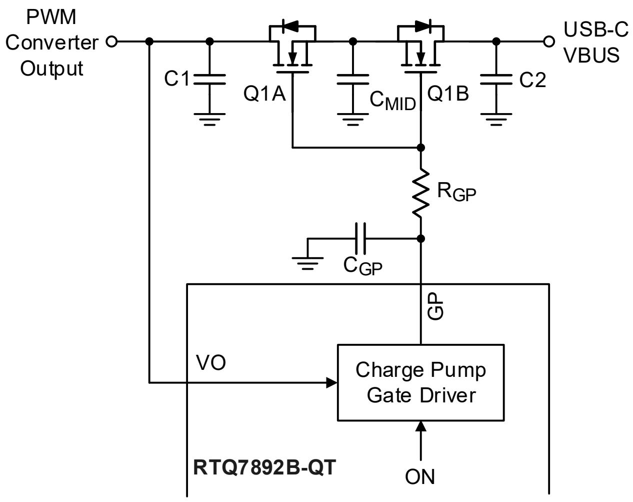


Figure 3. Functional Diagram of the Power-Path Control

17.2 Using Charge-Pump Gate Driver for Power-Path On/Off Control

Figure 3 shows the application schematic of a power-path on/off control. In this schematic, two N-channel MOSFETs with low on-resistance driven by a built-in gate driver, supplied by the charge pump, are employed to turn on or off the power-path between the PWM converter output and the USB-C VBUS terminal. If the internal control signal "ON" goes high, the GP voltage (V_{GP}) will be pulled high to turn on the power MOSFETs (Q1A and Q1B) and connect the power-path. If "ON" goes low, V_{GP} will be pulled low by a built-in MOSFET to disconnect the power-path.

Power input (VO) is needed for the charge pump, and the VO pin must be connected to the PWM converter output to ensure the power MOSFETs can be turned on successfully.

An optional MLCC capacitor (C_{GP}) can be used to reduce the V_{GP} rising rate and surge current in the power-path as the power MOSFETs being switched on. When the power MOSFETs are being switched off, the parasitic inductance and capacitance, C1 or C2, on the power path may cause voltage ringing at the drain of the Q1A or Q1B. An optional gate resistor (R_{GP}) can be added to reduce the falling rate of the power-path current and prevent voltage spikes. A 1μF MLCC capacitor (C_{MID}) between the source terminals and ground is necessary to prevent oscillation due to the dual-MOSFET connection.

17.3 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to- ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN7x7-62 package, the thermal resistance, θ_{JA}, is 38.37°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C − 25°C) / (38.37°C/W) = 3.26W for a WQFN7x7-62 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 4 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

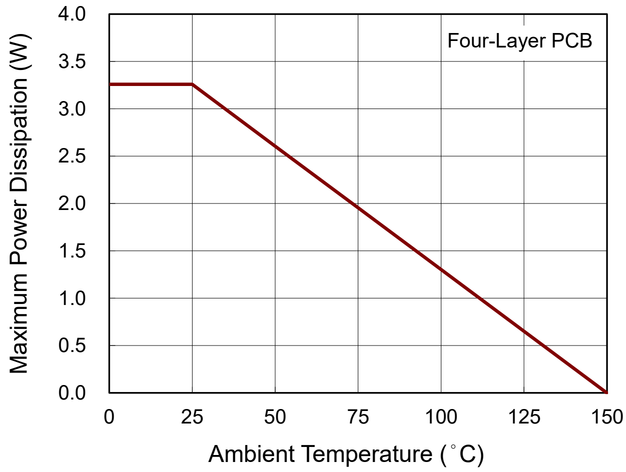


Figure 4. Derating Curve of Maximum Power Dissipation

17.4 Layout Considerations

- Connect the IC GND pin and the exposed pad to a ground plane (IC-ground), and then connect the IC-ground to the USB GND terminals via a low-impedance path. The exposed pad is also used to dissipate the heat into PCB.
- Connect the decoupling MLCCs near the pins of VDD, V2, PVDD and VBUS. Connect the MLCCs to the pins and IC-ground via low impedance paths.
- Connect the decoupling MLCC from the BOOT1/2 pin to the SW1/2 pin via a short and low-impedance path.
- Connect the SW2 and ZCD pins respectively to the source and the drain of high-side power MOSFET (controlled by UGATE2) via dedicated and low-impedance paths.
- Connect the capacitor (between the CSOP and CSON pins) close to these pins. The paths of CSOP and CSON must be directly connected to the terminals of current-sense resistor (R_{CSO}) using Kelvin connections as shown in the layout shown in Figure 5.

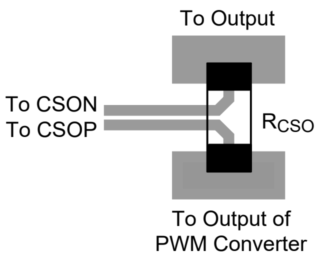


Figure 5. Kelvin Connections for the R_{CSO}

- Figure 6 is a recommended placement of the PWM buck-boost power-stage. Two critical loops "from C_{IN} → R_{CSI} → Q_A → IC internal Q_B to C_{IN}" and "from C_O → Q_D → IC internal Q_C to C_O" must be as short as possible to minimize the switching noise at PCIP/CSIP, PCIN, SW1, SW2 and ZCD pins. The shorter paths also help to reduce radiated EMI. It is necessary to use an MLCC (10μF/50V, X7R) for the input capacitor (C_{IN}) and output capacitor (C_O). For reducing the input and output voltage ripples during heavy load operation, it is recommended to add more MLCCs or solid input and output capacitors. Moreover, to improve heat dissipation, one needs to increase the PCB areas for drains of high-side and low-side MOSFETs.

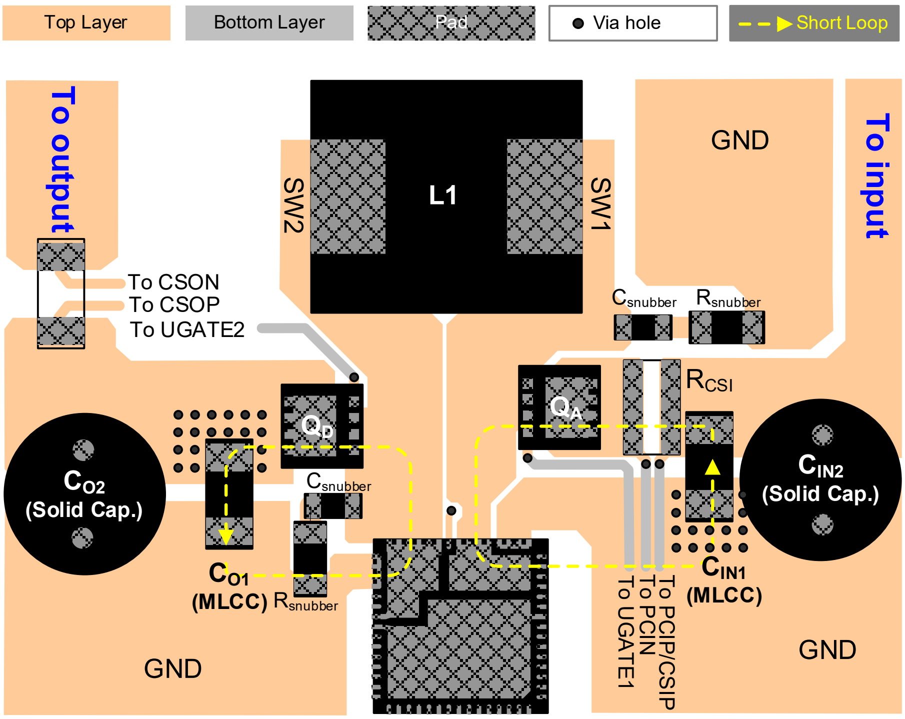


Figure 6. Recommended PCB Layout of the Power Stage

- To prevent the switching noises, separate the following signals from the switching nodes and the switching-current paths connected with SW1/SW2 pin:
  - Input and output current-sense signals
  - CC1 and CC2 signals
  - CV-loop feedback signal
- For improving ESD immunity, connect MLCCs close to the GND and VBUS terminals of the USB Type-C connector. Connect the capacitors to the USB VBUS and GND terminals through the low-impedance paths.

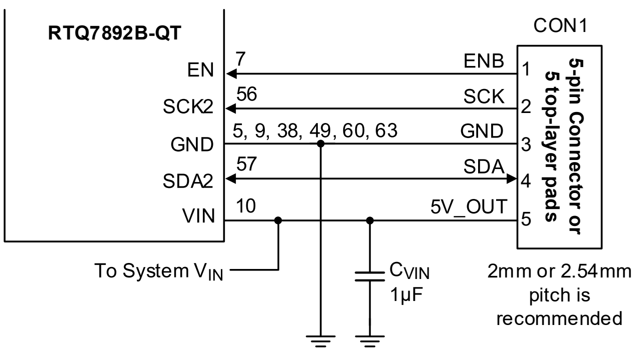


Figure 7. Connections for Manual Firmware Updates

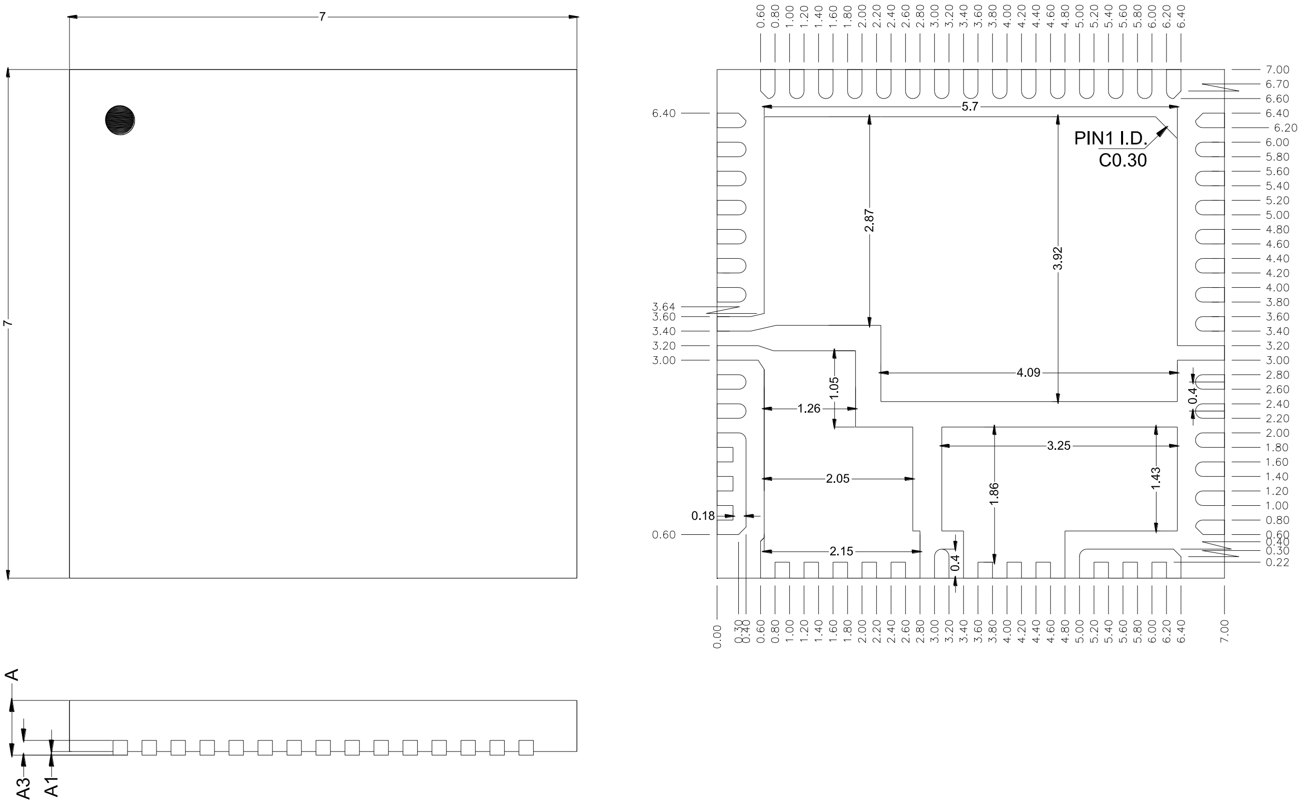
17.5 Manual Firmware Update

During the product development stage, users might need to download or update the RTQ7892B-QT firmware. This can be done by adding a 5-pin connector (CON1) or five test pads on PCBs for updating the RTQ7892B-QT firmware manually as shown in Figure 7. This connector is then connected to a “Firmware update fixture” by a 5-pin cable. The fixture is also connected to a PC via a micro USB cable and acts as a bridge between the RTQ7892B-QT and the PC. With this setup, users can download firmware to the RTQ7892B-QT by using the RTQ7892B-QT graphic user interface (GUI) installed in the PC. During the firmware update process, the fixture can supply current (up to 40mA) to the RTQ7892B-QT and the system V_{IN} via the 5V_OUT pin of the 5-pin cable.

If the power from the fixture is enough to power the RTQ7892B-QT and the system V_{IN}, it is not necessary to use the auxiliary input voltage for the system V_{IN}. On the other hand, if the system V_{IN} consumes more current than the fixture capability, an auxiliary input voltage is needed.

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension

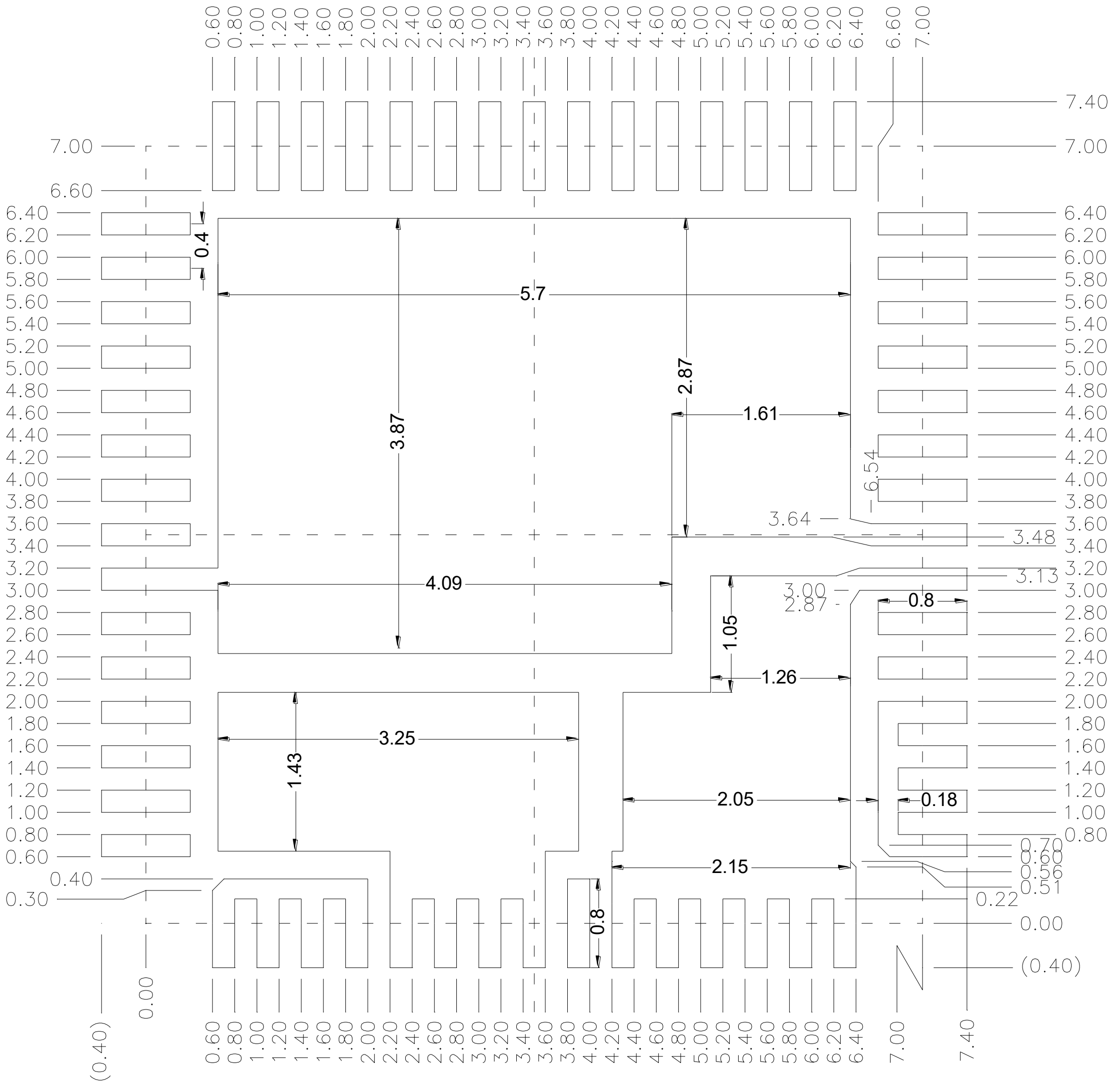


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050 mm

WQFN7x7-62 Package

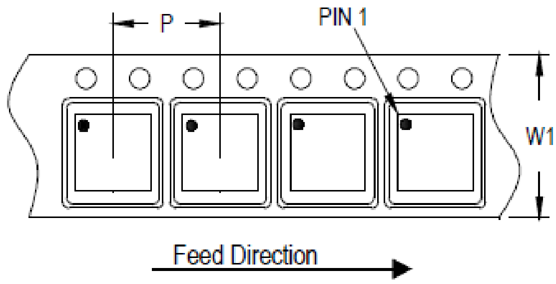
19 Footprint Information

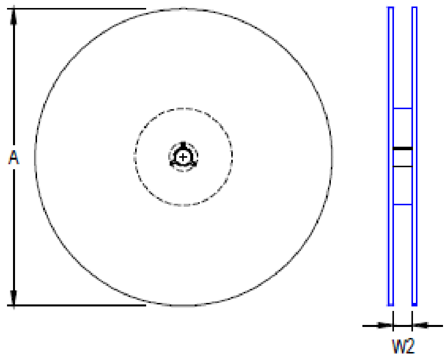


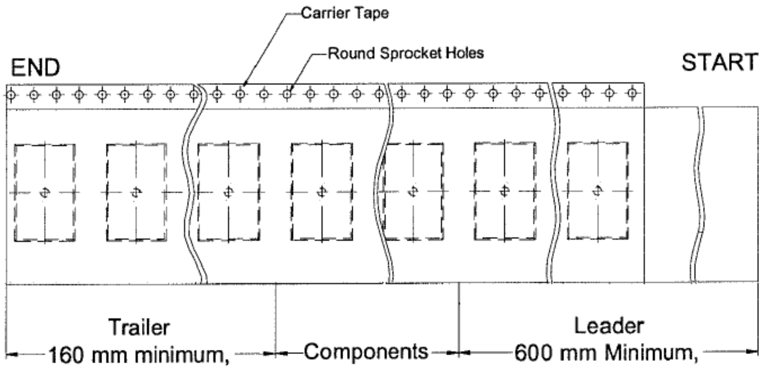
Package	Number of Pins	Tolerance
V/W/U/XQFN7x7-62	62	±0.05

20 Packing Information

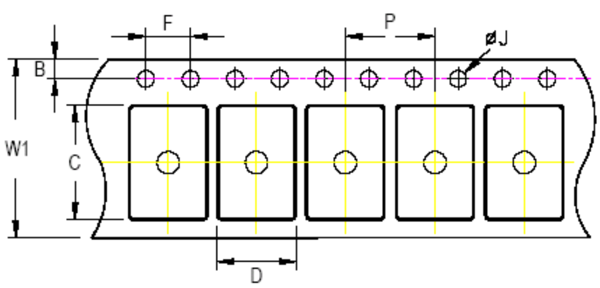
20.1 Tape and Reel Data

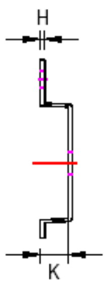






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 7x7	16	12	330	13	2,500	160	600	16.4/18.4





C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN and DFN 7x7	13”	2,500	Box G	1	2,500	Carton A	6	15,000

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation

14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

21 Datasheet Revision History

Version	Date	Description
00	2026/8/31	First Edition