Dual Rail 3+2-Phase PWM Controller with PMBus

General Description

The RTQ8825 is a dual output voltage rail 3+2-phase controller: a 3/2/1/0 phase synchronous buck controller, the rail A and a 2/1/0 phase synchronous buck controller, the rail B. The RTQ8825 adopts G-NAVP^{TM} (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to support all CPU/Microprocessor requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP^{TM} topology, the RTQ8825 features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and reduce output capacitors. The RTQ8825 supports VID on-the-fly function with four different slew rates via PMBus command setting. The DAC converts the VOUT_COMMAND code ranging from 0.25V to 1.516V with 1.953mV per step. The RTQ8825 integrates a high accuracy ADC for platform and function settings, such as SPS type, PMBus address, boot voltage and load-line. The RTQ8825 provides reset Vout function, Vout to be set to the VBOOT value while RESET# pin is asserted low. The RTQ8825 provides VR_Ready and thermal indicators. It also features complete fault protection functions including over-voltage (OV), under-voltage (UV), slow over-current (SLOW_OC), fast over-current (Fast_OC), over-temperature (OT) and under-voltage lockout (UVLO). The RTQ8825 more supports several functions which can be set by I2C/PMBus interface.

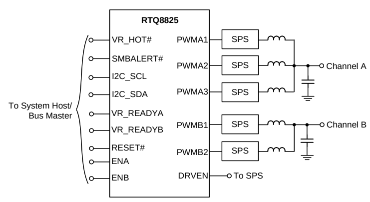
Applications

- Networking system
- Telecom, Datacom and Server system
- Point-of-load power supply (DSP, ASIC, FPGA)

Features

- **3/2/1/0 Phase (rail A) + 2/1/0 Phase (rail B) PWM Controller**
- **G-NAVP^{TM} (Green Native Adaptive Voltage Positioning) Topology**
- **Each Output Voltage Ranges 0.25V to 1.516V**
- **Embedded LDO for Dr.MOS 3.3V PWM Level**
- **Pin Programmable 27 VBOOT Voltages**
- **Current Sensing by Either Current Type or Voltage Type SPS**
- **Digital Current Balancing With Programmable Gain for Thermal Balancing**
- **Differential Output Voltage Sense for High Output Accuracy**
- **Supports Start-Up Into Pre-Bias Voltage**
- **Pin Selection for Enabling Load-Line Function**
- **Supports Returning to VBOOT from Existing Voltage or from 0V**
- **PMBus v1.3 Compliant Serial Interface**
  - **Pin Selectable 16 Addresses**
  - **1.8V and 3.3V Logic Level Compliant**
  - **SMBALERT#**
  - **Internal Non-Volatile Memory (NVM) to Store Custom Configurations**
  - **Programmable Power Up/Down Timing**
  - **Monitoring for V_{OUT}, I_{OUT} and Temperature**
  - **Selectable Latch or Autonomous Recovery After Shutdown Due to Fault**
  - **Extensive Fault Detection and Protection Capability**
  - **VIN & VCC Input Pins UVLO**
  - **Averaged Output SLOW/FAST_OC Protection**
  - **Output OV & UV Protection**
  - **Output Temperature Warning & Protection**
  - **Indicator for VR_Ready & VR_Hot#**
- **Small 48-Lead WQFN Package**

Simplified Application Circuit



Ordering Information

RTQ8825□□
- Package Type
  QW : WQFN-48L 7x7 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Richtek Green Policy Compliant

Note :

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Marking Information

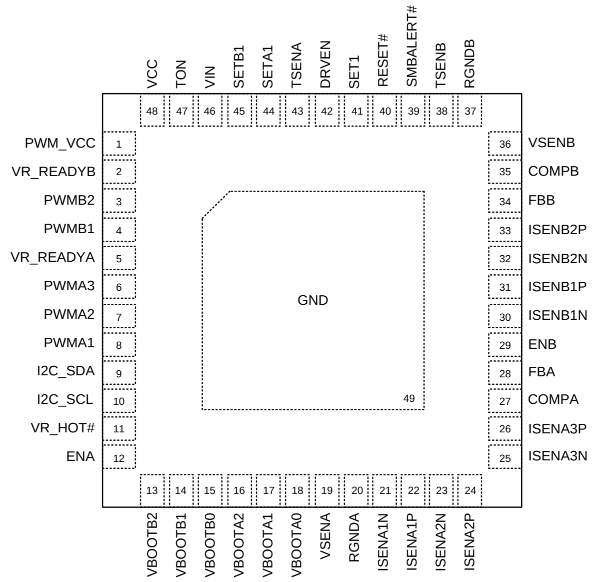
RTQ8825
GQW
YMDNN

RTQ8825GQW : Product Number

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-48L 7x7

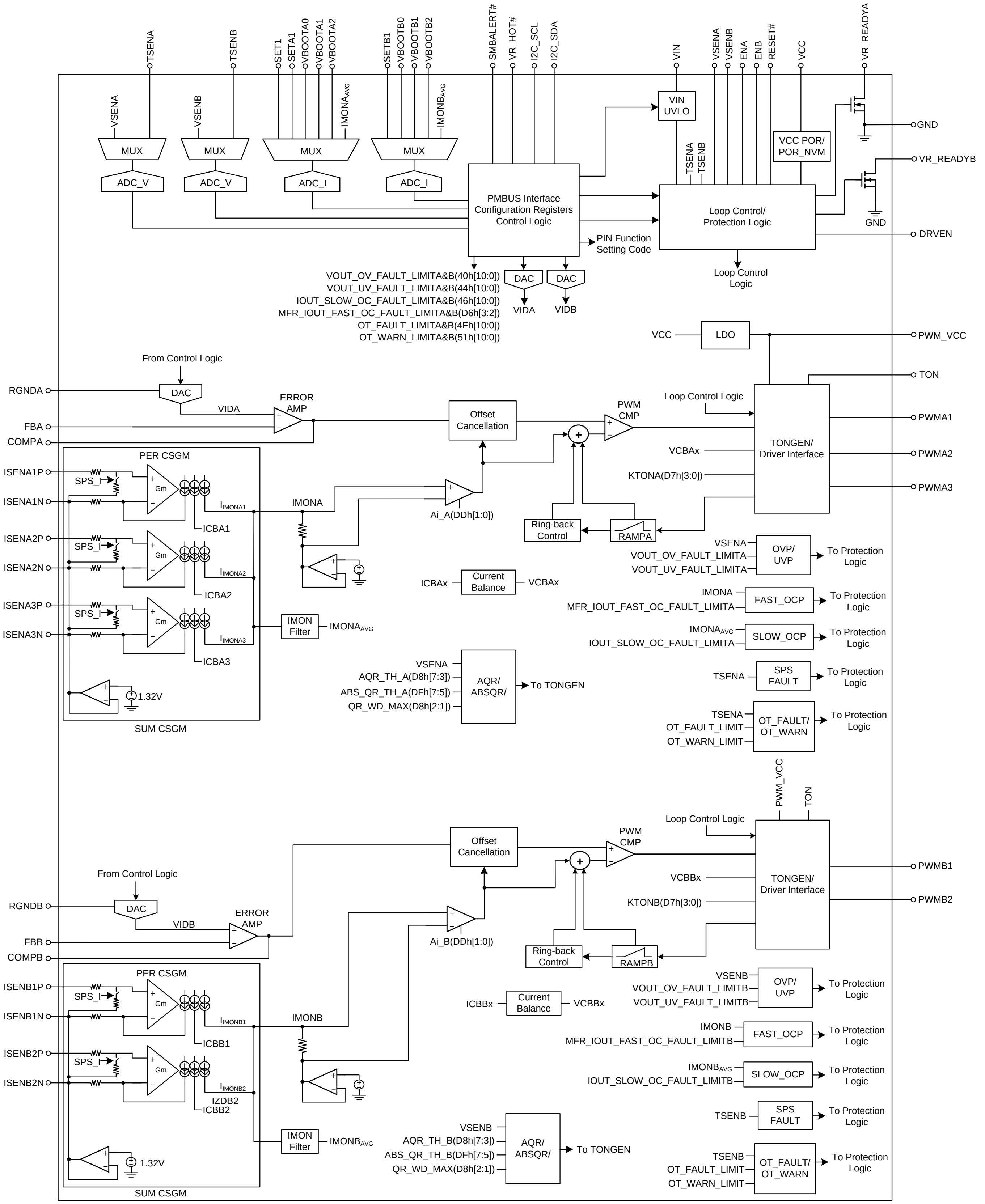
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PWM_VCC	Internally generated 3.3V. This pin is provided for attaching external decoupling capacitors only. Decouple using high quality 0.1μF/X7R + 4.7μF/X7R ceramic capacitors that minimum effective capacitance should be more than 1μF. It is suggested to place the capacitors as close to PWM_VCC pin as possible. This pin has limited source and sink capability and should not be used to drive external components.
2	VR_READYB	Voltage regulator "Ready" output signal for rail B. The VR_READYB indicator will be asserted when the controller reaches the VBoot voltage. This open-drain output requires an external pull-up resistor. VR_READYB will be pulled low when a shutdown fault occurs.
3	PWMB2	Phase #2 Rail B PWM output. This signal is used to drive the PWM input of the FET diver IC. Unused PWM pins should be left unconnected. The tri-state window = 1.1V to 2V.
4	PWMB1	Phase #1 Rail B PWM output. Refer to PWMB2 description.
5	VR_READYA	Voltage regulator "Ready" output signal for rail A. The VR_READYA indicator will be asserted when the controller reaches the VBoot voltage. This open-drain output requires an external pull-up resistor. VR_READYA will be pulled low when a shutdown fault occurs.
6	PWMA3	Phase #3 Rail A PWM output. Refer to PWMB2 description.
7	PWMA2	Phase #2 Rail A PWM output. Refer to PWMB2 description.
8	PWMA1	Phase #1 Rail A PWM output. Refer to PWMB2 description.
9	I2C_SDA	PMBus/I2C data signal.
10	I2C_SCL	PMBus/I2C clock signal.
11	VR_HOT#	Thermal warning flag. This open-drain output will be pulled low in the event of a sensed over temperature warning without disabling the regulators.
12	ENA	Active high output enable input of Rail A. Faults will be cleared when ENA is reasserted.
13	VBOOTB2	Tied the pin with resistor to ground to set boot voltage for rail B. 27 VBOOT voltage and VBOOT voltage range from 0.602V to 1.211V.
14	VBOOTB1	Refer to VBOOTB2 description.
15	VBOOTB0	Refer to VBOOTB2 description.
16	VBOOTA2	Tied the pin with resistor to ground to set boot voltage for rail A. 27 VBOOT voltage and VBOOT voltage range from 0.602V to 1.211V.
17	VBOOTA1	Refer to VBOOTA2 description.
18	VBOOTA0	Refer to VBOOTA2 description.
19	VSENA	Positive differential voltage sense input for rail A. Connect to positive remote sensing point.
20	RGNDA	Negative differential voltage sense input for rail A. Connect to negative remote sensing point.

Pin No.	Pin Name	Pin Function
21	ISENA1N	Phase #1 current sense inputs of Rail A. The ISENA1N and ISENA1P pins are used to differentially sense the corresponding channel current. Connect ISENA1P to VCC if rail A is not used.
22	ISENA1P	
23	ISENA2N	Phase #2 current sense inputs of Rail A. Refer to ISENA1P/N description.
24	ISENA2P	
25	ISENA3N	Phase #3 current sense inputs of Rail A. Refer to ISENA1P/N description.
26	ISENA3P	
27	COMPA	Error amplifier output of rail A.
28	FBA	Error amplifier voltage feedback of rail A.
29	ENB	Active high output enable input of rail B. Faults will be cleared when ENB is reasserted.
30	ISENB1N	Phase #1 current sense inputs of Rail B. The ISENB1N and ISENB1P pins are used to differentially sense the corresponding channel current. Connect ISENB1P to VCC if rail B is not used.
31	ISENB1P	
32	ISENB2N	Phase #2 current sense inputs of Rail B. Refer to ISENB1P/N description.
33	ISENB2P	
34	FBB	Error amplifier voltage feedback of rail B.
35	COMPB	Error amplifier output of rail B.
36	VSENB	Positive differential voltage sense input for rail B. Connect to positive remote sensing point.
37	RGNDB	Negative differential voltage sense input for rail A. Connect to negative remote sensing point.
38	TSENB	Input pin for external temperature measurement at rail B.
39	SMBALERT#	SMB_ALERT# output. Active low.
40	RESET#	Return to VBoot input pin. When asserted (active low), Vout to be set to the VBoot value for both rail A and rail B.
41	SET1	Used with SETA1 pin via resistor tied to ground to sets PMBus address, SPS type of rail A and enabling load-line function of rail A.
42	DRVEN	External driver mode control. Must connect this pin directly to EN pin of smart power stage (SPS).
43	TSENA	Input pin for external temperature measurement at rail A.
44	SETA1	Refer to SET1 description.
45	SETB1	A resistor tied to ground sets both the SPS type of rail B and enabling load-line function of rail B.
46	VIN	VIN (+12V) voltage divider input. The VIN pin must be connected to +12V supply through a resistor divider and is used to guarantee a valid input voltage before starting up (input under-voltage lockout).
47	TON	Input voltage sense pin. Connect a low pass filter which time constant is at the switching frequency to this pin for setting on-time.

Pin No.	Pin Name	Pin Function
48	VCC	5V power supply input to controller. This pin should be connected to the system +5V supply and decoupled using high quality 1.0μF ceramic capacitors.
49 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND with enough via numbers for maximum power dissipation.

Functional Block Diagram



Operation

G-NAVP™ Control Mode

The RTQ8825 adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When sensed current signal reaches sensed voltage signal, RTQ8825 generates a PWM pulse to achieve loop modulation. Figure 1 left part shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage, that is inverted and amplified signal of output voltage. While current loading is increasing, referring to Figure 1 right part, COMP rises due to output voltage droop. Then rising COMP forces PWM turn on earlier and closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage and corresponding output voltage is in the steady state of lower voltage. The load-line, output voltage drooping by an amount proportional to loading current, is achieved.

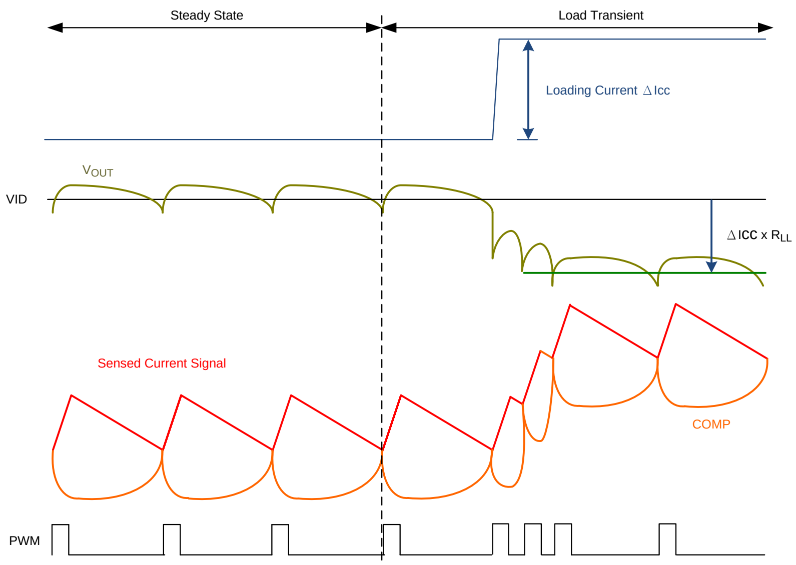


Figure 1. G-NAVP™ Behavior Waveform

POR/POR_NVM

NVM loading of the RTQ8825 begins after VCC crosses its rising VCC_POR_NVM threshold. When POR_NVM conditions are met, RTQ8825 will loading NVM into the control registers.

Initialization of the RTQ8825 begins after VCC crosses its rising VCC_POR threshold. When POR conditions are met, the internal 3.3V LDO is enabled and begins pin setting indicated by the SET pin resistor value.

PMBus Interface/Control Logic/Configuration Registers

The PMBus Interface receives or transmits signal with system host/bus master. Control logic executes command (Read/Write registers) and sends related signals to control VR. Configuration registers include function setting registers and PMBus basic required registers.

IMON Filter

The IMON Filter is used to average current signal by analog low-pass filter. It outputs $IMONA_{AVG}$ and $IMONB_{AVG}$ to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs of SET1, SETA1, SETB1, VBOOTA, VBOOTB, TSENA, TSENB, VSENA, VSENB, $IMONA_{AVG}$ and $IMONB_{AVG}$. The ADC converts these analog signals to digital codes for reporting or function settings.

UVLO

The RTQ8825 provide the input under-voltage lockout (UVLO) with VIN and VCC pins. When the VIN falls below VIN_OFF(36h) or the VCC falls below VCC_POR threshold, the UVLO fault is asserted. The device will stop power conversion to make sure the device works properly. For more information, see Application Information and Table 4.

Loop Control/Protection Logic

It controls power-on/off sequence, protections and PWM sequence.

DAC

Generates a reference VID voltage according to the VID code sent by Control Logic. According to VOUT_COMMAND command, Control Logic dynamically changes VID voltage to the target with required slew rate.

ERROR AMP

Inverts and amplifies the difference between output voltage and VID with externally setting finite DC gain. The output signal is COMP for PWM triggers.

PER CSGM

Senses per-phase inductor current. The outputs are used for loop response, Current Balance, current reporting and over-current protection.

SUM CSGM

Senses total inductor current with RIMON gain adjustment. SUM CSGM output is used for PWM trigger.

RAMP

RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal and sum current signal based on RAMP to trigger PWM.

Offset Cancellation

Cancel the current signal/comp voltage ripple issue to control output voltage accuracy.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

AQR/ABS_QR

AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWM to turn on. PWM pulse width triggered by AQR is adaptive to loading level. Absolutely Quick Response (ABS_QR) is used in the no load-line system which detects the absolute value of output voltage drop. The RTQ8825 also provides various ABS_QR threshold via MFR_ABS_QR (DFh) register and AQR threshold via MFR_AQR (D8h) register.

TONGEN/Driver Interface

PWM comparator output signal triggers TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. PWM pulse width is determined by frequency setting, current balance output, Adaptive Quick Response (AQR) and ABS-QR settings. Once AQR is triggered, VR allows all PWM to turn on at the same time. Driver interface provides high/low/tri-state to drive external driver. In addition, PWM state is controlled by protection logic. Different protections force required PWM state.

OVP/UVP/SLOW_OCP/FAST_OCP/OTP/VIN_UVLO/SPS_FAULT

Over-voltage protection/Under-voltage protection / Slow over-current protection / Fast over-current protection / Over-temperature protection / Input Voltage under-voltage lockout/Smart Power Stage device fault protection.

Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- –0.3V to 6.5V
- TON to GND ---------- –0.3V to 28V
- PWM_VCC to GND ---------- –0.3V to 6.5V
- VCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- VR Supply Voltage to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4)

- WQFN-48L 7x7, θ_{JA} ---------- 26.5°C/W
- WQFN-48L 7x7, $\theta_{JC(Top)}$ ---------- 10.3°C/W

Electrical Characteristics

(V_{CC} = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from –40°C to 125°C, unless other noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}		4.5	--	5.5	V
Controller Supply Current	I_{VCC}	VCC = 5V Both EN = L, no switching	8	11.5	15	mA
VCC Power-ON Reset (POR)	$V_{CC\_POR\_R}$	Rising edge	4.2	4.3	4.4	V
	$\Delta V_{CC\_POR\_F\_HYS}$	Falling edge hysteresis	150	190	230	mV
VCC Power-ON Reset for NVM (POR_NVM)	$V_{CC\_POR\_NVM\_R}$	Rising edge	--	3.2	3.6	V
	$V_{CC\_POR\_NVM\_F}$	Falling edge	2.6	2.8	--	
VIN						
Sensing Power Stage Input Voltage Divider Range	V_{IN}		1.1	--	3	V
TON						
Sensing Power Stage Input Voltage Range	V_{TON}		4.5	--	17	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN							
VR Enable Threshold	Logic-High	V_{IH_EN}		0.7	--	--	V
VR Disable Threshold	Logic-Low	V_{IL_EN}		--	--	0.6	V
Leakage Current of EN		I_{LEAK_EN}		–1	--	1	μA
SETx, VBOOTx							
Current Source from SETx pins and VBOOTx pins		I_{SET}	V(SET) = 1.6V	77	80	83	μA
I2C_SCL, I2C_SDA I/O							
I2C_SCL/I2C_SDA Threshold	Logic-High	V_{IH_I2C}		1	--	--	V
	Logic-Low	V_{IL_I2C}		--	--	0.6	V
Leakage Current of I2C_SCL/I2C_SDA		I_{LEAK_I2C}	I2C_SCL/SDA = H	–1	--	1	μA
Active Low Voltage of I2C_SDA		V_{I2C_SDA}	I_{I2C_SDA} = 10mA	0.04	--	0.13	V
PMBus Interface Timing Characteristics							
SCL Clock Rate		f_{SCL}		10	--	1000	kHz
Hold Time (Repeated) Start Condition.		$t_{HD;STA}$		0.26	--	--	μs
Low Period of the SCL Clock		t_{LOW}		0.5	--	--	μs
High Period of the SCL Clock		t_{HIGH}		0.6	--	50	μs
Set-Up Time for a Repeated START Condition		$t_{SU;STA}$		0.26	--	--	μs
Data Hold Time		$t_{HD;DAT}$		0	--	--	ns
Data Set-Up Time		$t_{SU;DAT}$		50	--	--	ns
Set-Up Time for STOP Condition		$t_{SU;STO}$		0.26	--	--	μs
Bus Free Time Between STOP and START Condition		t_{BUF}		0.5	--	--	μs
I2C_SCL/I2C_SDA Rise Time		t_R		--	--	120	ns
I2C_SCL/I2C_SDA Fall Time		t_F		--	--	120	ns
RESET#							
RESET# Threshold	Logic-High	V_{IH_RESET}		0.8	--	--	V
	Logic-Low	V_{IL_RESET}		--	--	0.4	V
TSENx							
Input Voltage Range				0	--	2	V
ISENxN							
Common Mode Voltage Range		V_{ISENxN}		1.19	1.32	1.45	V
Current Sensing Amplifier							
Impedance at Positive Input		R_{ISENxP}	I-type SPS	1	--	--	MΩ
		R_{ISENxP}	V-type SPS	4.25	5	5.75	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sense Input Voltage	$V_{CSIN\_V\text{-}type\ SPS}$	Differential voltage range of current sense input. (VCSIN = ISENxP - ISENxN)	–40	--	400	mV
	$V_{CSIN\_I\text{-}type\ SPS}$	Differential voltage range of current sense input. (VCSIN = ISENxP - ISENxN)	–10	--	100	
Current Sense Gain Error	A_{MIRROR}	Internal current mirror gain of per phase current sense. (AMIRROR = IMONx / ICS,PERx)	0.95	1	1.05	A/A
PWM Output						
PWM_VCC	V_{PWM_VCC}		3	3.3	3.6	V
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
VR_READYx						
Output Voltage Low of VR_READY	$V_{OL\_VR\_READY}$	I_{VR_READY} = 10mA	--	0.13	0.2	V
SMBALERT#, VR_HOT#						
Output Voltage Low of SMBALERT#/VR_HOT#	$V_{OL\_SMBALERT\#}$ $V_{OL\_VR\_HOT\#}$	$I_{SMBALERT\#}$ = 10mA $I_{VR\_HOT\#}$ = 10mA	--	--	0.13	V
Leakage Current of SMBALERT#/VR_HOT#	$I_{LEAK\_SMBALERT\#}$ $I_{LEAK\_VR\_HOT\#}$	SMBALERT# = H VR_HOT# = H	–1	--	1	μA
TON Setting						
ON-Time Setting	T_{ON}	V_{IN} = 12V, VID = 1V, freq. = 410kHz, k_{TON} = 1	--	208	--	ns
DAC Voltage Characteristics						
DAC Voltage Range	DAC		0.25	--	1.516	V
DAC Voltage Accuracy	$DAC_{(acc)}$	VID = 1.516V, 1.2V, 1V, 0.746V；T_J from –10°C to 125°C	–1	--	1	%
		VID = 1.516V, 1.2V, 1V, 0.746V；T_J from –40°C to 125°C	–1.3	--	1.3	
Telemetry for VOUT/IOUT/Temperature						
Output Voltage Measurement	M_{VOUT}	Range by VID Setting	0	--	1.516	V
	$M_{VOUT(acc)}$	Accuracy	–10	--	10	LSB
	$M_{VOUT(lsb)}$	Bit Resolution	--	1.953	--	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Current Measurement		M_{IOUT}	Range	0	--	416	A
		$M_{IOUT(acc)}$	Accuracy, $I_{OUT} \leq 120A$	–4.5	--	4.5	LSB
			Accuracy, $I_{OUT} > 120A$	–5	--	5	%
		$M_{IOUT(lsb)}$	Bit Resolution	--	1	--	A
Temperature Measurement		M_{temp}	Range	–75	--	175	°C
		$M_{temp(acc)}$	Accuracy	–4	--	4	
		$M_{temp(lsb)}$	Bit Resolution	--	1	--	
Protections							
Sensing Input Voltage Divider Under-Voltage Lockout (UVLO)	VIN_ON	V_{IN_ON}	Programmable range, 10 different settings	1.2	--	3	V
		$V_{IN\_ON(acc)}$	Accuracy	–1.5	--	1.5	%
	VIN_OFF	V_{IN_OFF}	Programmable range, 10 different settings	1.1	--	2.9	V
		$V_{IN\_OFF(acc)}$	Accuracy	–1.5	--	1.5	%
OVP Threshold Accuracy		$V_{OV(acc)}$	VID ≥ 1V	–1.5	--	1.5	%
			VID < 1V	–15	--	15	mV
Debounce Time of All OVP		D_{T_OVP}		--	0.5	--	μs
UVP Threshold Accuracy		$V_{UV(acc)}$	VID ≥ 1V	–1.5	--	1.5	%
			VID < 1V	–25	--	25	mV
Debounce Time of UVP		D_{T_UVP}		--	3	--	μs
Slow OCP Threshold Accuracy		$I_{SLOW\_OC(acc)}$		–3.5	--	3.5	%
Fast OCP Threshold Accuracy		$I_{FAST\_OC(acc)}$	(Note 5)	–5	--	5	%
OT_FAULT Threshold Accuracy		$T_{OT\_FAULT(acc)}$		–4	--	4	°C
OT_WARNING Threshold Accuracy		$T_{OT\_WARN(acc)}$		–4	--	4	°C
SPS FAULT Threshold		V_{SPS_FAULT}	Driver Fault Comp. Threshold	2	2.2	2.24	V

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

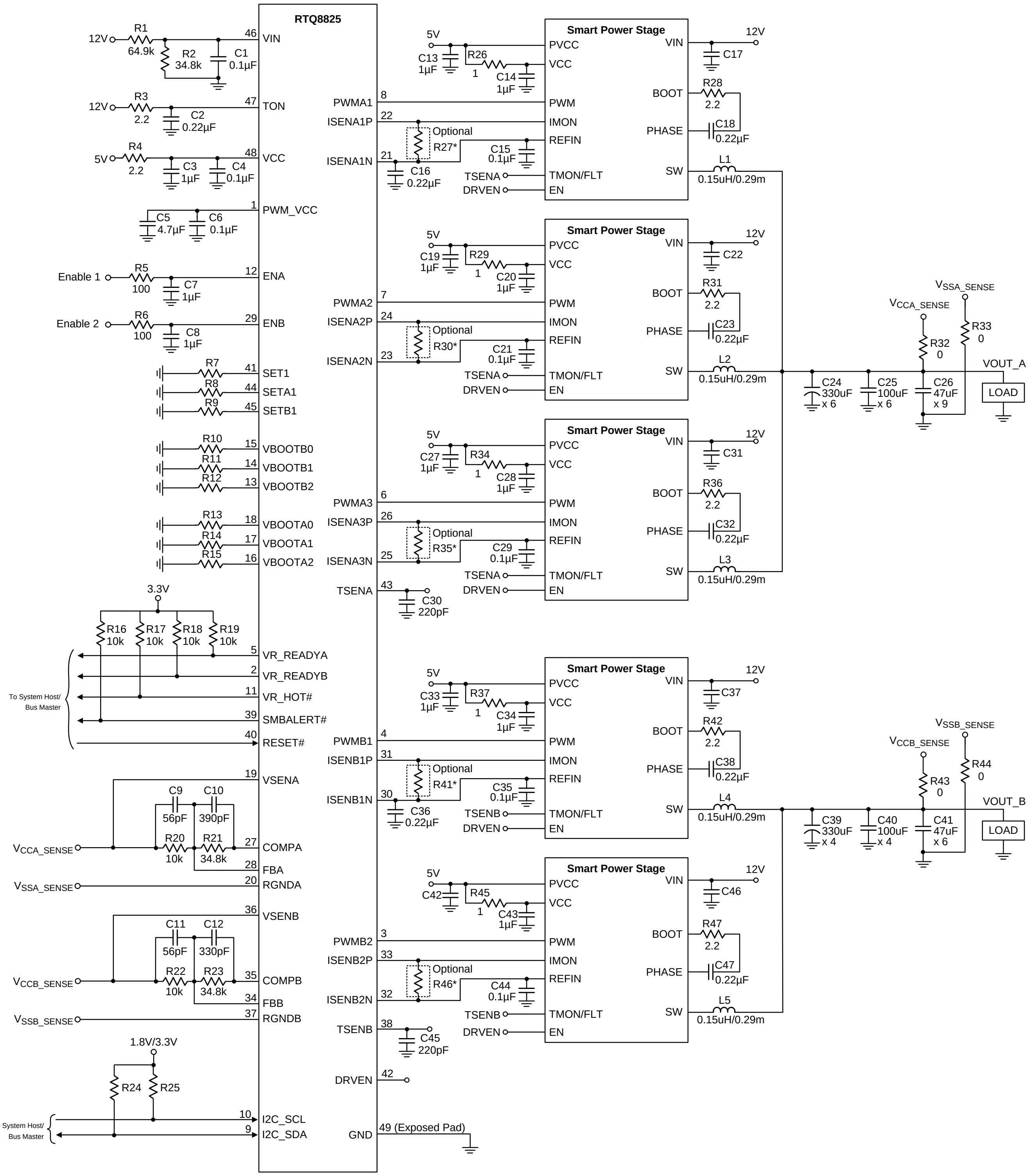
Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. Not subject to production test - verified by design and/or characterization.

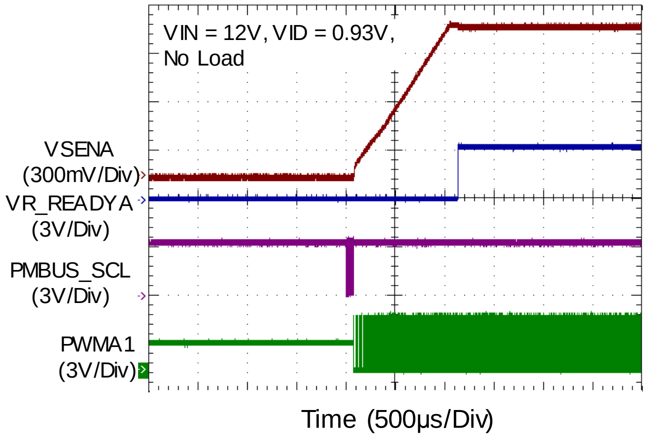
Typical Application Circuit



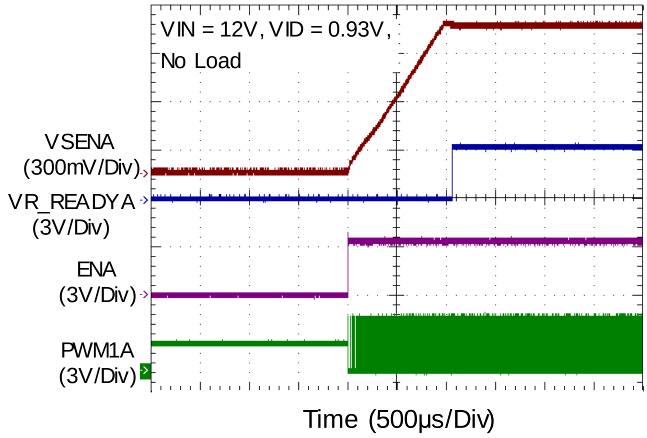
* An optional resistor for I-type SPS that suggestion is 249Ω

Typical Operating Characteristics

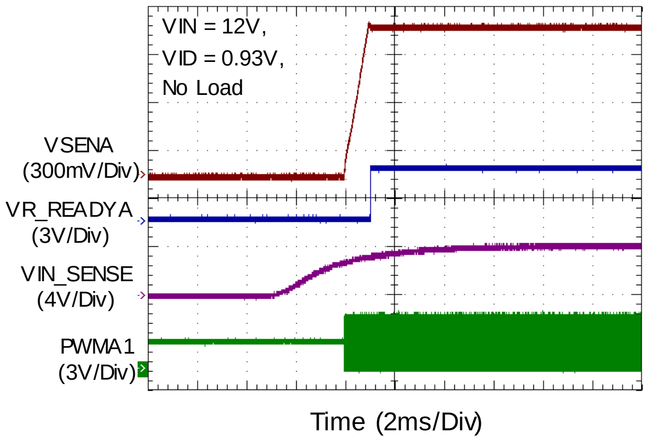
Power On from PMBUS



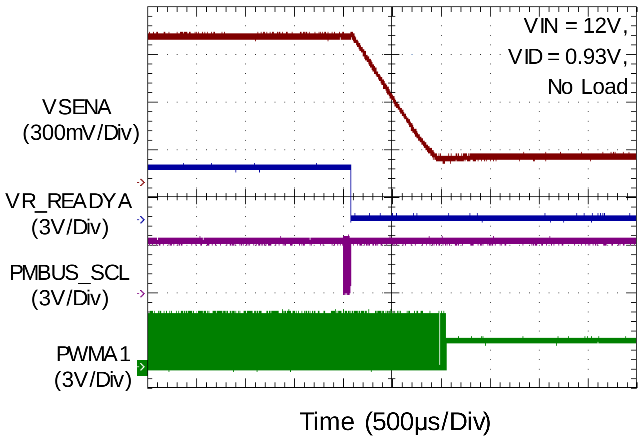
Power On from EN



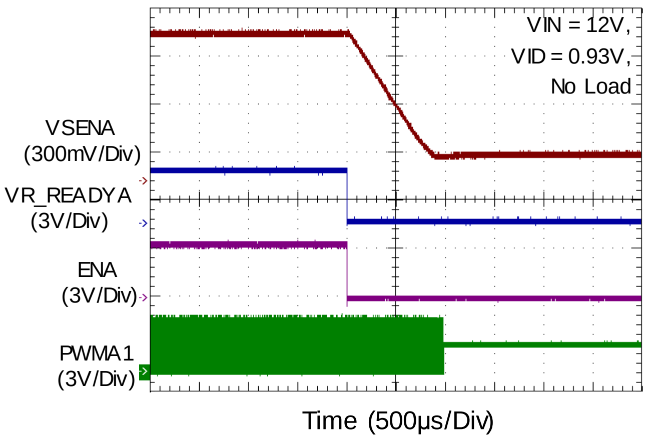
Power On from VIN



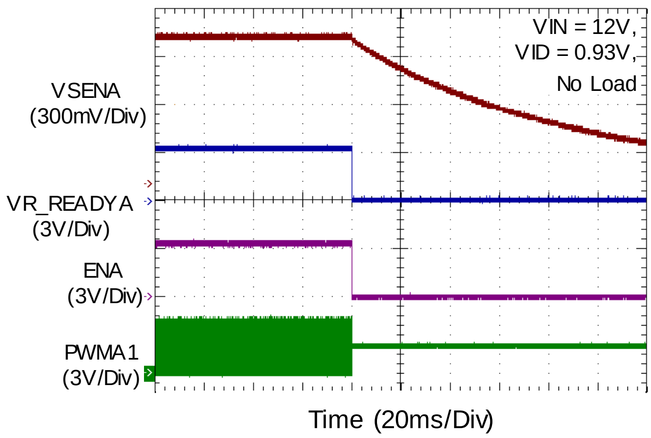
Power Off from PMBUS



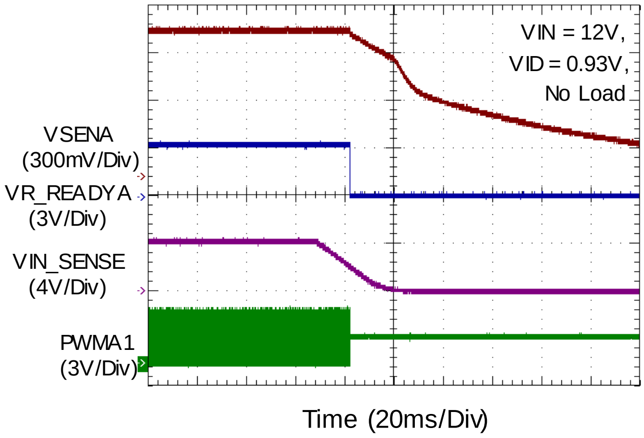
Power Off from EN (Soft Off)



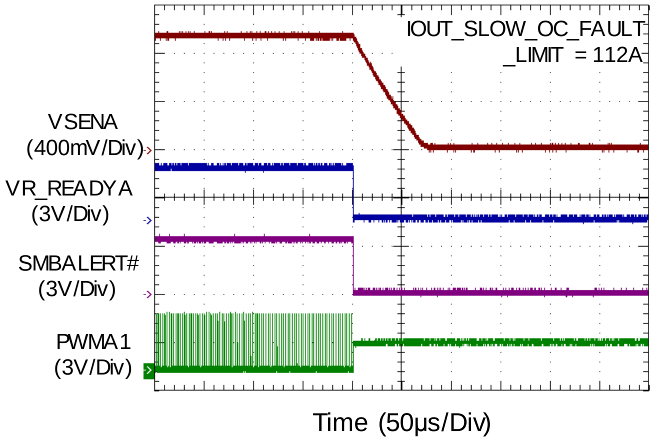
Power Off from EN (Immediately Off)



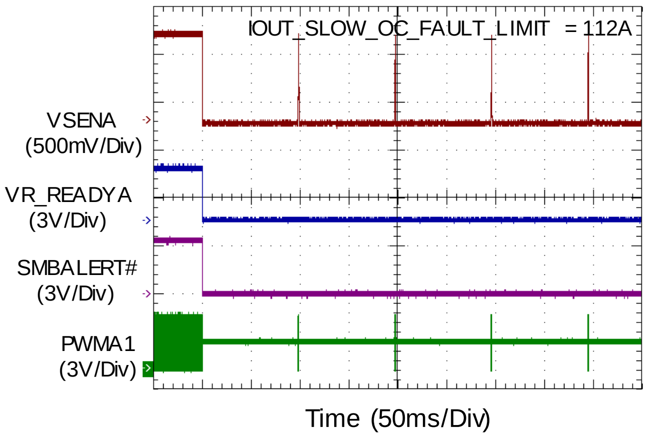
Power Off from VIN



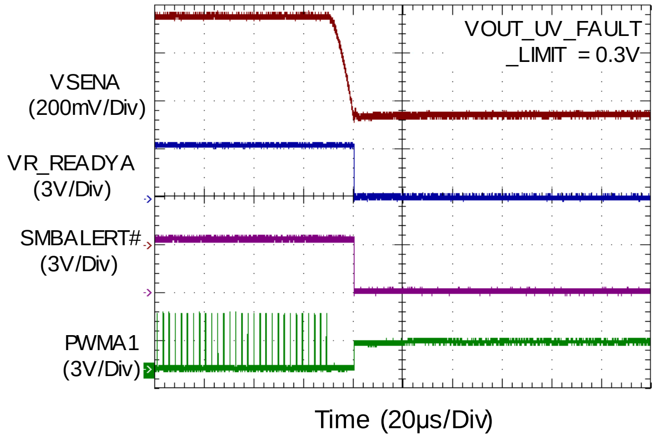
VR OCP (Latched Shutdown)



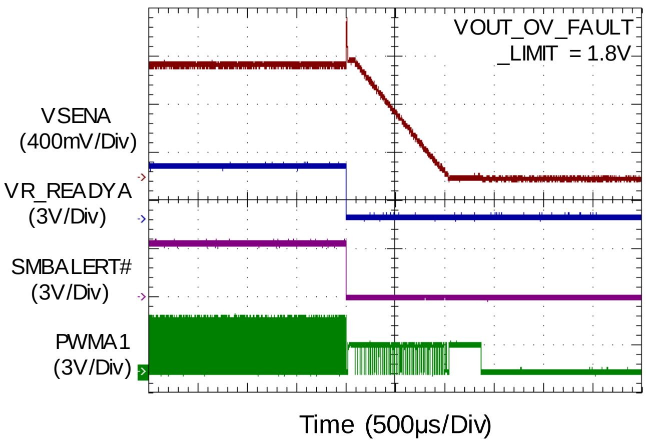
VR OCP (Hiccup Mode)



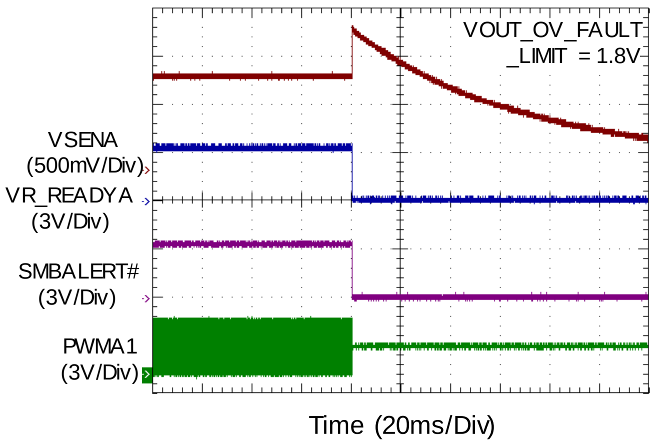
VR UVP



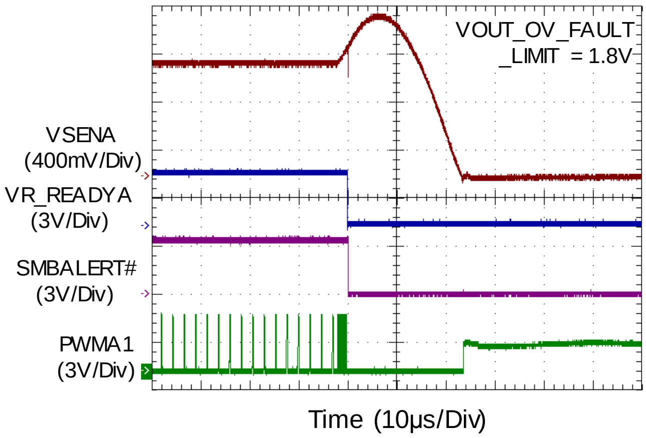
VR OVP (Soft Shutdown)



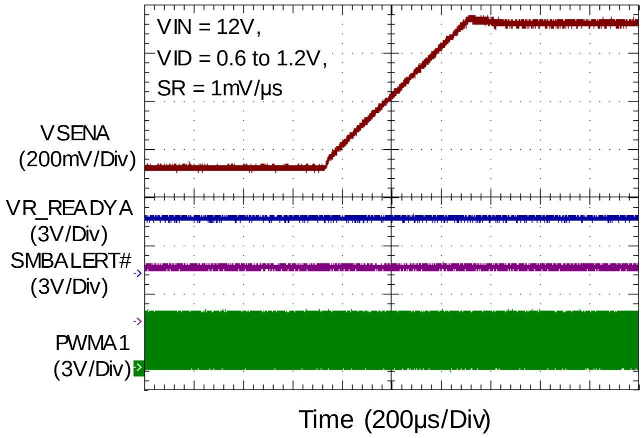
VR OVP (HiZ Shutdown)



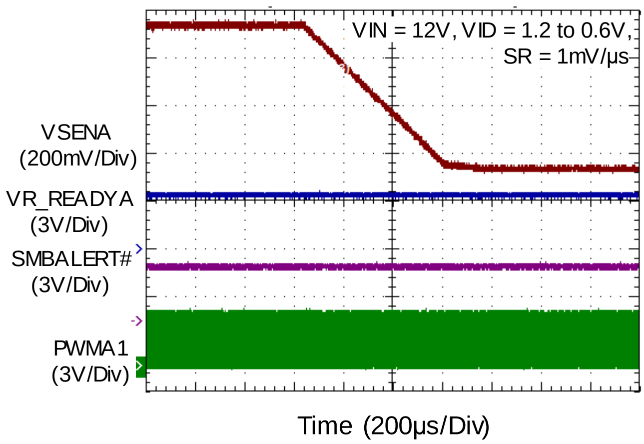
VR OVP (Turn On Low-Side MOSFET)



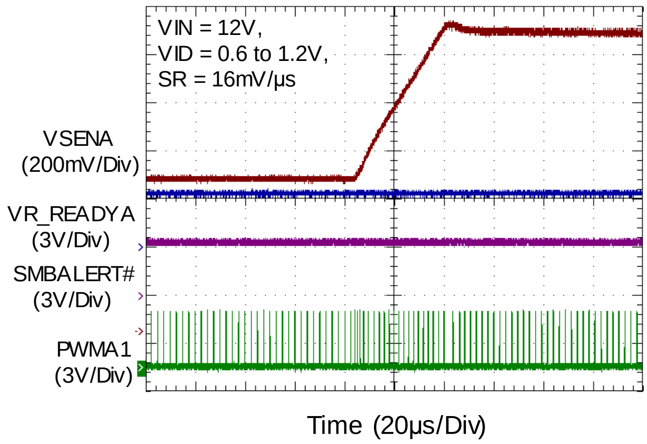
Dynamic-VID Up with Slow SR (1mV/μs)



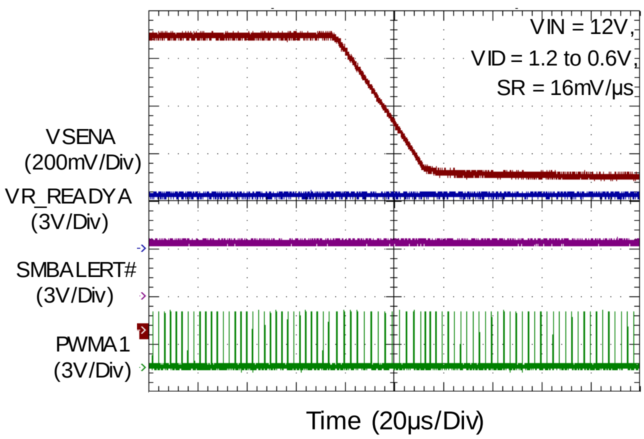
Dynamic-VID Down with Slow SR (1mV/μs)



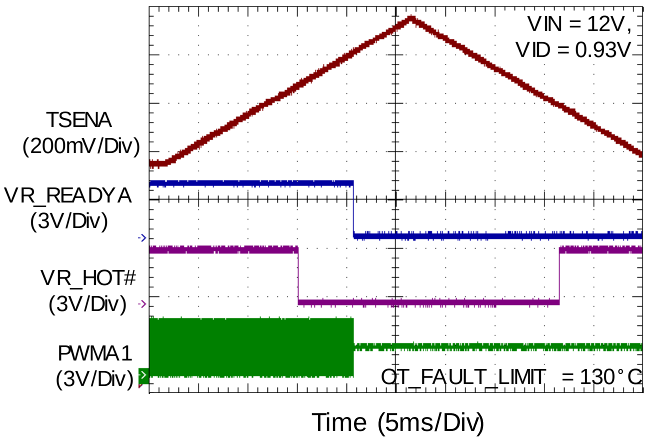
Dynamic-VID Up with Fast SR (16mV/μs)



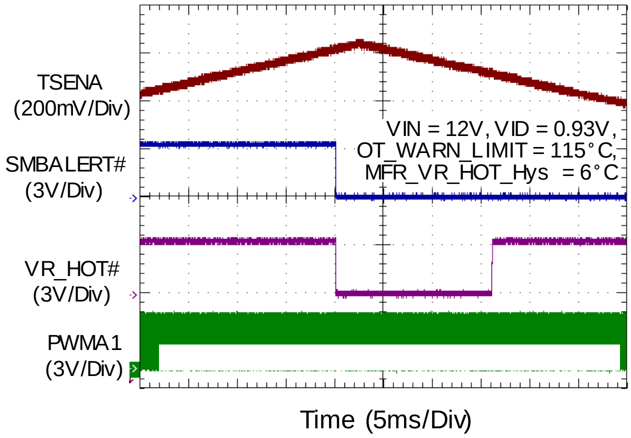
Dynamic-VID Down with Fast SR (16mV/μs)



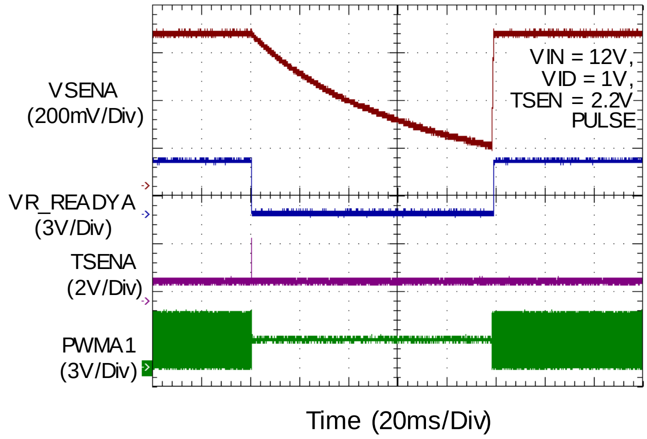
VR OTP



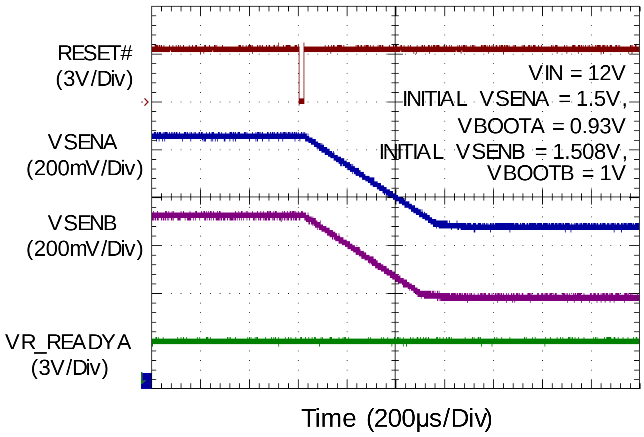
VR Thermal Warning



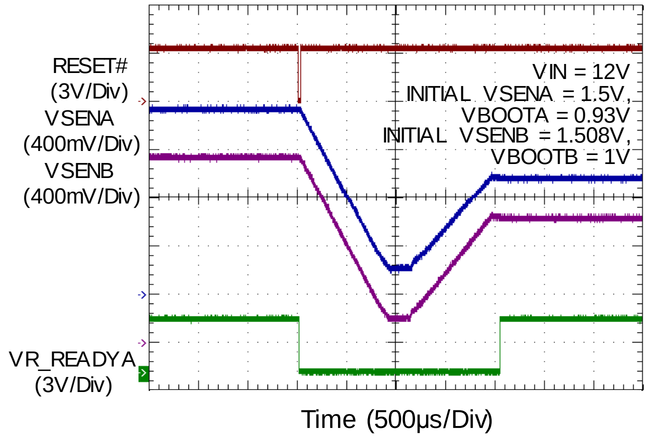
SPS Fault



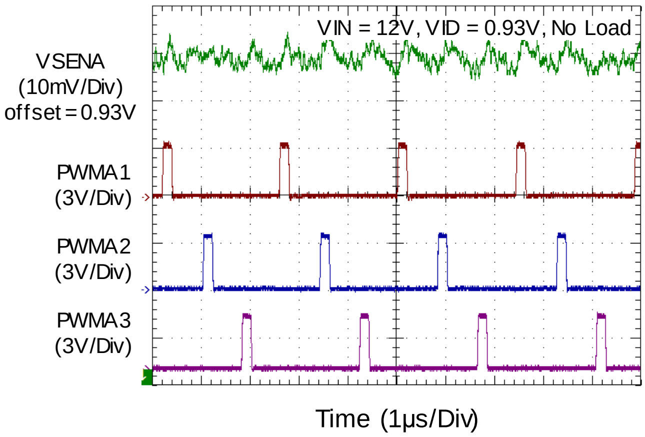
RESET# Function (Return to VBOOT)



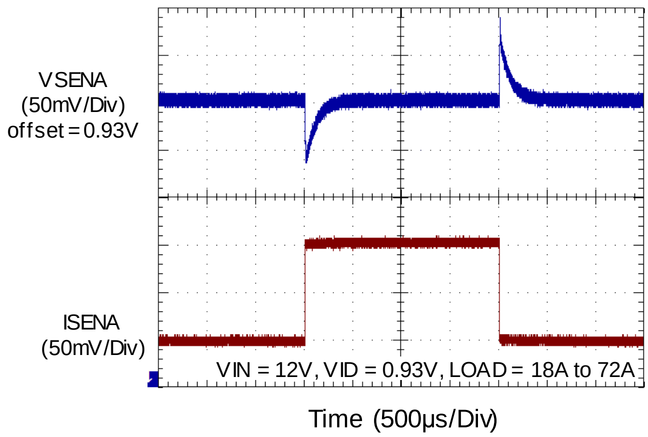
RESET# Function (Restart)



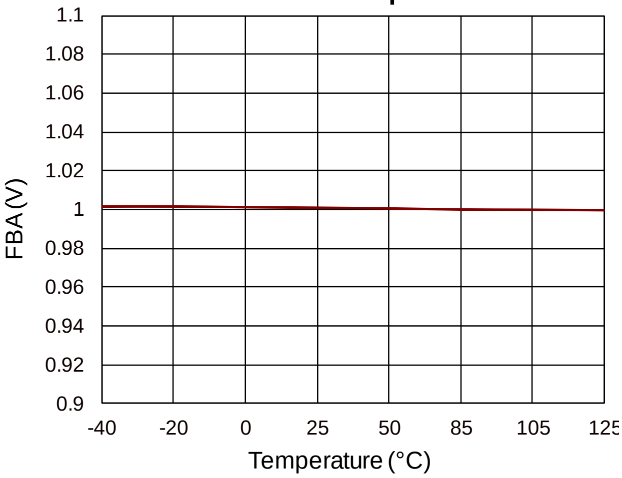
Output Ripple



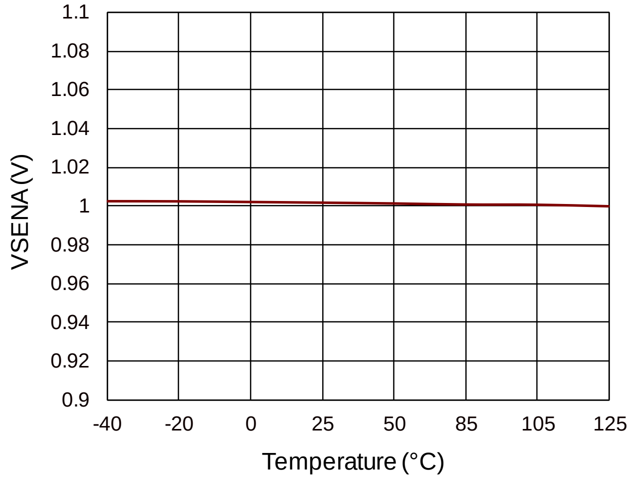
Transient Response



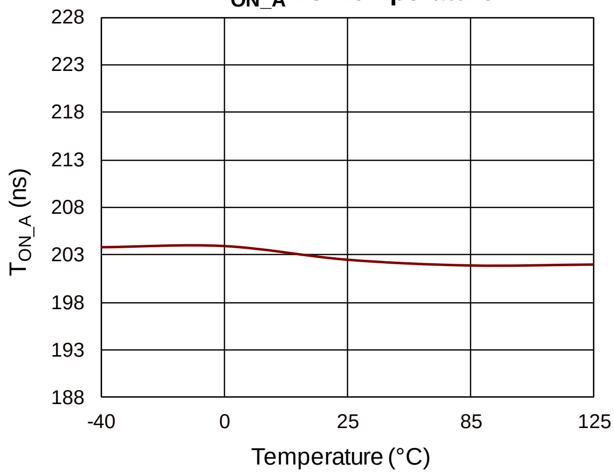
FBA vs. Temperature



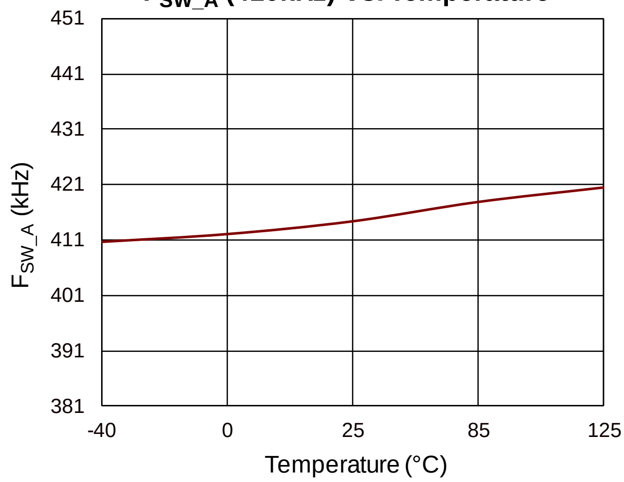
VSENA vs. Temperature



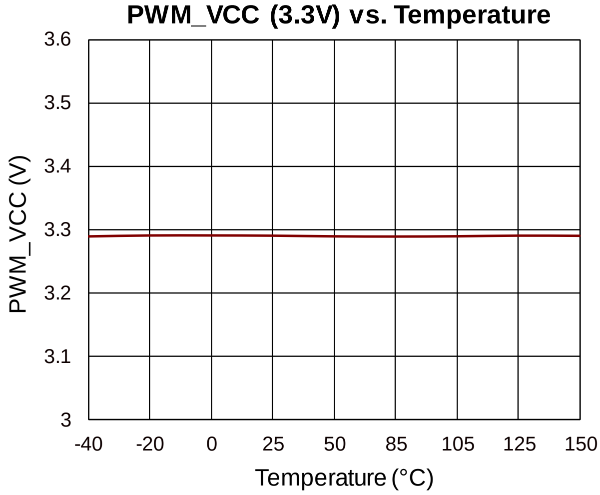
T_{ON_A} vs. Temperature



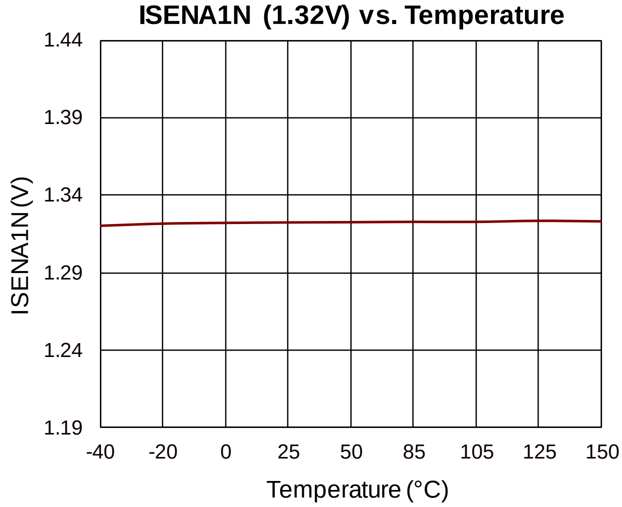
F_{SW_A} (410kHz) vs. Temperature



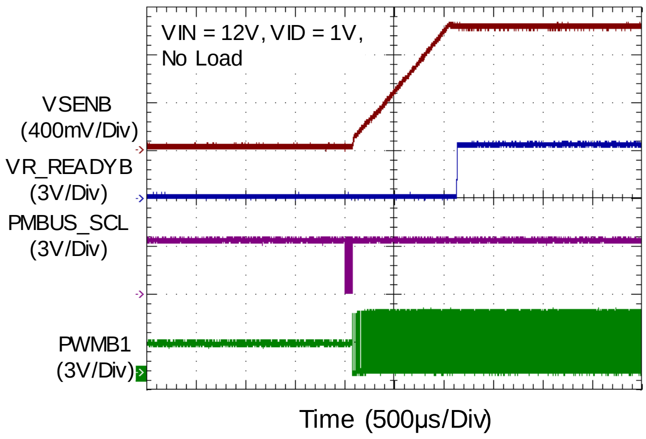
PWM_VCC (3.3V) vs. Temperature



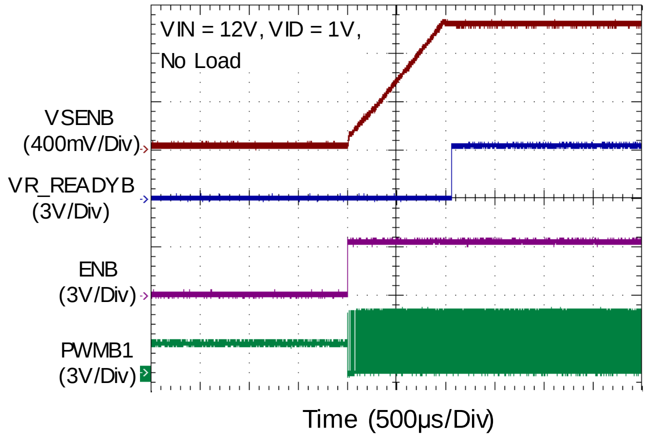
ISENA1N (1.32V) vs. Temperature



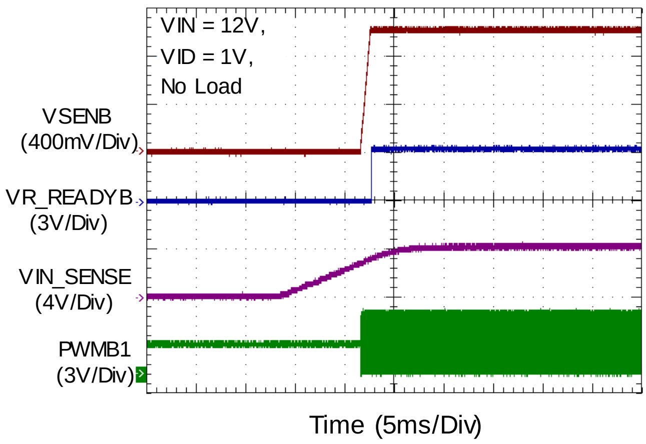
Power On from PMBUS



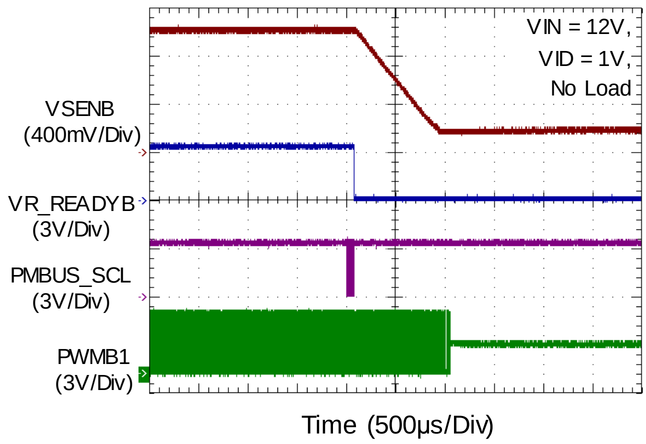
Power On from EN



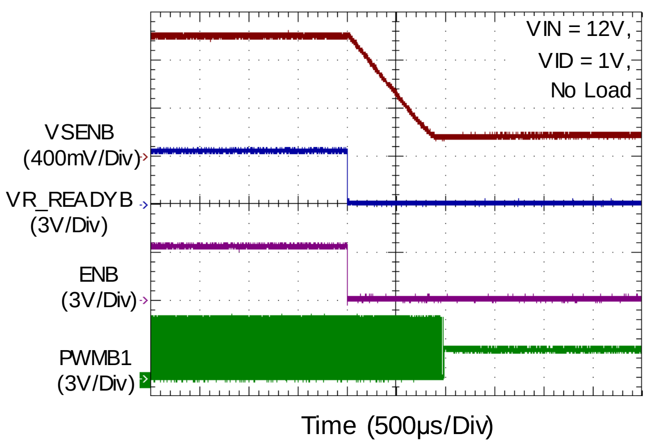
Power On from VIN



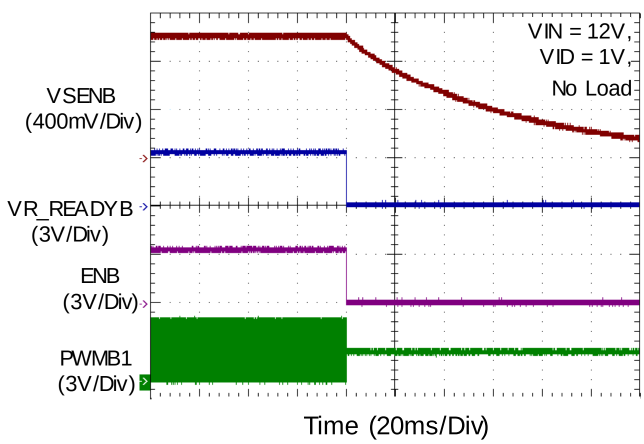
Power Off from PMBUS



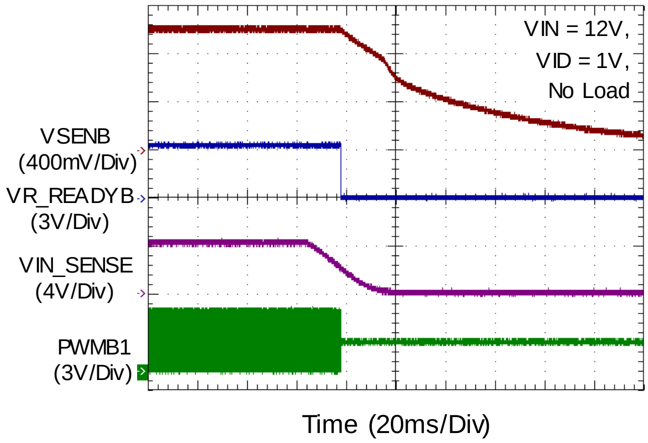
Power Off from EN (Soft Off)



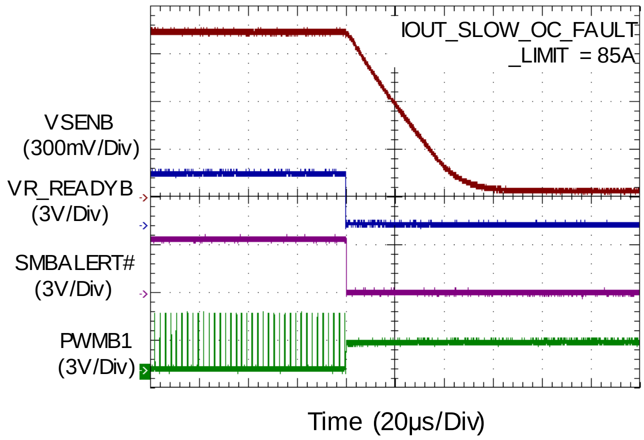
Power Off from EN (Immediately Off)



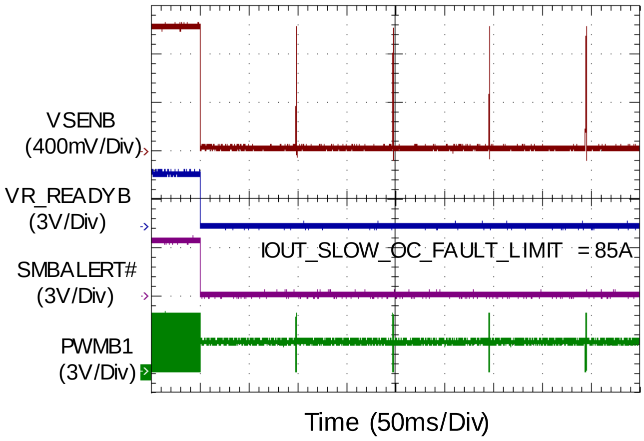
Power Off from VIN



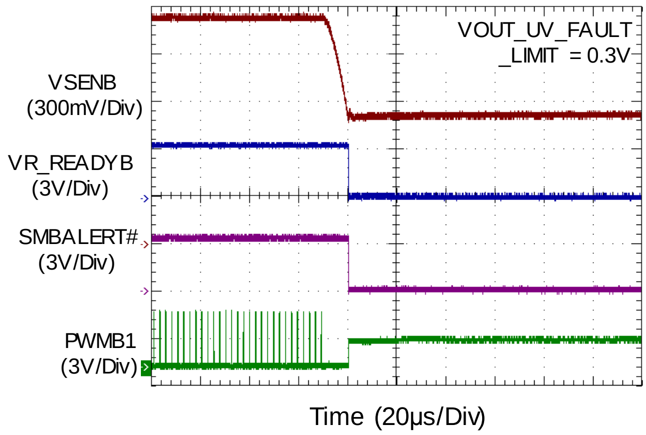
VR OCP (Latched Shutdown)



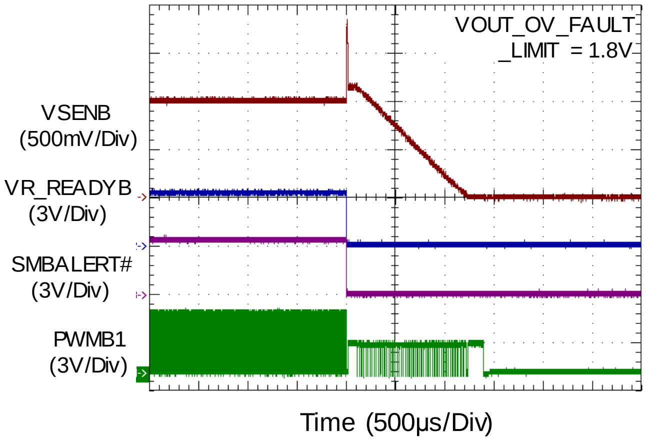
VR OCP (Hiccup Mode)



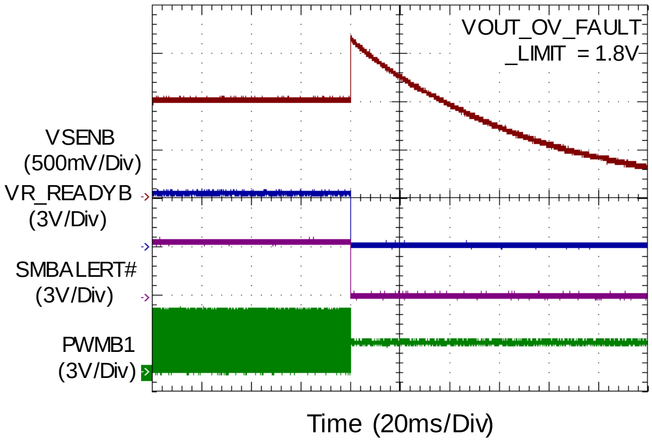
VR UVP



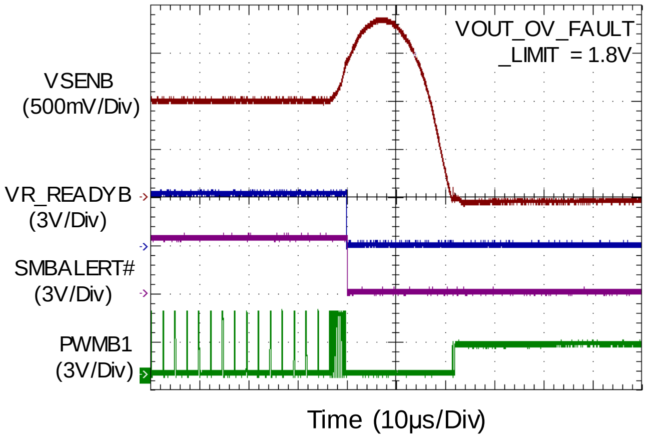
VR OVP (Soft Shutdown)



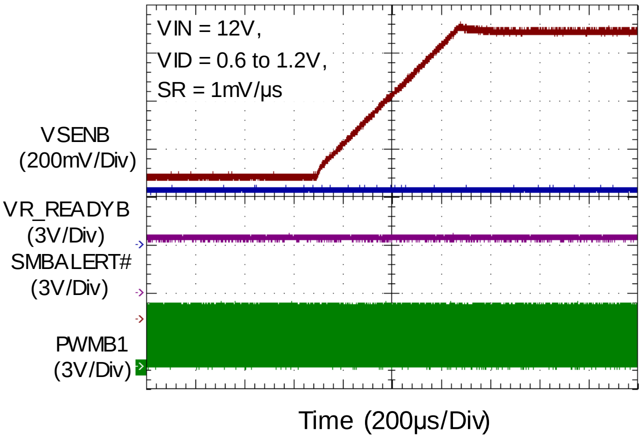
VR OVP (HiZ Shutdown)



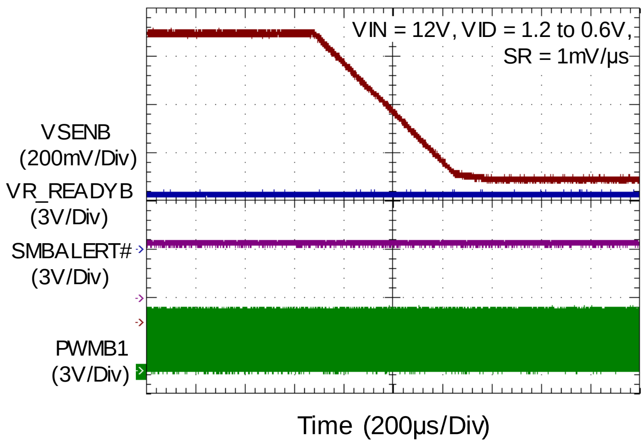
VR OVP (Turn On Low-Side MOSFET)



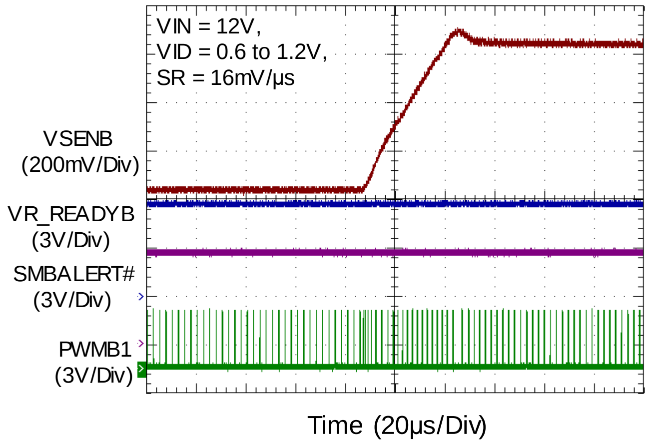
Dynamic-VID Up with Slow SR (1mV/μs)



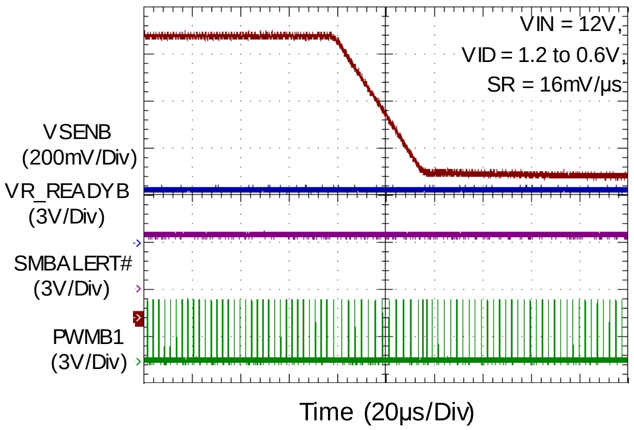
Dynamic-VID Down with Slow SR (1mV/μs)



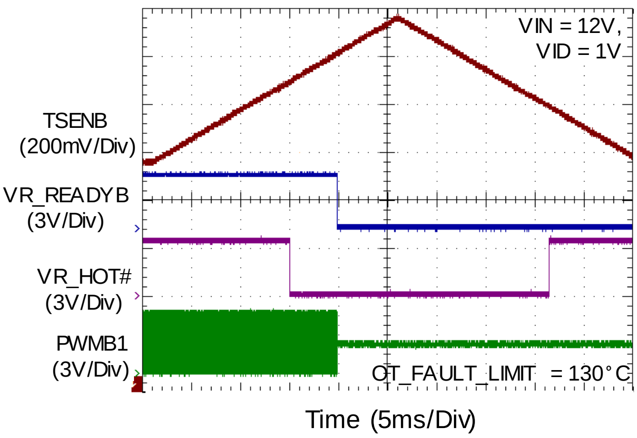
Dynamic-VID Up with Fast SR (16mV/μs)



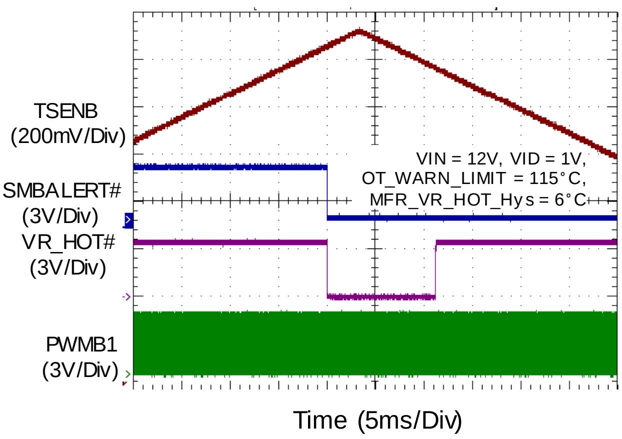
Dynamic-VID Down with Fast SR (16mV/μs)



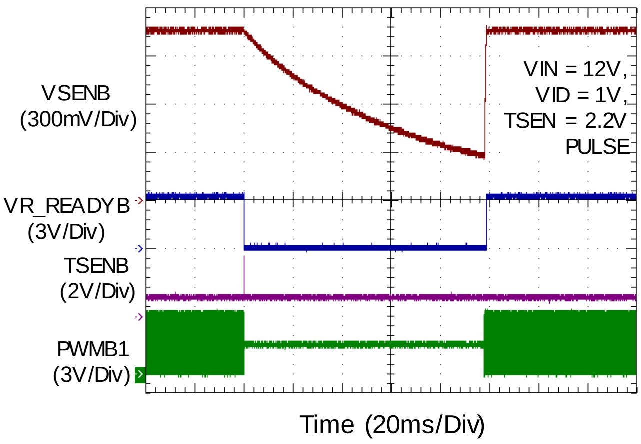
VR OTP



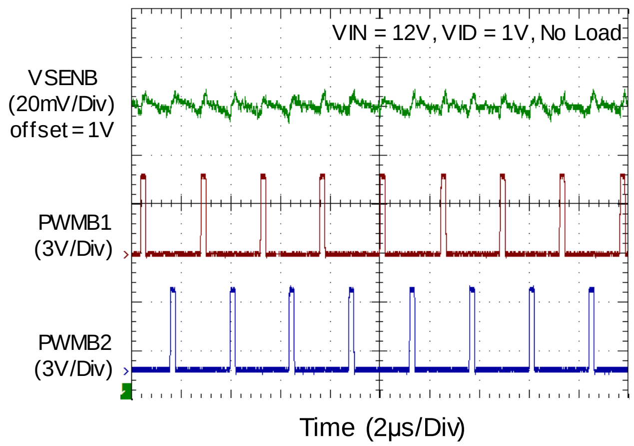
VR Thermal Warning



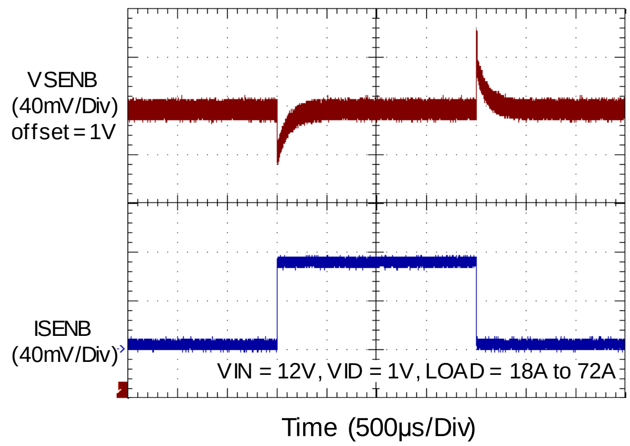
SPS Fault



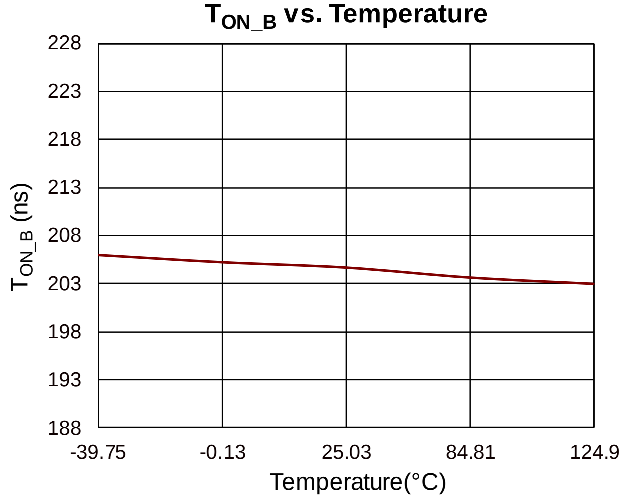
Output Ripple



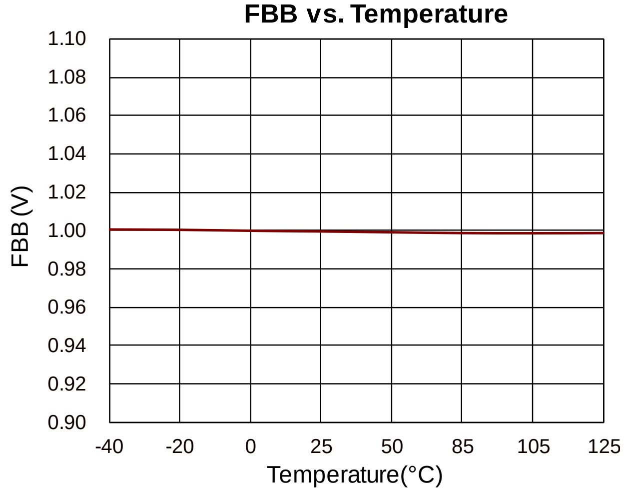
Transient Response

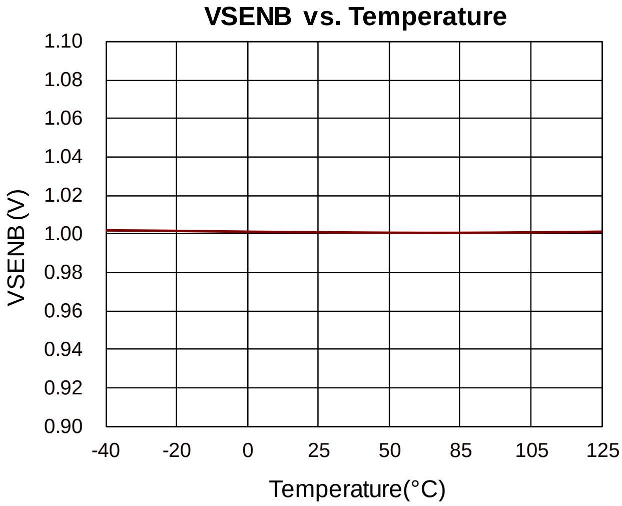


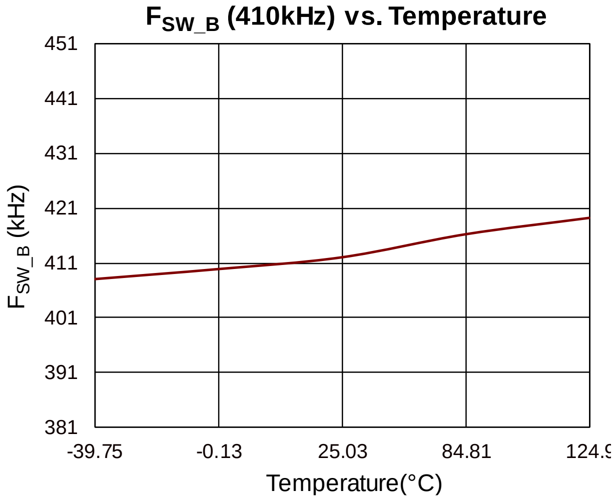
T_{ON_B} vs. Temperature

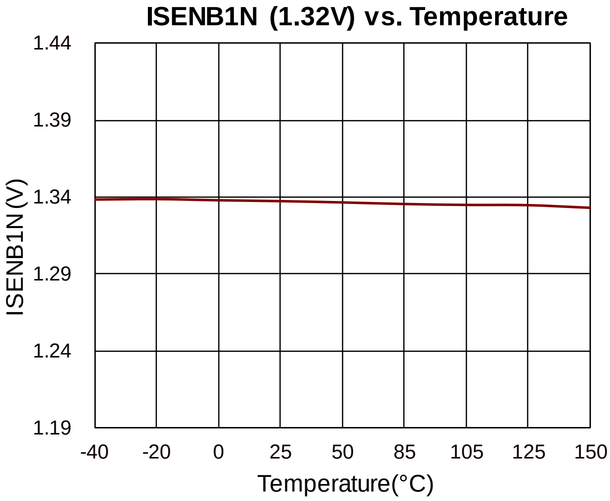


FBB vs. Temperature




VSENB vs. Temperature
1.10
1.08
1.06
1.04
1.02
1.00
0.98
0.96
0.94
0.92
0.90
VSENB (V)
-40
-20
0
25
50
85
105
125
Temperature(°C)


FSW_B (410kHz) vs. Temperature
451
441
431
421
411
401
391
381
FSW_B (kHz)
-39.75
-0.13
25.03
84.81
Temperature(°C)


ISENB1N (1.32V) vs. Temperature
1.44
1.39
1.34
1.29
1.24
1.19
ISENB1N (V)
-40
-20
0
25
50
85
105
125
150
Temperature(°C)

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RTQ8825 includes two voltage rails: a 3/2/1/0 phase synchronous buck controller, the rail A, and a 2/1/0 phase synchronous buck controller, the rail B. The RTQ8825 uses an ADC to implement all kinds of settings to save total pin number for easy use and increase PCB space utilization. The RTQ8825 is used in networking or telecom system.

Startup Configuration

The RTQ8825 is the state-machine based power management. Figure 2 shows the state-machine. Operation is controlled by application specific configuration settings loaded into control registers. For typical applications, the control registers are pre-programmed at the factory and stored in the on-chip nonvolatile memory (NVM). However, control registers can also be reprogrammed in the field via the serial communication PMBus and stored into the NVM.

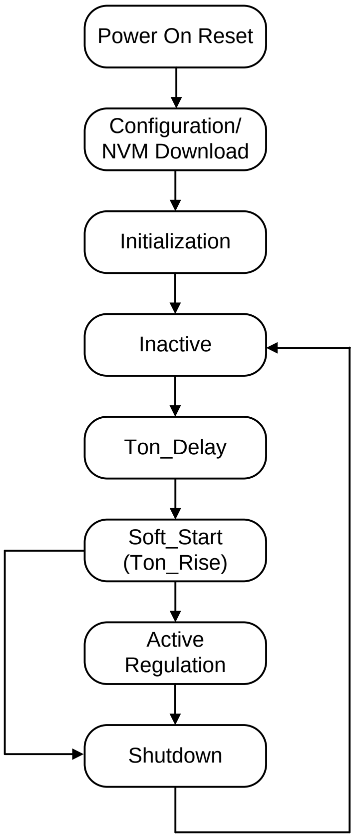


Figure 2. State-Machine

Power-ON Configuration

Supply a single +5.0V (VCC) to the RTQ8825 to start power-on. Figure 3 shows the power-on timings. NVM loading of the RTQ8825 begins after VCC crosses its rising VCC_POR_NVM threshold. When POR_NVM conditions are met, RTQ8825 will download NVM into the control registers. RTQ8825 operation is initialized while VCC exceeds VCC_POR threshold. Note that power on during OTP & SPS_Fault condistions, RTQ8825 will start from initialization after OTP & SPS_Fault are cleared. During this period, the internal 3.3V LDO is enabled, and the PWM outputs are held in high impedance (Hi-Z) state to ensure the SPS remain off. Allowing board pull-down resistors sets the correct default levels for static input signals, such as the I2C address, enabling load-line, SPS type and VBOOT (SET1, SETA1, SETB1, VBOOTAx and VBOOTBx). The maximum time from VCC exceeds VIN_POR threshold to initialization end is 5ms. When VCC and VIN satisfy their respective voltage conditions, the controller is in its shutdown state. It will transition to its active state and begin soft-start when the state of EN or OPERATION Command start-up. Note that SPS_VCC is strongly suggested to be ready before the RTQ8825_VCC exceeds VCC_POR threshold.

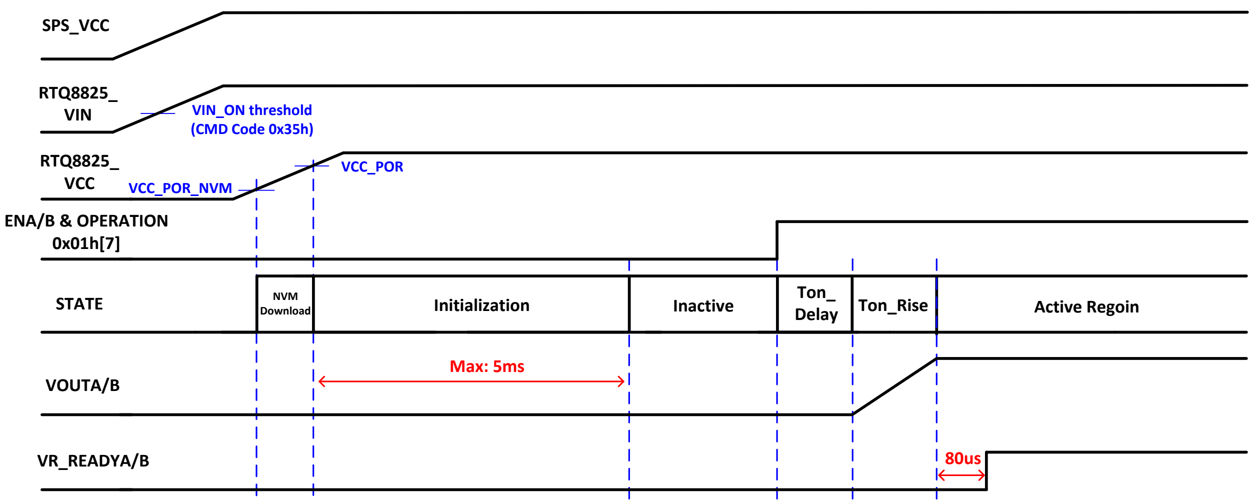


Figure 3. Power-ON Timings

Initialization

During the Initialization state, the RTQ8825 measures the external temperatures, input voltage, and executes the various calibration routines within the IC. To properly set the boot−up voltage, resistors with 1% tolerance must be connected from the VBOOTA0/B0, VBOOTA1/B1 and VBOOTA2/B2 pins to ground. Table 1 shows the boot−up voltage. To properly set the PMBus address(7-bit addressing), SPS type of rail A and enabling load-line function of rail A, resistors with 1% tolerance must be connected from the SETA1 and SET1 pins to ground. Table 2 shows the PMBus address, SPS type of rail A and enabling load-line function of rail A. To properly set the SPS type of rail B and enabling load-line function of rail B, resistors with 1% tolerance must be connected from the STEB1 pin to ground. Table 3 shows the SPS type of rail B and enabling load-line function of rail B.

Table 1. The Boot−up Voltage

VBOOTA2 VBOOTB2	VBOOTA1 VBOOTB1	VBOOTA0 VBOOTB0	VBOOT(V)
0Ω	0Ω	0Ω	0.602
0Ω	0Ω	16.9kΩ	0.625
0Ω	0Ω	31.6kΩ	0.648
0Ω	16.9kΩ	0Ω	0.672
0Ω	16.9kΩ	16.9kΩ	0.695
0Ω	16.9kΩ	31.6kΩ	0.719
0Ω	31.6kΩ	0Ω	0.742
0Ω	31.6kΩ	16.9kΩ	0.766
0Ω	31.6kΩ	31.6kΩ	0.789
16.9kΩ	0Ω	0Ω	0.813
16.9kΩ	0Ω	16.9kΩ	0.836
16.9kΩ	0Ω	31.6kΩ	0.859
16.9k Ω	16.9kΩ	0Ω	0.883
16.9k Ω	16.9kΩ	16.9kΩ	0.906
16.9k Ω	16.9kΩ	31.6kΩ	0.930
16.9k Ω	31.6kΩ	0Ω	0.953
16.9k Ω	31.6kΩ	16.9kΩ	0.977
16.9k Ω	31.6kΩ	31.6kΩ	1.000
31.6k Ω	0Ω	0Ω	1.023
31.6k Ω	0Ω	16.9kΩ	1.047
31.6k Ω	0Ω	31.6kΩ	1.070
31.6k Ω	16.9kΩ	0Ω	1.094
31.6k Ω	16.9kΩ	16.9kΩ	1.117
31.6k Ω	16.9kΩ	31.6kΩ	1.141
31.6k Ω	31.6kΩ	0Ω	1.164
31.6k Ω	31.6kΩ	16.9kΩ	1.188
31.6k Ω	31.6kΩ	31.6kΩ	1.211

Table 2. The PMBus Address (7-bit format), SPS Type of rail A and Enabling Load-Line Function of Rail A

SETA1	SET1	SPS Type	Load-line	PMBus Address	SETA1	SET1	SPS Type	Load-line	PMBus Address
0kΩ	0Ω	V-type	no LL	68	16.5kΩ	0Ω	V-type	no LL	70
	6.19kΩ			69		6.19kΩ			71
	9.09kΩ			6A		9.09kΩ			72
	12.4kΩ			6B		12.4kΩ			73
	16.5kΩ			6C		16.5kΩ			74
	21.5kΩ			6D		21.5kΩ			75
	27.4kΩ			6E		27.4kΩ			76
	35.7kΩ			6F		35.7kΩ			77
6.19kΩ	0Ω		LL*	68	21.5kΩ	0Ω		LL*	70
	6.19kΩ			69		6.19kΩ			71
	9.09kΩ			6A		9.09kΩ			72
	12.4kΩ			6B		12.4kΩ			73
	16.5kΩ			6C		16.5kΩ			74
	21.5kΩ			6D		21.5kΩ			75
	27.4kΩ			6E		27.4kΩ			76
	35.7kΩ			6F		35.7kΩ			77

SETA1	SET1	SPS Type	Load-line	PMBus Address	SETA1	SET1	SPS Type	Load-line	PMBus Address
9.09kΩ	0Ω	I-type	no LL	68	27.4kΩ	0Ω	I-type	no LL	70
	6.19kΩ			69		6.19kΩ			71
	9.09kΩ			6A		9.09kΩ			72
	12.4kΩ			6B		12.4kΩ			73
	16.5kΩ			6C		16.5kΩ			74
	21.5kΩ			6D		21.5kΩ			75
	27.4kΩ			6E		27.4kΩ			76
	35.7kΩ			6F		35.7kΩ			77
12.4kΩ	0Ω		LL*	68	35.7kΩ	0Ω		LL*	70
	6.19kΩ			69		6.19kΩ			71
	9.09kΩ			6A		9.09kΩ			72
	12.4kΩ			6B		12.4kΩ			73
	16.5kΩ			6C		16.5kΩ			74
	21.5kΩ			6D		21.5kΩ			75
	27.4kΩ			6E		27.4kΩ			76
	35.7kΩ			6F		35.7kΩ			77

*The Ai-gain for LL is set by MFR_Load_Line_DDh[[1:0].

Table 3. The SPS type of Rail B and Enabling Load-Line Function of Rail B

SETB1 pin	SPS Type	Load-line
0Ω	V-type	no LL
6.19kΩ		LL*
9.09kΩ	I-type	no LL
12.4kΩ		LL*
16.5kΩ	V-type	no LL
21.5kΩ		LL*
27.4kΩ	I-type	no LL
35.7kΩ		LL*

*The Ai-gain for LL is set by MFR_Load_Line_DDh[[1:0].

Inactive State and Ton_Delay

Upon completion of the Initialization process, the RTQ8825 will enter the Inactive State. Before the system can be started, the RTQ8825 will verify that the following conditions are satisfied:

1. VCC is valid: The voltage applied to VCC must exceed VIN_POR for the internal power valid signal to be asserted. Otherwise, RTQ8825 will be shutdown.

2. No shutdown faults are asserted.

3. VIN is valid: The voltage applied to VIN must exceed VIN_ON threshold for the internal VIN valid signal to be asserted. Otherwise, a VIN UVLO fault will be issued.

4. EN is asserted: It is recommended that EN be asserted only after VCC and VIN are ready.

Once the above startup conditions are satisfied, the RTQ8825 will wait for a programmable period of time (TON_DELAY) before ramping up the output voltage. TON_DELAY can be adjusted from 0ms to 51.0ms in 0.25ms increments.

Soft-Start (Ton_Rise)

Prior to entering the Active Regulation state, the RTQ8825 performs a controlled, monotonic soft-start ramp of the voltage output. At the onset of soft-start, the RTQ8825 will perform a pre-bias condition measurement of the output voltage. The RTQ8825 will set the initial startup ramp voltage at the appropriate level so that it will not sink current from the pre-biased output. Soft-start is performed by actively regulating the output voltage while digitally ramping up a DAC reference voltage from the measured pre-biased voltage to its final target value. After the regulator completes the initial output ramp to the Vboot voltage in the TON_RISE time, it enters the Active Regulation state and the VR_READY pin is asserted indicating after 80μs.

Active Regulation

The RTQ8825 doesn't need a complex type III compensator to optimize control loop performance. It can adopt a type II compensator (one pole, one zero) in the G-NAVP^{TM} topology to achieve the best performance in load-transient test. The one pole and one zero compensator is shown in Figure 4. R_{EA2}/R_{EA1} is ERROR AMP gain and is suggested within 2.5~3.5 for better transient response.

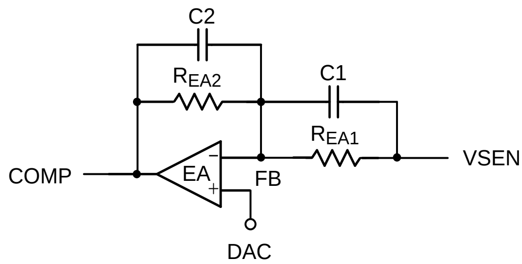


Figure 4. Type II Compensator

Shutdown

The Shutdown state can be entered from either Soft Start or Active Regulation states through user intervention (de-asserting EN) or through a detected fault including over-temperature, over-current, input under-voltage, output over-voltage, output under-voltage and SPS fault conditions. For cases where the shutdown is caused by a fault, the resultant shutdown response is always Hi-Z where the output stage power FETs are immediately switched off. Once the RTQ8825 enters the shutdown state, the IC will be transformed to the inactive state.

Maximum Active phases Number

The number of active phases is determined by ISENxP voltages. Normally, the RTQ8825 operates as a 3+2-phase PWM RTQ8825. Connecting directly or tie 0Ω from ISENA3P pin to VCC programs 2−phase operation on rail A, and connecting directly or tie 0Ω from ISENA2P pin to VCC programs 1−phase operation on rail A. The unused ISENxN pins and PWM pins can be floating.

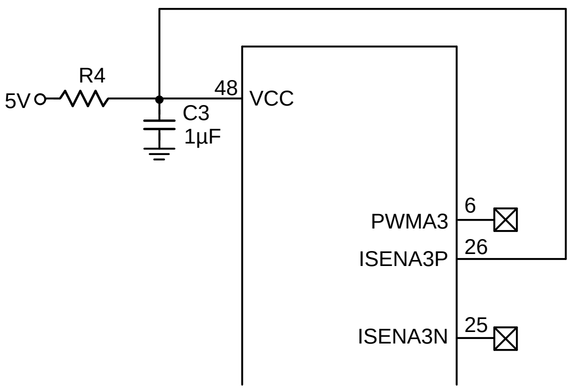


Figure 5. Disable the third phase of rail A

Rail Disable

Connect directly or tie 0Ω from ISENA1P to VCC to disable rail A. Connect directly or tie 0Ω from ISENB1P to VCC to disable rail B. The unused ISENxN pins and PWM pins can be floating.

AC-droop

The RTQ8825 builds in AC-droop feature, and the output voltage is determined only by VID and does not vary with the loading current like load-line system behavior. The AC-droop to effectively suppress load transient ring back and to control overshoot. Figure 6 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back ΔV2 due to C area charge. Figure 7 shows the condition with AC-droop control. While loading occurs, the RTQ8825 will temporarily change VID target to short-term voltage target. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as the follows :

$$Short\_Term\_Voltage\_Target = VID - \Delta I_{CC} \times R_{LL}$$

The setting method of R_{LL} is the same as loadline system. The short-term voltage target reverts to VID target slowly after a period of time. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back ΔV2 can be suppressed. The overshoot amplitude is reduced to only ΔV3.

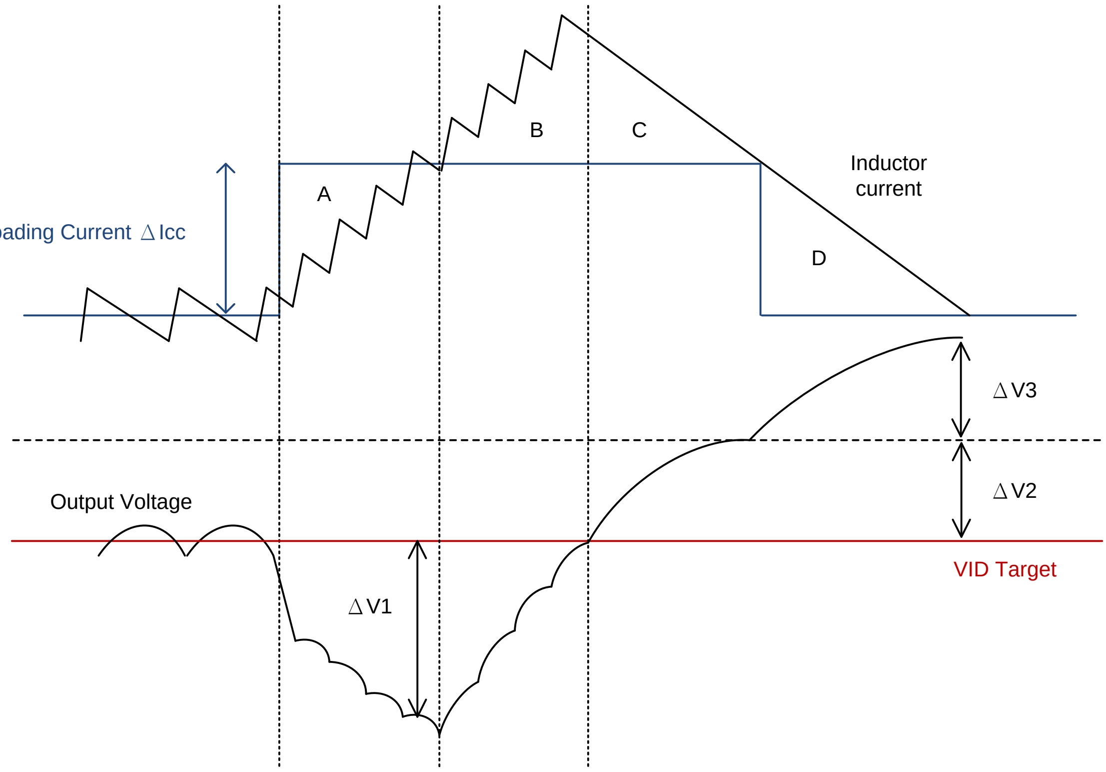


Figure 6. Without AC-droop Control

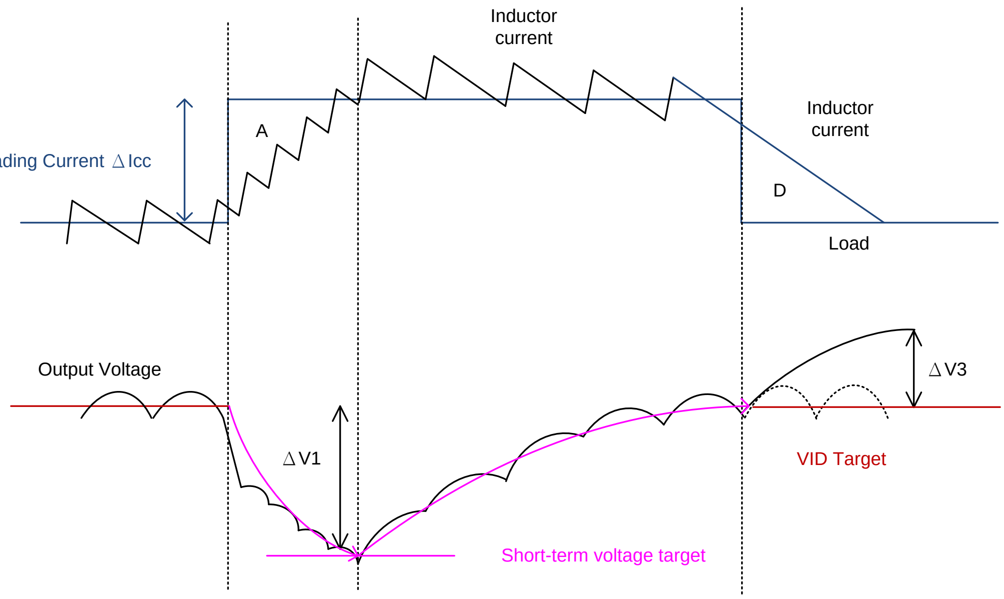


Figure 7. with AC-droop Control

Load-line (R_{LL})

An output voltage load-line (Adaptive Voltage Positioning) are specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount proportional to the increasing loading current, i.e. the slope between output voltage and loading current (R_{LL}) is shown in Figure 8. Figure 9 shows how the voltage and current loop parameters of RTQ8825 to achieve load-line. The detailed equation is described as below :

For voltage type SPS :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{5mV}{1A} \times \frac{Ai}{\frac{R_{EA2}}{R_{EA1}}} \times \frac{5}{4}$$

For current type SPS :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{5\mu A}{1A} \times \frac{Ai}{\frac{R_{EA2}}{R_{EA1}}} \times 1250\Omega$$

Ai is current gain. $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested within 2.5~3.5 for better transient response. RLL can be programmed by Ai and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be selected by MFR_Load_Line (DDh) register.

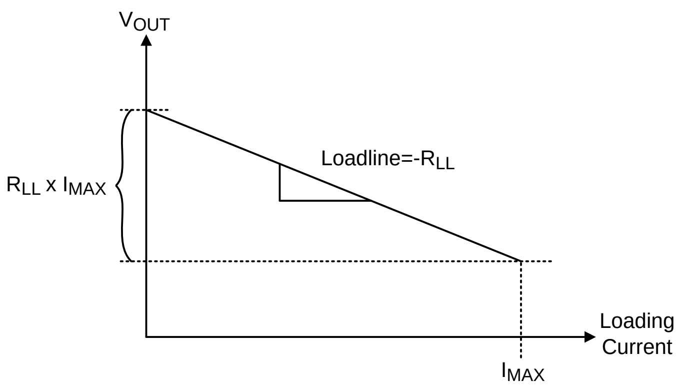


Figure 8. Load-Line (Droop)

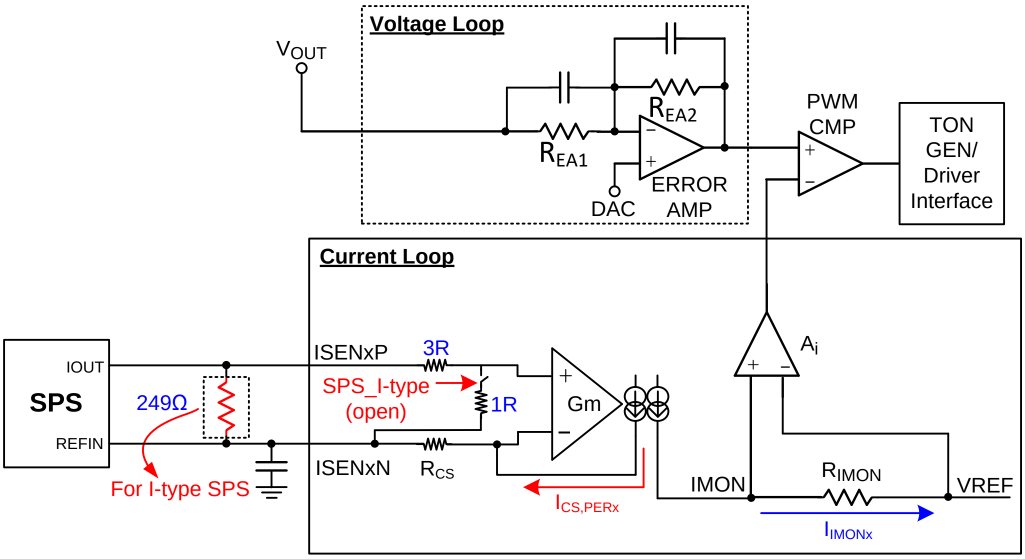


Figure 9. Voltage Loop and Current Loop for Load-line

Dynamic VS (DVS) Compensation

During VOUT transition, an extra current is required to charge output capacitor for increasing voltage. The charging current approximates to the product of the DVS slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach target within the specified time. The extra voltage drop approximates to DVS Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the load-line slope, Ω). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 10. DVS compensation function is shown in Figure 11. An internal current I_{DVS_LIFT} is sinking internally from FB pin to generate DVS compensation I_{DVS_LIFT} x R_{EA1}. I_{DVS_LIFT} can be set via MFR_DVS_Compensate (DCh) register. For different scale of DVS SR, I_{DVS_LIFT} is internally adjusted. Compensating magnitude can also be adjusted by R_{EA1}. While DAC just arrives target, inductor current is still high and needs a time to settle down to the DC loading current. ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects DVID behavior. The final setting should be based on actual measurement.

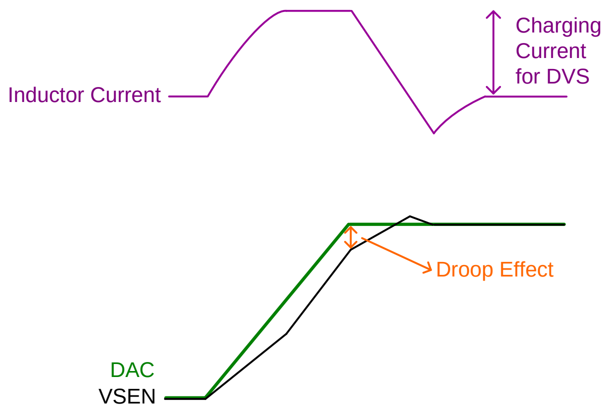


Figure 10. Droop Effect in VOUT Transition

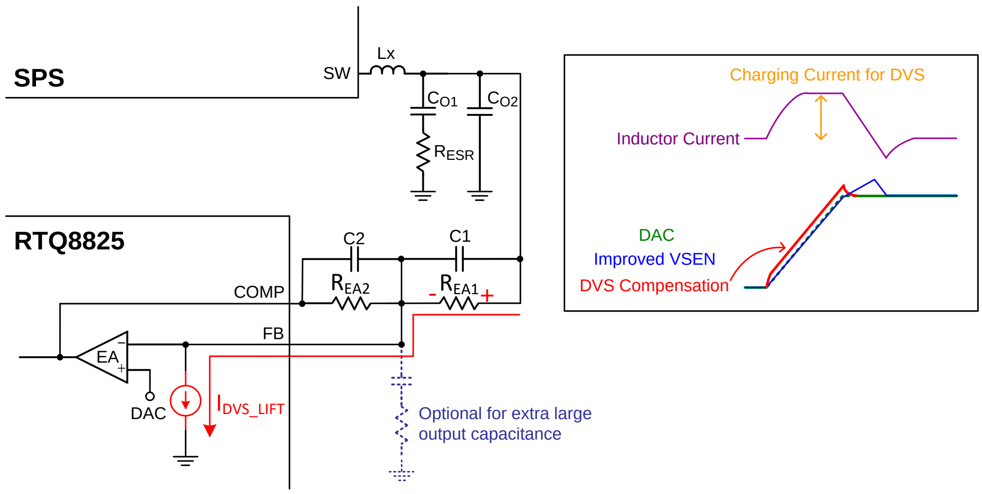


Figure 11. DVS Compensation

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the board traces, SOC internal power routes and socket contacts. The SOC contains on-die sense pins, VCC_SENSE and VSS_SENSE. The related connection is shown in Figure 12. The DAC voltage is referred to RGND to provide accurate voltage at remote SOC side. While SOC is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

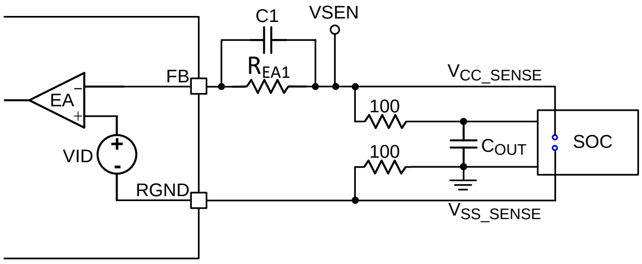


Figure 12. Remote Sensing Circuit

Switching Frequency

The topology G-NAVP^{TM} (Green Native AVP) is one kind of current-mode constant on-time control. It generates an adaptive TON (PWM) with input voltage (VIN) for better line regulation. The TON is also adaptive to DAC voltage. For DAC < 0.6V application, the adaptive TON is based on constant current ripple concept for better output voltage ripple size control. For DAC ≥ 0.6V application, the adaptive TON is based on constant frequency concept for better efficiency performance. Figure 13 is the conceptual chart showing the relationships between switching frequency vs DAC and current ripple vs DAC. The RTQ8825 provides a parameter setting of k_{TON} to design TON width. The k_{TON} is set via MFR_Kton (D7h) register.

The equations of TON are listed as below :

DAC ≥ 0.6V,

$$T_{ON}=2.2634\mu\times\frac{DAC}{k_{TON}\times(V_{IN}-0.6V)}+10ns$$

0.3 < DAC < 0.6V,

$$T_{ON}=1.3584\mu\times\frac{1}{k_{TON}\times(V_{IN}-DAC)}+10ns$$

DAC ≤ 0.3V,

$$T_{ON}=1.3584\mu\times\frac{1}{k_{TON}\times(V_{IN}-0.3)}+10ns$$

The switching frequency can be derived from TON as shown as below. The losses in the main power stage and driver characteristics are considered.

$$Freq=\frac{DAC+\frac{I_{CC}}{N}\times\left(DCR+\frac{R_{ON_{LS,max}}}{n_{LS}}-N\times R_{LL}\right)}{\left[V_{IN}+\frac{I_{CC}}{N}\times\left(\frac{R_{ON_{LS,max}}}{n_{LS}}-\frac{R_{ON_{HS,max}}}{n_{HS}}\right)\right]\times\left(T_{ON}-T_D+T_{ON,\,VAR}\right)+\frac{I_{CC}}{N}\times\frac{R_{ON_{LS,max}}}{n_{LS}}\times T_D}$$

DAC : DAC voltage

VIN : input voltage

I_{CC} : loading current

N : total phase number

$R_{ON_{HS,max}}$: maximum equivalent high-side RDS(ON) n_{HS} : number of high-side MOSFETs

$R_{ON_{LS,max}}$: maximum equivalent low-side RDS(ON)

n_{LS} : number of low-side MOSFETs

T_D : summation of the high-side MOSFET delay time and rising time

$T_{ON,VAR}$: on-time variation value

DCR : inductor DCR

R_{LL} : loadline setting (Ω)

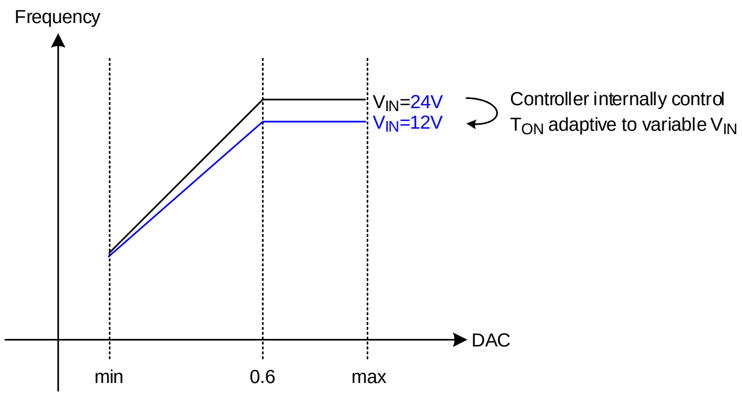


Figure 13. Switching Frequency and Current Ripple with Different DAC

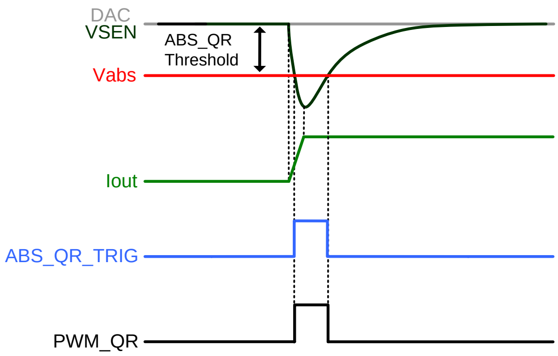
Absolutely Quick Response (ABS_QR) and Adaptive Quick Response(AQR)

The RTQ8825 provides Absolutely Quick Response (ABS_QR) and Adaptive Quick Response (AQR) to optimize transient response for no load-line and load-line system respectively. Figure 14 shows the mechanism concept for Absolutely Quick Response (ABS_QR) and Adaptive Quick Response (AQR). The output voltage is monitored at the VSEN pin. Absolutely Quick Response (ABS_QR) is illustrated in Figure 14(a), the Vabs represents DAC minus ABS_QR Threshold. Since output voltage does not change with loading during steady-state in no load-line system, RTQ8825 detects the absolute value of output voltage drop. While the absolute value of output voltage drop exceeds ABS_QR_threshold, an ABS_QR_TRIG signal is generated to turn on all PWMs at the same time, and ABS_QR_TRIG width is decided by the duration of output voltage drop exceeds ABS_QR_threshold.

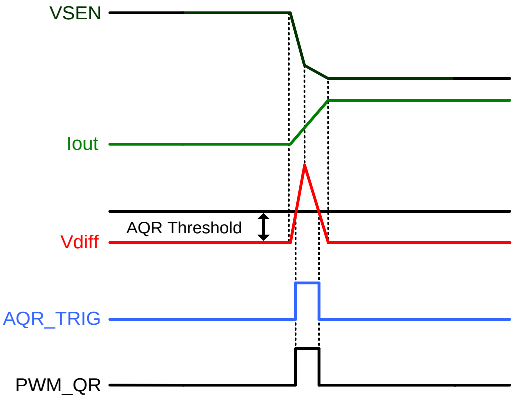
In load-line system, ABS_QR is not applicable because output voltage decreases with the increasing loading current. Instead of ABS_QR, RTQ8825 provides Adaptive Quick Response (AQR) which detects output voltage drop slew rate in Figure 14(b). While the slew rate exceeds the AQR threshold, AQR_TRIG signal is generated until output voltage slew rate significantly slows down. The output voltage slew rate transition also indicates that inductor current almost reaches the loading current. Under such mechanism, AQR_TRIG width is adaptive to variable loading step. The AQR starting trigger threshold equation is described as below :

$$\text{AQR Starting Trigger Threshold} = -4u \times \frac{dVSEN}{dt}$$

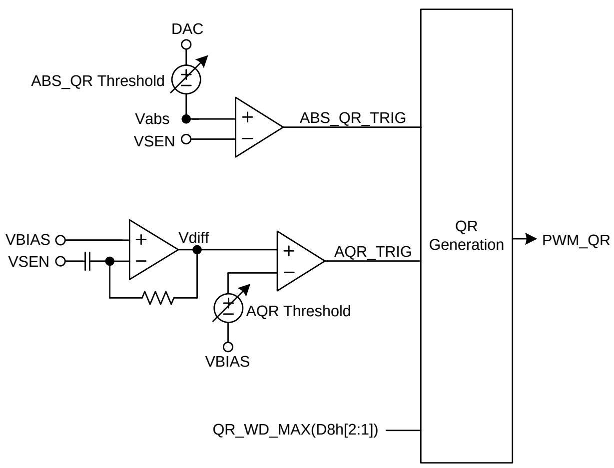
As ABS_QR_TRIG or AQR_TRIG is triggered, PWM_QR is generated by QR generation to force all PWMs turn on simultaneously in Figure 14(c). For ABS_QR, PWM_QR pulse width is decided by output voltage drop and maximum is adjustable by QR_WD_MAX(D8h[2:1]). For AQR, PWM_QR pulse width is decided by slew rate of output voltage drop and maximum is adjustable by QR_WD_MAX(D8h[2:1]). The RTQ8825 also provides various ABS_QR threshold via MFR_ABS_QR (DFh) register and AQR threshold via MFR_AQR (D8h) register. Smaller threshold indicates larger ABS_QR_TRIG or AQR_TRIG width. For ABS_QR, to avoid triggering ABS_QR in the steady-state, note that the threshold should be larger than output voltage ripple. For AQR, to avoid triggering AQR in the steady-state, note that the threshold should be larger than the falling slew rate of output voltage ripple and the falling slew rate of overshoot.



(a). Absolutely Quick Response Mechanism



(b). Adaptive Quick Response Mechanism



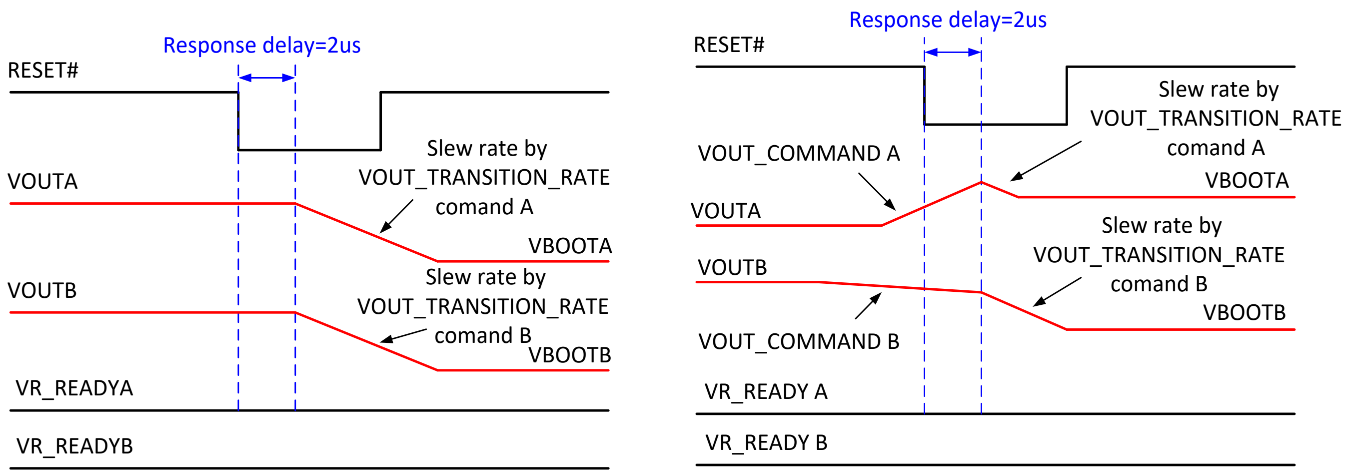
(c). Quick Response Block Diagram

Figure 14. Quick Response Mechanism

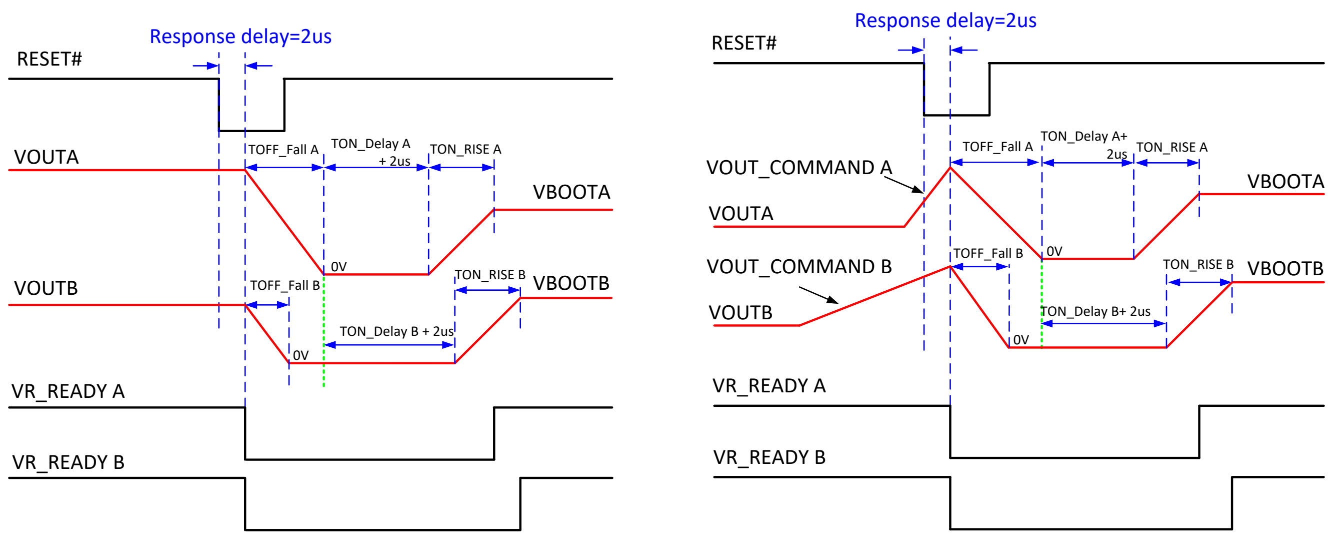
Reset VOUT

Without power cycling, the VOUT_COMMAND value and the corresponding output voltage can be reset to the default value which is latched when the devices are powered up from VCC. When the RESET# pin is pulled low, the RTQ8825 sets the VOUT_COMMAND value to the default value. Figure 15 shows the timing diagram for resetting the output voltage. When the RESET# pin is asserted low, after a short delay (greater than 2μs), the output voltage begins to transition from the current value to the default VOUT_COMMAND value according to the slew-rate set in the VOUT_TRANSITION_RATE command. The reset VOUT mode selection in the MFR_RESET _RESPONSE_Rail_Fault_Mode (DAh) register is set.

The VOUT_COMMAND value does not change to any values programmed in the VOUT_COMMAND register while the RESET# pin is held low.



(a). Mode 1 : The output voltage begins to transition from the current value to the VBOOT value.



(b). Mode 2 : Rails be restarted.

Figure 15. Output Voltage Reset

Output Voltage Discharge

When the RTQ8825 is disabled through VIN, EN or PMBus OPERATION command both the high-side and low-side MOSFET are turned off. A discharge MOSFET connected between VSEN and GND is turned on to discharge the output voltage. The typical switch on-resistance of this MOSFET is about 40Ω.

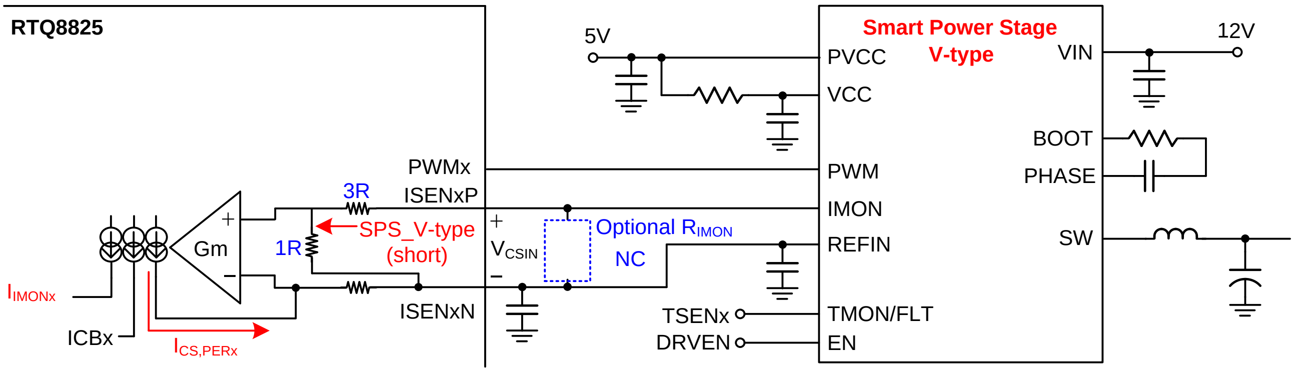
Per Phase SPS Current Sense

To achieve higher efficiency, SPS current sense is accomplished by sensing each SPS IOUT output individually using a 1.32V common mode buffer ISENxN pin to provide biasing for the current sense signal. The current sense lines should be run as differential pairs from the SPS back to the RTQ8825 on the same layer. Differential voltage range of current sense input (V_{CSIN} = ISENxP - ISENxN) is -40mV to 400mV with V-type SPS and -10mV~100mV with I-type SPS individually through pin setting with SETA1 pin.

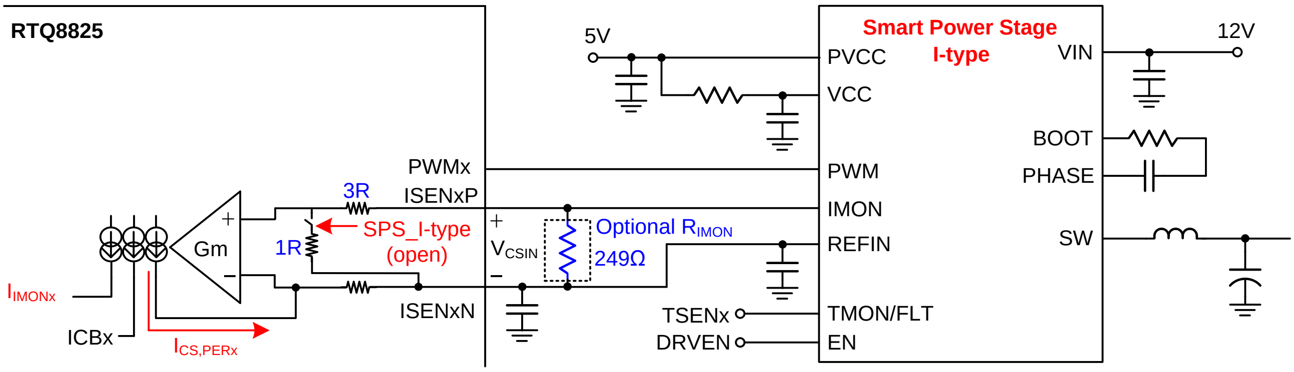
For V-type SPS, SPS IOUT output voltage represents current information at 5mV/A. To prevent V_{CSIN} from exceeding current sense amplifier input range, 1R is internal closed through pin setting, as illustrated in Figure 16(a). The internal current sense input is 0.25 time of V_{CSIN} through resistance divider.

For I-type SPS, SPS IOUT output current represents current information at 5μA/A. To prevent V_{CSIN} from exceeding current sense amplifier input range, 1R is internal open through pin setting, and RIMON is suggested 249Ω that is must place at IC side, as illustrated in Figure 16(b).

The current signal $I_{CS,PERx}$ is mirrored for loadline controls current reporting and current balance. The mirrored current to I_{MONx} is A_{MIRROR} time $I_{CS,PERx}$. A_{MIRROR} is internal current mirror gain of per phase current sense ($I_{IMON} = A_{MIRROR} \times I_{CS,PERx}$, $A_{MIRROR} = 1$).



(a). V-type SPS Current Sense Configuration



(b). I-type SPS Current Sense Configuration

Figure 16. SPS Current Sense Configuration

Under-Voltage Lockout (UVLO)

The RTQ8825 monitors the input voltage of power stage and controller using the VIN and VCC pins to detect an under-voltage condition.

The devices provide flexible user adjustment of the under-voltage lockout (UVLO) threshold and hysteresis for VIN. Two PMBus commands, VIN_ON (35h) and VIN_OFF (36h), allow the user to independently set turn on and turn off thresholds of these input voltages, with a minimum of 1.1V turn off to a maximum 3V turn on. Note that VIN pin must be connected to +12V supply through a resistor divider. While the VIN falls below VIN_OFF(36h) threshold, the VIN_UVLO fault is triggered. The device will de-assert VR_READY, assert SMBALERT#, STATUS_INPUT[3] is set to 01h and turns off both the high-side and low-side MOSFET to stop power conversion immediately.

While the VCC falls below ($V_{CC\_POR\_R}$ − $\Delta V_{CC\_POR\_F\_HYS}$), the VCC_UVLO fault is triggered. The device will shutdown and PWM will be Hi-Z state and PMBus registers will be invalid. For more information, see Table 4.

Thermal Monitoring and Over-Temperature Protection (OTP)

The RTQ8825 support integrated power stages with dedicated temperature monitors. The VR_HOT# pin indicates the temperature status of the voltage regulator. The VR_HOT# pin is an open-drain output and an external pull-up resistor is required. The VR_HOT# signal can be used to inform the system that the temperature of the voltage regulator is too high and the load should reduce its power consumption. VR_HOT# only indicates a thermal warning, not a fault. The RTQ8825 asserts VR_HOT and SMBALERT#, and PWM maintains control of FETs while OT_WARNING is triggered.

The OT_FAULT_LIMIT (4Fh) register set the over-temperature threshold and the MFR_VR_HOT_Hys (D9h) register set the VR_HOT# hysteresis. If temperature drops below OT warning condition minus hysteresis and then VR_HOT# de-asserts. The OTP is triggered and turns off both the high-side and low-side MOSFET. Figure 17 shows the thermal warning to VR_HOT# and Figure 18 shows the over-temperature fault to shutdown. There are three kinds of OTP Fault response: Latch-off, Restart, and Ignore. That can be set through the OT_FAULT_RESPONSE (50h) register. Table 4 summarizes the Fault Protection Responses scheme.

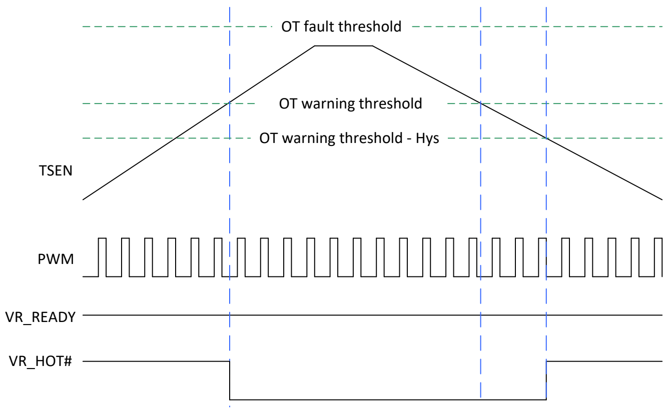


Figure 17. Thermal Warning

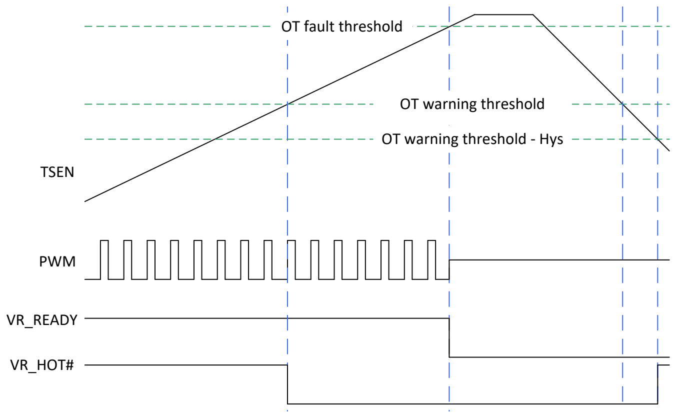


Figure 18. Over-temperature Fault

Slow Over-Current Protection (SLOW_OCP)

The RTQ8825 calculate total current by summing of phase currents from all active phases. The IOUT_SLOW_OC_FAULT_LIMIT (46h) register sets the over total current threshold and the SLOW_OC_DLY_Time (D6h[1:0]) register sets the SLOW_OC delay time = 20μs/32μs/44μs/56μs. It is recommended that the SLOW_OCP threshold be set at number of active phases multiplied by the current handling capability of the power stage. The SLOW_OCP is masked during VOUT transition period and 80us after VOUT settles. The RTQ8825 de-assert VR_READY, asserts SMBALERT# and turns off both the high-side and low-side MOSFET while SLOW_OCP is triggered. Figure 19 shows the over-Slow Over-Current Fault to shutdown. There are three kinds of SLOW_OCP Fault response : Latch-off, Restart , and Ignore. That can be set through the IOUT_SLOW_OC_FAULT_RESPONSE (47h) register. Table 4 summarizes the Fault Protection Responses scheme.

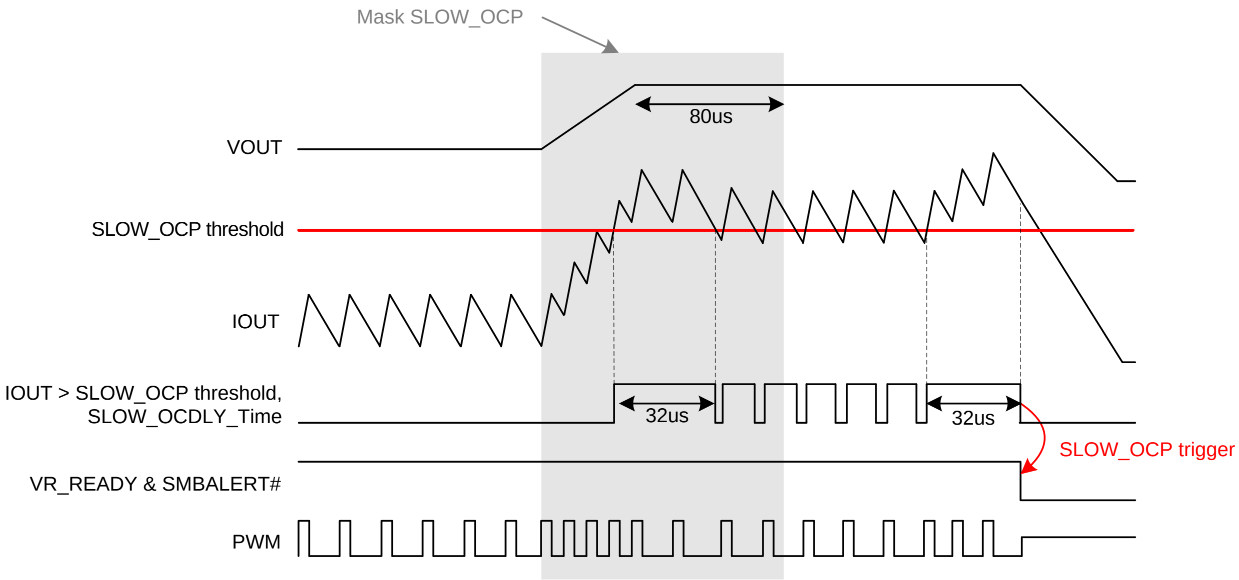


Figure 19. Slow Over-Current Fault SLOW_OC_DLY_Time (D6h[1:0]=01)

Fast Over-Current Protection (FAST_OCP)

The RTQ8825 provide Fast Over-Current Protection (FAST_OCP) in soft-start state within 2us delay, ex: short then power on, hiccup, during VOUT transition period etc. The IOUT_FAST_OC_FAULT_LIMIT (D6h[3:2]) register sets the value of the pre-phase output current, in Amps, that causes an fast over-current fault condition. It is recommended that the FAST_OCP threshold(per-phase) be set above SLOW_OCP threshold(sum) to protect the device not destroyed from charging current or inrush current in soft-start state. The RTQ8825 de-assert VR_READY, asserts SMBALERT# and turns off both the high-side and low-side MOSFET while FAST_OCP is triggered. Figure 20 shows the Fast Over-Current Fault to shutdown. There are three kinds of FAST_OCP Fault response : Latch-off, Restart , and Ignore. That can be set through the MFR_IOUT_ FAST_OC _FAULT_RESPONSE (E1h) register. Table 4 summarizes the Fault Protection Responses scheme.

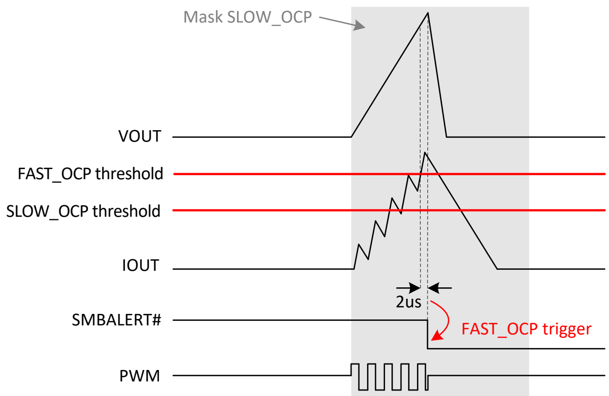


Figure 20. Fast Over-Current Fault (Output short then power on)

Under-Voltage Protection (UVP)

The RTQ8825 monitors the output voltage using the VSEN pin to detect an under-voltage condition. The VOUT_UV_FAULT_LIMIT (44h) register set the under-voltage threshold. If the VSEN voltage drops below the UVP threshold with 3μs debounce time. The RTQ8825 de-assert VR_READY, asserts SMBALERT# and turns off both the high-side and low-side MOSFET while UVP is triggered. The UVP is masked during VOUT transition period and 80us after VOUT settles. Figure 21 shows the over-current fault to shutdown. There are three kinds of UVP Fault response : Latch-off, Restart, and Ignore. That can be set through the VOUT_UV_FAULT_RESPONSE (45h) register. Table 4 summarizes the Fault Protection Responses scheme.

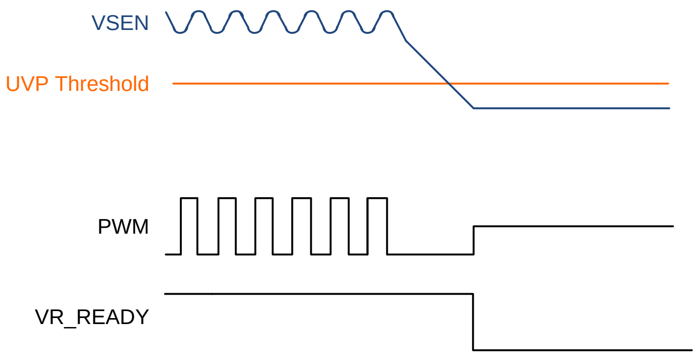


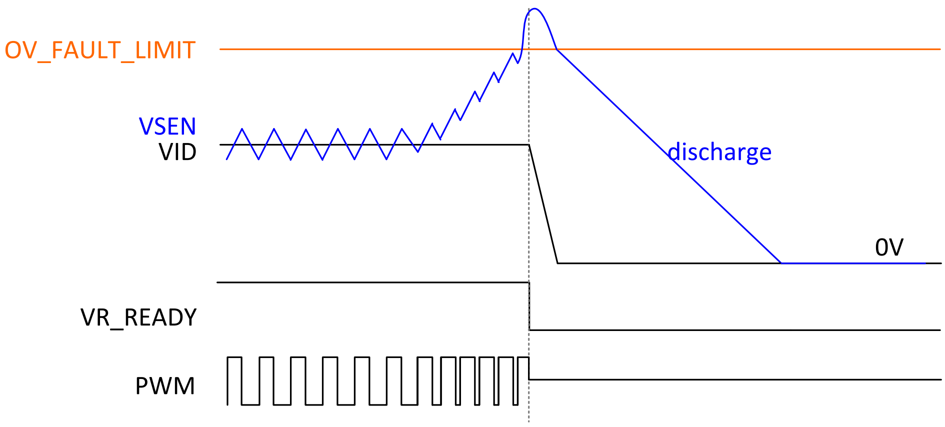
Figure 21. Under-Voltage Fault

Over-Voltage Protection (OVP)

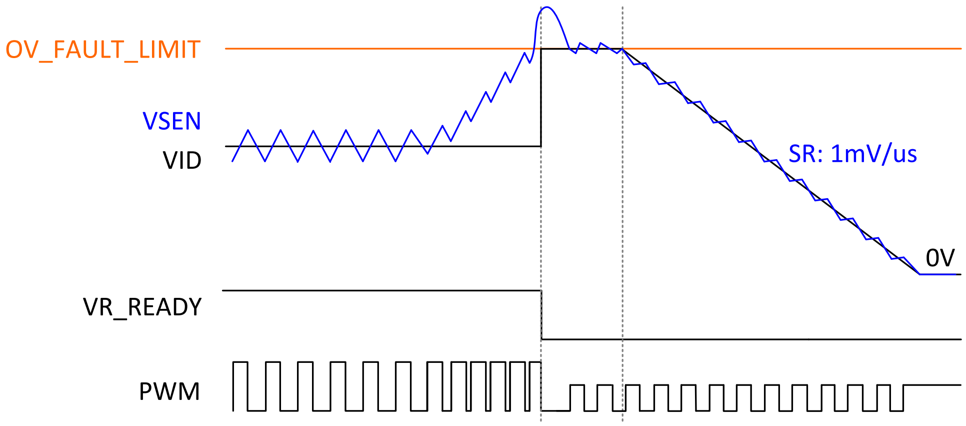
The RTQ8825 monitors the output voltage using the VSEN pin to detect an over-voltage condition. There are three kinds of OVP behaviors, and the OVP behavior can be set through the MFR_OV_Behavior (DBh) register. For the first OVP behavior, when OVP is triggered with 0.5μs filter time, the RTQ8825 de-asserts VR_READY, asserts SMBALERT# and turns off both high-side and low-side power MOSFETs.

For the second OVP behavior, when OVP is triggered with 0.5μs filter time, the RTQ8825 de-asserts VR_READY, asserts SMBALERT# and DAC voltage of the OVP rail will be slowly ramp down to 0V.

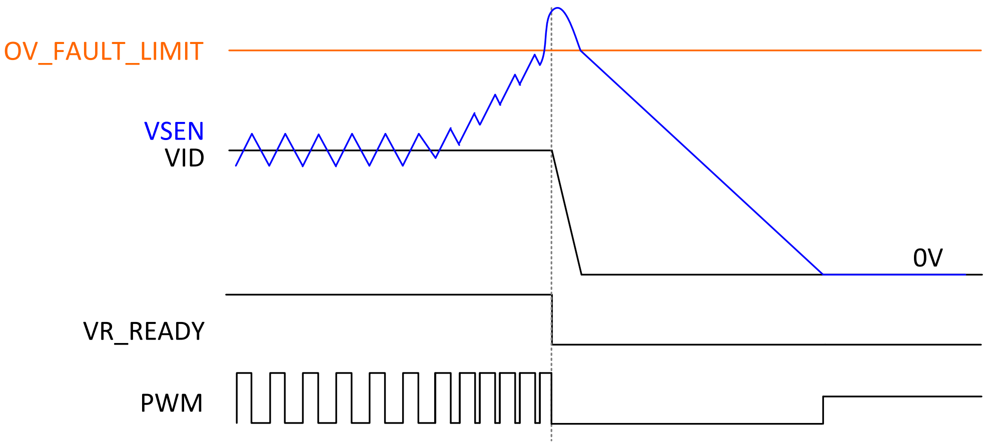
For the third OVP behavior, when OVP is triggered with 0.5μs filter time, the RTQ8825 de-asserts VR_READY, asserts SMBALERT# and forces all PWMs low to turn on low-side power MOSFETs. The PWM remains low until the output voltage is pulled down below DAC. The OVP mechanism is shown in Figure 22. There are three kinds of OVP Fault response : Latch-off, Restart, and Ignore. That can be set through the VOUT_OV_FAULT_RESPONSE (41h) register. Table 4 summarizes the Fault Protection Responses scheme.



(a). The First OVP Behavior (HiZ shutdown mode)



(b). The Second OVP Behavior (Soft-shutdown mode)



(c). The Third OVP Behavior (Turn on the low-side MOSFET)

Figure 22. Over-Voltage Fault

SPS Fault

The RTQ8825 supports integrated power stages with SPS Fault. The SPS (Smart Power Stage) will pull the temperature reporting pin (TSENA/B) high when a driver fault is detected by the integrate power stage. The RTQ8825 de-asserts VR_READY, asserts SMBALERT# and turns off both high-side and low-side power MOSFETs while TSENA/B exceeds Driver Fault Comp threshold. Then, RTQ8825 restarts after both 100ms and SPS Fault = L. Driver faults include over-current, over-temperature, high-side FET short, and low-side FET short etc. Table 4 summarizes the Fault Protection Responses scheme.

Telemetry for VOUT/IOUT/Temperature

The RTQ8825 supports the telemetry function for VOUT/IOUT/Temperature.

The device continually digitizes the sensed output voltage from differential voltage sense input (VSEN and RGND), and averages it to reduce measurement noise. Using the MFR_VOUT_RPT_GAIN (E0h) command to cancel IR drop affect to improve accuracy of VOUT reporting. Then the current value is stored in the READ_VOUT (8Bh) register.

The device continually digitizes the sensed the corresponding channel current, and averages sum-current to reduce measurement noise. $V_{ISENxP} – I_{SENxN}$ voltage represents current information at 5mV/A. Using the IOUT_CAL_OFFSET (39h) command to null out any offset current in Amps, and use MFR_IOUT_CAL_GAIN

(DEh) command to calibration for the READ_IOUT (8Ch) result by removing systematic errors related to board layout after assembly. Then the current value is stored in the READ_IOUT (8Ch) register.

The device continually digitizes the sensed the corresponding channel temperature from temperature output pin of SPS (TSEN), and averages it to reduce measurement noise. V_{TSEN} voltage represents temperature information at 8mV/°C + 0.6V. Then the current value is stored in the READ_TEMPERATURE_1 (8Dh) register.

Fault Protection Responses

Table 4 summarizes the various fault protections and associated responses.

Table 4. Fault Protection and Response Summary

FAULT or WARN	PMBus PROGRAMMING	FAULT RESPONSE	FET BEHAVIOR	ACTIVE DURING TON_RISE(+80us)	DURING ACTIVE Regulation	SMBALERT#	VR_READY
VIN UVLO	VIN_ON(35h) VIN_OFF(36h)	Shutdown	Both FETs off	Yes	Yes	Low (After VIN > VIN_ON)	Low
OVP	OV_FAULT _LIMIT(40h)	Latch-off	High-side FET is OFF, low-side FET response is configured by MFR_OV_Behavior[1:0]: OFF/ turn-on for soft-shutdown/ turn-on till VOUT=0V	Yes	Yes	Low	Low
		Restart	High-side FET is OFF, low-side FET response is configured by MFR_OV_Behavior[1:0]: OFF/ turn-on for soft-shutdown/ turn-on till VOUT=0V and then restart after 100ms +TON_DELAY			Low	Low
		Ignore	PWM maintains control of FETs			Low	High
UVP	UV_FAULT _LIMIT(44h)	Latch-off	Both FETs are off	No	Yes	Low	Low
		Restart	Both FETs are off, then restart after 100ms + TON_DELAY				
		Ignore	PWM maintains control of FETs			Low	High
SLOW_OCP	IOUT_SLOW_OC _FAULT_LIMIT(46h)	Latch-off	Both FETs are off	No	Yes	Low	Low
		Restart	Both FETs are off, then restart after 100ms + TON_DELAY				
		Ignore	PWM maintains control of FETs			Low	High
FAST_OCP	IOUT_FAST_OC _FAULT_LIMIT (D6h[3:2])	Latch-off	Both FETs are off	Yes	Yes	Low	Low
		Restart	Both FETs are off, then restart after 100ms + TON_DELAY				

FAULT or WARN	PMBus PROGRAMMING	FAULT RESPONSE	FET BEHAVIOR	ACTIVE DURING TON_RISE(+80us)	DURING ACTIVE Regulation	SMBALERT#	VR_READY
		Ignore	PWM maintains control of FETs			Low	High
OTP	OT_FAULT _LIMIT(4Fh)	Latch-off	Both FETs are off	Yes	Yes	Low	Low
		Restart	Both FETs are off, then restart after 100ms + TON_DELAY & OTP<"OTP_FAULT_LIMIT-15 degree"				
		Ignore	PWM maintains control of FETs			Low	High
OT _WARNING	OT_WARN _LIMIT(51h)	VR_HOT# assert	PWM maintains control of FETs	Yes	Yes	Low	High
SPS FAULT	X	Restart	Both FETs are off, then restart after 100ms + TON_DELAY & SPS_FAULT=L	Yes	Yes	Low	Low

PMBus Operation

The RTQ8825 PMBus slave address is pin selectable using the SET1 and SETA1 pin and resistor value described in Table 2. For the RTQ8825, pages 0x00 and 0x01 correspond to rail A and rail B, respectively, in this device. The PMBus slave address is the 7-bit format addresses. The PMBus data formats follow PMBus specification version 1.3.

PMBus Protocol

PMBus Packet Protocol Diagram Element Key

S: Start Condition

A: Acknowledge (“0”)

NA: Not Acknowledge (“1”)

Rd: Read (“1”)

Wr: Write (“0”) Send Byte Protocol

Sr: Repeated Start Condition

PEC: Packet Error Checking

P: Stop Condition

■ Slave to Master

□ Master to Slave

Send Byte Protocol

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	PEC	A	P

Write Byte Protocol

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	PEC	A	P

Write Word Protocol

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Low Data Byte	A	High Data Byte	A	PEC	A	P

Read Byte Protocol

1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A

1	7	1	1	8	1	8	1	1
Sr	Slave Address	Rd	A	Data Byte	A	PEC	A	P

Read Word Protocol

1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A

1	7	1	1	8	1	8	1	8	1	1
Sr	Slave Address	Rd	A	Low Data Byte	A	High Data Byte	A	PEC	A	P

Block Read Protocol

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count=N	A

8	1	8	1	8	1		8	1	8	1	1
Data Byte 1	A	Data Byte 2	A	Data Byte 3	A	…	Data Byte N	A	PEC	NA	P

Alert Response Address (ARA) Protocol

1	7	1	1	8	1	8	1	1
S	ARA	Rd	A	Device Address	A	PEC	NA	P

Supported PMBus Commands

Command Code/Name		Description	Type	PAGED	Default Value	NVM
00h	PAGE	Channel or page currently selected for any command that supports paging.	R/W Byte	No	0x00	No
01h	OPERATION	Operating mode control.	R/W Byte	Yes	0x00	Yes
02h	ON_OFF_CONFIG	EN pin and PMBus bus on/off command configuration.	R/W Byte	Yes	0x16	Yes
03h	CLEAR_FAULTS	Clears all fault status registers to 0x00 and releases SMBALERT#.	Send Byte	Yes	N/A	No
10h	WRITE_PROTECT	Level of protection provided by the device against accidental changes.	R/W Byte	No	0x00	Yes
15h	STORE_USER_ALL	Stores all current storable register settings into EEPROM as new defaults.	Send Byte	No	N/A	No
16h	RESTORE_USER_ALL	Restores all storable register settings from EEPROM.	Send Byte	No	N/A	No
19h	CAPABILITY	Summary of PMBus optional communication protocols supported by this device.	R Byte	No	0xD0	No
20h	VOUT_MODE	Output voltage format and exponent. (linear, exponent = -9)	R Byte	Yes	0x17	No
21h	VOUT_COMMAND	Nominal output voltage set point.	R/W Word	Yes	Initial VBOOT	No
24h	VOUT_MAX	Sets the maximum output voltage.	R/W Word	Yes	0x0308 (1.516V)	Yes
27h	VOUT_TRANSITION_RATE	The rate of output voltage changes when VOUT commanded to a new value.	R/W Word	Yes	0xD040 (1mV/us)	Yes
2Bh	VOUT_MIN	Sets the minimum output voltage.	R/W Word	Yes	0x0080 (0.25V)	Yes
35h	VIN_ON	Sets value of input voltage at which the device should start power conversion.	R/W Word	No	0xD0B4 (2.8V)	Yes
36h	VIN_OFF	Sets value of input voltage at which the device should stop power conversion.	R/W Word	No	0xD087 (2.1V)	Yes
39h	IOUT_CAL_OFFSET	The IOUT_CAL_OFFSET command is used to compensate for offset errors in the READ_IOUT results and IOUT_SLOW_OC_FAULT_LIMIT & IOUT_FAST_OC_FAULT_LIMIT.	R/W Word	Yes	0x0000 (0A)	Yes
40h	VOUT_OV_FAULT_LIMIT	Output overvoltage fault limit.	R/W Word	Yes	0x03B2 (1.8V)	Yes
41h	VOUT_OV_FAULT_RESPONSE	Sets response to output overvoltage faults to latch-off, hiccup mode or ignore.	R/W Byte	Yes	0xB9	Yes
44h	VOUT_UV_FAULT_LIMIT	Output under-voltage fault limit	R/W Word	Yes	0x00B2 (0.3V)	Yes
45h	VOUT_UV_FAULT_RESPONSE	Sets response to output under-voltage faults to latch-off, hiccup mode or ignore.	R/W Byte	Yes	0xB9	Yes
46h	IOUT_SLOW_OC_FAULT_LIMIT	Output slow over-current fault limit.	R/W Word	Yes	Page 0 : 0x0070 (112A) Page 1 : 0x0055 (85A)	Yes
47h	IOUT_SLOW_OC_FAULT_RESPONSE	Sets response to output slow over-current faults to latch-off, hiccup mode or ignore.	R/W Byte	Yes	0xB9	Yes
4Fh	OT_FAULT_LIMIT	Sets the value of the sensed temperature that causes an over-temperature fault condition.	R/W Word	Yes	0x0082 (130°C)	Yes
50h	OT_FAULT_RESPONSE	Sets response to over temperature faults to latch-off, hiccup mode or ignore.	R/W Byte	Yes	0xB9	Yes

Command Code/Name		Description	Type	PAGED	Default Value	NVM
51h	OT_WARN_LIMIT	Sets the value of the sensed temperature that causes an over-temperature warning condition. If temperature rise above warning condition and then VR_HOT# asserts low.	R/W Word	Yes	0x0073 (115°C)	Yes
60h	TON_DELAY	Sets the turn-on delay.	R/W Word	Yes	0xF000 (0ms)	Yes
61h	TON_RISE	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Yes	0x0001 (1ms)	Yes
64h	TOFF_DELAY	Sets the turn-off delay.	R/W Word	Yes	0xF000 (0ms)	Yes
65h	TOFF_FALL	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Yes	0x0001 (1ms)	Yes
78h	STATUS_BYTE	Returns one byte summarizing of the most critical faults.	R Byte	Yes	Current status	No
79h	STATUS_WORD	Returns two bytes summarizing fault and warning conditions.	R Word	Yes	Current status	No
7Ah	STATUS_VOUT	Output voltage fault and warning status.	R/W Byte	Yes	Current status	No
7Bh	STATUS_IOUT	Output current fault and warning status.	R/W Byte	Yes	Current status	No
7Ch	STATUS_INPUT	Input supply fault and warning status.	R/W Byte	No	Current status	No
7Dh	STATUS_TEMPERATURE	Temperature fault and warning status.	R/W Byte	Yes	Current status	No
7Eh	STATUS_CML	Communication and memory fault and warning status.	R/W Byte	No	Current status	No
80h	STATUS_MFR_SPECIFIC	Manufacturer specific fault and state information.	R/W Byte	Yes	Current status	No
8Bh	READ_VOUT	Returns the output voltage in volts.	R Word	Yes	Current status	No
8Ch	READ_IOUT	Returns the output current in amps.	R Word	Yes	Current status	No
8Dh	READ_TEMPERATURE_1	Returns the temperature in degrees Celsius.	R Word	Yes	Current status	No
98h	PMBUS_REVISION	PMBus revision supported by this device. Current revision is 1.3.	R Byte	No	0x33	No
99h	MFR_ID	The manufacturer ID	R Block	No	0x1214	No
ADh	IC_DEVICE_ID	The IC device identification	R Block	No	0x8825	No
AEh	IC_DEVICE_REV	The IC device revision	R Block	No	0x00	No
D0h	MFR_PH1_Current_Balance_Gain	Sets phase1 current balance gain.	R/W Byte	Yes	0x04 (100%)	Yes
D1h	MFR_PH2_Current_Balance_Gain	Sets phase2 current balance gain.	R/W Byte	Yes	0x04 (100%)	Yes
D2h	MFR_PH3_Current_Balance_Gain	Sets phase3 current balance gain.	R/W Byte	No	0x04 (100%)	Yes
D6h	MFR_ IOUT_FAST_OC_FAULT_LIMIT & SLOW_OCDLY	The IOUT_FAST_OC_FAULT_LIMIT command sets the value of the pre-phase output current, in Amps, that causes an fast over-current fault condition. Sets SLOW_OC delay time. The controller ignore/latched shutdown/hiccup shutdown if output current exceeds IOUT_SLOW_OC_FAULT_LIMIT for SLOW_OC delay time.	R/W Byte	Yes	0x05 (60A, 32us)	Yes
D7h	MFR_Kton_frequency	Sets switching frequency (kton). Total PWMs Frequency < 3.6MHz.	R/W Byte	Yes	0x04 (1)	Yes

Command Code/Name		Description	Type	PAGED	Default Value	NVM
D8h	MFR_AQR	Sets adaptive quick response threshold for load-line > 0mΩ and QR width maximum.	R/W Byte	Yes	0x00	Yes
D9h	MFR_VR_HOT_Hys	Sets VR_HOT# hysteresis. If temperature drops below OT warning condition minus hysteresis and then VR_HOT# de-asserts.	R/W Byte	No	0x01 (6°C)	Yes
DAh	MFR_RESET_RESPONSE_Rail_Fault_Mode	Sets VOUT behavior when RESET# assert. Sets the behavior when the channel has fault.	R/W Byte	No	0x01	Yes
DBh	MFR_OV_Behavior	Sets PWM behavior during OVP. Hi-Z, turn-on the low side or soft shutdown	R/W Byte	Yes	0x00	Yes
DCh	MFR_DVS_Compensate	Sets DVS compensate.	R/W Byte	Yes	0x01	Yes
DDh	MFR_Load_Line	Sets Ai-gain for load line.	R/W Byte	Yes	0x03 (1)	Yes
DEh	MFR_IOUT_CAL_GAIN	The MFR_IOUT_CAL_GAIN command is used to compensate for gain errors in the READ_IOUT results and IOUT_SLOW_OC_FAULT_LIMIT & IOUT_FAST_OC_FAULT_LIMIT.	R/W Byte	Yes	0x00 (0%)	Yes
DFh	MFR_ABS_QR	Sets quick response threshold for no load-line.	R/W Byte	Yes	0x00	Yes
E0h	MFR_VOUT_RPT_GAIN	The MFR_VOUT_RPT_GAIN command is used to compensate for gain errors in the READ_VOUT results.	R/W Byte	Yes	0x00 (0%)	Yes
E1h	MFR_IOUT_FAST_OC_FAULT_RESPONSE	Sets response to output fast over-current faults to latch-off, hiccup mode or ignore.	R/W Byte	Yes	0xB9	Yes

Command Code: 00h Description: The PAGE command provides the ability to configure, control and monitor multiple PWM channels through only one physical address. Each PAGE contains the operating commands for one PWM channel.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PAGE							
Default Value	0x00h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:0]	Channel	[7:0] = 00h: rail A [7:0] = 01h: rail B [7:0] = FFh: All rail All other combinations are not defined.

Command Code: 01h Description: The OPERATION command is issued to turn on or off (enable or disable) in conjunction with the input from the EN pin. Faults will be cleared when output is commanded through the OPERATION command to turn off and then to turn back on.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OPERATION							
Default Value	0x00h							
Read/Write	RW	RW	R	R	R	R	R	R

Bits	Name	Description
[7]	ON/OFF State	[7] = 0: Off. [7] = 1: On. Vout is set to Initial Vboot or Vout Command.
[6]	Turn Off Behavior	[6] = 0: Immediately turn off the output when commanded off through OPERATION[7] [6] = 1: Soft Off. Use the programmed turnoff delay (TOFF_DELAY) and ramp down (TOFF_FALL) when commanded off through OPERATION[7]
[5:4]	Voltage Command Source	[5:4] = 00: VOUT_COMMAND All other combinations are not defined.
[3:0]	Reserved	Reserved

Command Code: 02h Description: The ON_OFF_CONFIG command configures the combination of EN pin input and serial bus commands needed to turn the unit on and off.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	ON_OFF_CONFIG							
Default Value	0x16h							
Read/Write	R	R	R	RW	RW	RW	RW	RW

Bits	Name	Description
[7:5]	Reserved	Reserved.
[4]	Power up	[4] = 0: Device powers up any time power is present regardless of state of the EN pin. [4] = 1: Device does not power up until commanded by the EN pin and OPERATION command as programmed in bits [3:0] of the ON_OFF_CONFIG register.
[3]	OPER_CMD	[3] = 0: Device ignores the “on” bit in the OPERATION command. [3] = 1: Device responds to the “on” bit in the OPERATION command.
[2]	EN_Response	[2] = 0: Device ignores the EN pin. Power conversion is controlled only by the OPERATION command. [2] = 1: Device requires the EN pin to be asserted to start the unit.
[1]	Polarity of the EN pin	[1] = 0: EN pin is active low. [1] = 1: EN pin is active high.
[0]	Turn off from EN pin	[0] = 0: Soft Off. Use the programmed turnoff delay (TOFF_DELAY) and ramp down (TOFF_FALL). [0] = 1: Immediately turn off the output.

Command Code: 03h Description: The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# pin signal output if the device is asserting the SMBALERT# pin signal.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CLEAR_FAULTS							
Default Value	N/A							
Read/Write	W	W	W	W	W	W	W	W

Note. The output is commanded through the EN pin, the OPERATION command, or the combined action of the EN pin and OPERATION command, to turn off and then to turn back on can also clear fault.

Command Code: 10h Description: The WRITE_PROTECT is used to control writing to the PMBus device. If a device receives a data byte that is not listed in [7:0] description, then the device shall treat this as invalid data.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	WRITE_PROTECT							
Default Value	0x00h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:0]	WRITE_PROTECT	[7:0] = 0x80h: Disable all writes except the WRITE_PROTECT command. [7:0] = 0x40h: Disable all writes except the WRITE_PROTECT, OPERATION, and PAGE commands. [7:0] = 0x20h: Disable all writes except the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands. [7:0] = 0x00h: Enable writes to all commands. All other combinations are not defined.

Command Code: 15h Description: The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store memory.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	STORE_USER_ALL							
Default Value	N/A							
Read/Write	W	W	W	W	W	W	W	W

Command Code: 16h Description: The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	RESTORE_USER_ALL							
Default Value	N/A							
Read/Write	W	W	W	W	W	W	W	W

Note. It is recommended that the output be disabled before issuing a RESTORE_USER_ALL command.

Command Code: 19h Description: The CAPABILITY command provides a way for the host system to determine some key capabilities of a PMBus device.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CAPABILITY							
Default Value	0xD0h							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7]	PEC	[7] = 1: Packet error checking is supported.
[6:5]	SPD	[6:5] = 10: Maximum supported bus speed is 1MHz.
[4]	ALRT	[4] = 1: Device does have a SMBALERT# pin and does support the SMBus alert response protocol
[3:0]	Reserved	Reserved

Command Code: 20h Description: The VOUT_MODE command, used for commanding and reading output voltage, consists of a three-bit Mode and a five-bit Parameter.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_MODE							
Default Value	0x17h							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:5]	Mode	[7:5] = 000: Linear mode.
[4:0]	Exponent	[4:0] = 10111: Exponent for linear mode values is –9 (equivalent of 1.953mV/count).

Command Code: 21h Description: The VOUT_COMMAND command sets the output voltage in volts.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_COMMAND															
Default Value	Initial VBOOT															
Read/Write	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Vout Range (V)		VOUT_COMMAND data valid range (decimal)														
0.25V to 1.516V		128(dec) to 776(dec). Vout(V) = [VOUT_COMMAND(dec) - 1] x 1.953mV, where VOUT_COMMAND(dec) is odd number. Vout(V) = [VOUT_COMMAND(dec)] x 1.953mV, where VOUT_COMMAND(dec) is even number.														

Command Code: 24h Description: The VOUT_MAX command sets the maximum output voltage. The purpose is to protect the devices on the output rail supplied by this device from a higher than acceptable output voltage.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_MAX															
Default Value	0x0308h															
Read/Write	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Vout Range (V)		VOUT_COMMAND data valid range (decimal)														
0.25V to 1.516V		128(dec) to 776(dec). Vout(V) = [VOUT_COMMAND(dec) - 1] x 1.953mV, where VOUT_COMMAND(dec) is odd number. Vout(V) = [VOUT_COMMAND(dec)] x 1.953mV, where VOUT_COMMAND(dec) is even number.														

Command Code: 27h Description: The VOUT_TRANSITION_RATE command sets the rate of change in mV/μs of any output voltage change during normal operation.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_TRANSITION_RATE															
Default Value	0xD040h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Bits		Name			Description											
[15:11]		Exponent			[15:11] = 11010: 2^(-6) = 0.015625											
[10:0]		VOUT_SR			[10:0] ≤ 0x040h, VOUT_TRANSITION rate is 1mV/us (default) 0x040h < [10:0] ≤ 0x100h, VOUT_TRANSITION rate is 4mV/us 0x100h < [10:0] ≤ 0x200h, VOUT_TRANSITION rate is 8mV/us 0x200h < [10:0], VOUT_TRANSITION rate is 16mV/us											

Command Code: 2Bh Description: The VOUT_MIN command sets the minimum output voltage. The purpose is to protect the devices on the output rail supplied by this device from a lower than acceptable output voltage.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_MIN															
Default Value	0x0080h															
Read/Write	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Vout Range (V)		VOUT_COMMAND data valid range (decimal)														
0.25V to 1.516V		128(dec) to 776(dec). Vout(V) = [VOUT_COMMAND(dec) - 1] x 1.953mV, where VOUT_COMMAND(dec) is odd number. Vout(V) = [VOUT_COMMAND(dec)] x 1.953mV, where VOUT_COMMAND(dec) is even number.														

Command Code: 35h Description: The VIN_ON command sets the input voltage in Volts, at which the unit should start power conversion. VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VIN_ON															
Default Value	0xD0B4h															
Read/Write	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW
Bits		Name				Description										
[15:11]		Exponent				[15:11] = 11010: 2^(-6) = 0.015625										
[10:0]		VIN_ON threshold				[10:0] ≤ 0x04Dh, VIN_ON threshold is 1.2V 0x04Dh < [10:0] ≤ 0x05Ah, VIN_ON threshold is 1.4V 0x05Ah < [10:0] ≤ 0x067h, VIN_ON threshold is 1.6V 0x067h < [10:0] ≤ 0x074h, VIN_ON threshold is 1.8V 0x074h < [10:0] ≤ 0x080h, VIN_ON threshold is 2.0V 0x080h < [10:0] ≤ 0x08Dh, VIN_ON threshold is 2.2V 0x08Dh < [10:0] ≤ 0x09Ah, VIN_ON threshold is 2.4V 0x09Ah < [10:0] ≤ 0x0A7h, VIN_ON threshold is 2.6V 0x0A7h < [10:0] ≤ 0x0B4h, VIN_ON threshold is 2.8V (default) 0x0B4h < [10:0], VIN_ON threshold is 3.0V										

Command Code: 36h Description: The VIN_OFF command sets the input voltage in Volts, at which the unit should stop power conversion. VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VIN_OFF															
Default Value	0xD087h															
Read/Write	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 11010: 2^(-6) = 0.015625
[10:0]	VIN_OFF threshold	[10:0] ≤ 0x047h, VIN_OFF threshold is 1.1V 0x047h < [10:0] ≤ 0x054h, VIN_OFF threshold is 1.3V 0x054h < [10:0] ≤ 0x060h, VIN_OFF threshold is 1.5V 0x060h < [10:0] ≤ 0x06Dh, VIN_OFF threshold is 1.7V 0x06Dh < [10:0] ≤ 0x07Ah, VIN_OFF threshold is 1.9V 0x07Ah < [10:0] ≤ 0x087h, VIN_OFF threshold is 2.1V (default) 0x087h < [10:0] ≤ 0x094h, VIN_OFF threshold is 2.3V 0x094h < [10:0] ≤ 0x0A0h, VIN_OFF threshold is 2.5V 0x0A0h < [10:0] ≤ 0x0ADh, VIN_OFF threshold is 2.7V 0x0ADh < [10:0], VIN_OFF threshold is 2.9V

Command Code: 39h Description: The IOUT_CAL_OFFSET command is used to null out any offset current in Amps.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_CAL_OFFSET															
Default Value	0x0000h															
Read/Write	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	IOUT_CAL_OFFSET	IOUT offset = [10:0] x 2^0, MSB(bit10) is programmable with sign, next 6 bits are sign extend only. Lower four bits are programmable with a default value of 0.

Command Code: 40h Description: The VOUT_OV_FAULT_LIMIT command sets the value of the average sensed output voltage in Volts that causes a "fixed" over-voltage fault.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_OV_FAULT_LIMIT															
Default Value	0x03B2h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Reserved	Reserved
[10:0]	VOUT_OV_FAULT_LIMIT	[10:0] ≤ 0x132h, VOUT OV threshold is 0.55V 0x132h < [10:0] ≤ 0x14Ch, VOUT OV threshold is 0.60V 0x14Ch < [10:0] ≤ 0x165h, VOUT OV threshold is 0.65V 0x165h < [10:0] ≤ 0x17Fh, VOUT OV threshold is 0.70V 0x17Fh < [10:0] ≤ 0x199h, VOUT OV threshold is 0.75V 0x199h < [10:0] ≤ 0x1B2h, VOUT OV threshold is 0.80V 0x1B2h < [10:0] ≤ 0x1CCh, VOUT OV threshold is 0.85V 0x1CCh < [10:0] ≤ 0x1E5h, VOUT OV threshold is 0.90V 0x1E5h < [10:0] ≤ 0x1FFh, VOUT OV threshold is 0.95V 0x1FFh < [10:0] ≤ 0x219h, VOUT OV threshold is 1.00V 0x219h < [10:0] ≤ 0x232h, VOUT OV threshold is 1.05V 0x232h < [10:0] ≤ 0x24Ch, VOUT OV threshold is 1.10V 0x24Ch < [10:0] ≤ 0x265h, VOUT OV threshold is 1.15V 0x265h < [10:0] ≤ 0x27Fh, VOUT OV threshold is 1.20V 0x27Fh < [10:0] ≤ 0x299h, VOUT OV threshold is 1.25V 0x299h < [10:0] ≤ 0x2B2h, VOUT OV threshold is 1.30V 0x2B2h < [10:0] ≤ 0x2CCh, VOUT OV threshold is 1.35V 0x2CCh < [10:0] ≤ 0x2E5h, VOUT OV threshold is 1.40V 0x2E5h < [10:0] ≤ 0x2FFh, VOUT OV threshold is 1.45V 0x2FFh < [10:0] ≤ 0x319h, VOUT OV threshold is 1.50V 0x319h < [10:0] ≤ 0x332h, VOUT OV threshold is 1.55V 0x332h < [10:0] ≤ 0x34Ch, VOUT OV threshold is 1.60V 0x34Ch < [10:0] ≤ 0x365h, VOUT OV threshold is 1.65V 0x365h < [10:0] ≤ 0x37Fh, VOUT OV threshold is 1.70V 0x37Fh < [10:0] ≤ 0x399h, VOUT OV threshold is 1.75V 0x399h < [10:0] ≤ 0x3B2h, VOUT OV threshold is 1.80V (default) 0x3B2h < [10:0] ≤ 0x3CCh, VOUT OV threshold is 1.85V 0x3CCh < [10:0] ≤ 0x3E5h, VOUT OV threshold is 1.90V 0x3E5h < [10:0] ≤ 0x3FFh, VOUT OV threshold is 1.95V 0x3FFh < [10:0] ≤ 0x419h, VOUT OV threshold is 2.00V 0x419h < [10:0] ≤ 0x432h, VOUT OV threshold is 2.05V 0x432h < [10:0], VOUT OV threshold is 2.10V

Command Code: 41h Description: The VOUT_OV_FAULT_RESPONSE command sets the response type to an output over voltage fault.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_OV_FAULT_RESPONSE							
Default Value	0xB9h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:6]	Response	[7:6] = 00: No shutdown (ignore fault response mode) [7:6] = 10: The device shuts down and responds according to the retry setting in bits [5:3]. All other combinations are not defined.
[5:3]	Retry setting	[5:0] = 000 000: Latched shutdown [5:0] = 111 001: Hiccup shutdown, retry delay time is 100ms + TON_DELAY. All other combinations are not defined.
[2:0]	Retry delay time	

Command Code: 44h Description: The VOUT_UV_FAULT_LIMIT command sets the value of the average sensed output voltage in Volts that causes a "fixed" under-voltage fault.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_UV_FAULT_LIMIT															
Default Value	0x00B2h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Reserved	Reserved
[10:0]	VOUT_UV_FAULT_LIMIT	[10:0] ≤ 0x099h, VOUT UV is disabled 0x099h < [10:0] ≤ 0x0B2h, VOUT UV threshold is 0.30V (default) 0x0B2h < [10:0] ≤ 0x0CCh, VOUT UV threshold is 0.35V 0x0CCh < [10:0] ≤ 0x0E5h, VOUT UV threshold is 0.40V 0x0E5h < [10:0] ≤ 0x0FFh, VOUT UV threshold is 0.45V 0x0FFh < [10:0] ≤ 0x119h, VOUT UV threshold is 0.50V 0x119h < [10:0] ≤ 0x132h, VOUT UV threshold is 0.55V 0x132h < [10:0] ≤ 0x14Ch, VOUT UV threshold is 0.60V 0x14Ch < [10:0] ≤ 0x165h, VOUT UV threshold is 0.65V 0x165h < [10:0] ≤ 0x17Fh, VOUT UV threshold is 0.70V 0x17Fh < [10:0] ≤ 0x199h, VOUT UV threshold is 0.75V 0x199h < [10:0] ≤ 0x1B2h, VOUT UV threshold is 0.80V 0x1B2h < [10:0] ≤ 0x1CCh, VOUT UV threshold is 0.85V 0x1CCh < [10:0] ≤ 0x1E5h, VOUT UV threshold is 0.90V 0x1E5h < [10:0] ≤ 0x1FFh, VOUT UV threshold is 0.95V 0x1FFh < [10:0], VOUT UV threshold is 1.00V

Command Code: 45h Description: The VOUT_UV_FAULT_RESPONSE command sets the response type to an output under-voltage fault.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_UV_FAULT_RESPONSE							
Default Value	0xB9h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:6]	Response	[7:6] = 00: No shutdown (ignore fault response mode) [7:6] = 10: The device shuts down and responds according to the retry setting in bits [5:3]. All other combinations are not defined.
[5:3]	Retry setting	[5:0] = 000 000: Latched shutdown [5:0] = 111 001: Hiccup shutdown, retry delay time is 100ms + TON_DELAY. All other combinations are not defined.
[2:0]	Retry delay time	

Command Code: 46h Description: The IOUT_SLOW_OC_FAULT_LIMIT command sets the value of the output current, in Amps, that causes an over-current fault condition.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_SLOW_OC_FAULT_LIMIT															
Default Value	Page 0: 0x0070h Page 1: 0x0055h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	IOUT_SLOW_ OC_FAULT_LIMIT	$Iout_{(Slow\_OCth)}$ = [10:0] x 2^(0) Range = 30A to 360A

Command Code: 47h Description: The IOUT_SLOW_OC _FAULT_RESPONSE command sets the response type to an over-current fault.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_SLOW_OC_FAULT_RESPONSE							
Default Value	0xB9h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:6]	Response	[7:6] = 00: No shutdown (ignore fault response mode) [7:6] = 10: The device shuts down and responds according to the retry setting in bits [5:3]. All other combinations are not defined.
[5:3]	Retry setting	[5:0] = 000 000: Latched shutdown [5:0] = 111 001: Hiccup shutdown, retry delay time is 100ms + TON_DELAY. All other combinations are not defined.
[2:0]	Retry delay time	

Command Code: 4Fh Description: The OT_FAULT_LIMIT command sets the value of the external sense temperature, in °C, that causes an over-temperature fault.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OT_FAULT_LIMIT															
Default Value	0x0082h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	OT_FAULT_LIMIT	$TEMP_{(OTth)}$ = [10:0] x 2^(0) Range = 75°C to 165°C

Command Code: 50h Description: The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an over-temperature fault.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OT_FAULT_RESPONSE							
Default Value	0xB9h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:6]	Response	[7:6] = 00: No shutdown (ignore fault response mode) [7:6] = 10: The device shuts down and responds according to the retry setting in bits [5:3]. All other combinations are not defined.
[5:3]	Retry setting	[5:0] = 000 000: Latched shutdown [5:0] = 111 001: Hiccup shutdown, retry delay time is 100ms + TON_DELAY. All other combinations are not defined.
[2:0]	Retry delay time	

Command Code: 51h Description: The OT_WARN_LIMIT command sets the value of the external sense temperature in °C, that causes an over-temperature warning. If temperature rises above warning condition and then VR_HOT# asserts low.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OT_WARN_LIMIT															
Default Value	0x0073h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	OT_WARN_LIMIT	$TEMP_{(OTth)}$ = [10:0] x 2^(0) Range = 75°C to 165°C

Command Code: 60h
Description: The TON_DELAY command sets the time in milliseconds, from when a start condition is received until the output voltage starts to rise.

Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TON_DELAY															
Default Value	0xF000h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 11110: 2^(-2) = 0.25
[10:0]	TON_DELAY	Ton_DT = [10:0] x 2^(-2) Range = 0ms to 51ms

Command Code: 61h
Description: The TON_RISE command sets the time in milliseconds, from when the output starts to rise until the output voltage has entered the regulation band.

Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TON_RISE															
Default Value	0x0001h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	TON_RISE	Trise = [10:0] x 2^(0) Range = 1ms to 10ms

Command Code: 64h
Description: The TOFF_DELAY command sets the time in milliseconds, from when a stop condition is received and when the output voltage starts to fall.

Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TOFF_DELAY															
Default Value	0xF000h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 11110: 2^(-2) = 0.25
[10:0]	TOFF_DELAY	Toff_DT = [10:0] x 2^(-2) Range = 0ms to 51ms

Command Code: 65h
Description: The TOFF_FALL command sets the time in milliseconds, from when a stop condition is received and when the output voltage starts to fall.

Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TOFF_FALL															
Default Value	0x0001h															
Read/Write	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	TOFF_FALL	Tfall = [10:0] x 2^(0) Range = 1ms to 10ms

Command Code: 78h Description: The STATUS_BYTE command returns one byte of information with a summary of the most critical faults.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		STATUS_BYTE							
Default Value		current status							
Read/Write		R	R	R	R	R	R	R	R
Bits	Name			Description					
[7]	BUSY			Not supported					
[6]	OFF			This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. (EN=L, OPERATION=L, rail disable)					
[5]	VOUT_OV_FAULT			An output over-voltage fault has occurred.					
[4]	IOUT_OC_FAULT			An output over-current fault has occurred.					
[3]	VIN_UV_FAULT			Not supported					
[2]	TEMPERATURE			A temperature fault or warning has occurred.					
[1]	CML			A communications, memory or logic fault has occurred.					
[0]	NONE_OF_THE_ ABOVE			A fault or warning not listed in bits [7:1] has occurred. VOUT_UV_FAULT, IOUT_FAST_OC_FAULT, SPS_FAULT, VOUT_MAX_MIN_Warning)					

Command Code: 79h Description: The STATUS_WORD command returns two bytes of information with a summary of the units fault condition.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	STATUS_WORD															
Default Value	current status															
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
[15]	VOUT	An output voltage fault has occurred.
[14]	IOUT	An output current fault has occurred.
[13]	INPUT	An input voltage fault has occurred.
[12]	MFRSPECIFIC	A manufacturer specific fault has occurred. (IOUT_FAST_OC_FAULT, SPS_FAULT)
[11]	PG_STATUS#	The VR_Ready signal, if present, is negated.
[10]	FANS	Not supported
[9]	OTHER	Not supported
[8]	UNKNOWN	Not supported
[7]	BUSY	Not supported
[6]	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
[5]	VOUT_OV_FAULT	An output over-voltage fault has occurred.
[4]	IOUT_OC_FAULT	An output over-current fault has occurred.
[3]	VIN_UV_FAULT	Not supported
[2]	TEMPERATURE	A temperature fault or warning has occurred.
[1]	CML	A communications, memory or logic fault has occurred.
[0]	NONE_OF_THE_ ABOVE	A fault or warning not listed in bits [7:1] has occurred. (VOUT_UV_FAULT, IOUT_FAST_OC_FAULT, SPS_FAULT, VOUT_MAX_MIN_Warning)

Command Code: 7Ah Description: The STATUS_VOUT command returns one byte of information relating to the status of the output voltage related faults.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	STATUS_VOUT							
Default Value	current status							
Read/Write	RW	R	R	RW	RW	R	R	R

Bits	Name	Description
[7]	VOUT_OV_FAULT	Output over-voltage fault. This bit is writeable 1b to clear.
[6]	VOUT_OV_WARNING	Not supported
[5]	VOUT_UV_WARNING	Not supported
[4]	VOUT_UV_FAULT	Output under-voltage fault. This bit is writeable 1b to clear.
[3]	VOUT_MAX_MIN WARNING	An attempt is made to program the VOUT_COMMAND in excess of the value in VOUT_MAX or under the value in VOUT_MIN. This bit is writeable 1b to clear.
[2]	TON_MAX_FAULT	Not supported
[1]	TOFF_MAX_WARNING	Not supported
[0]	VOUT Tracking Error	Not supported

Command Code: 7Bh Description: The STATUS_IOUT command returns one byte of information relating to the status of the output current related faults.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	STATUS_IOUT							
Default Value	current status							
Read/Write	RW	R	R	R	R	R	R	R

Bits	Name	Description
[7]	SLOW_OC_FAULT	Output Slow Over-current Fault. This bit is writeable 1b to clear.
[6]	OC_LV_FAULT	Not supported
[5]	OC_WARNING	Not supported
[4]	UC_FAULT	Not supported
[3]	Current Share Fault	Not supported
[2]	In Power Limiting Mode	Not supported
[1]	POUT_OP_FAULT	Not supported
[0]	POUT_OP_WARNING	Not supported

Command Code: 7Ch **Description**: The STATUS_INPUT command returns one byte of VIN status information.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		STATUS_INPUT							
Default Value		Current status							
Read/Write		R	R	R	R	R/W	R	R	R
Bits	**Name**		**Description**						
[7]	VIN_OV_FAULT		Not supported						
[6]	VIN_OV_WARNING		Not supported						
[5]	VIN_UV_WARNING		Not supported						
[4]	VIN_UV_FAULT		Not supported						
[3]	Unit Off for Insufficient Input Voltage		The unit is off because of insufficient input voltage. The bit is set to 1 when the unit powers up and stays until the first time VIN exceeds VIN_ON. During the initial power up, the bit is not latched and does not trigger SMBALERT#. Once VIN exceeds VIN_ON for the first time, the bit will be latched at any subsequent VIN < VIN_OFF events, and the SMBALERT# will be triggered. This bit is writeable 1b to clear.						
[2]	IIN_OC_FAULT		Not supported						
[1]	IIN_OC_WARNING		Not supported						
[0]	PIN_OP_WARNING		Not supported						

Command Code: 7Dh Description: The STATUS_TEMPERATURE command returns one byte of information relating to the status of the external temperature related faults.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		STATUS_ TEMPERATURE							
Default Value		current status							
Read/Write		RW	RW	R	R	R	R	R	R
Bits	Name		Description						
[7]	OT_FAULT		Over-temperature Fault. This bit is writeable 1b to clear.						
[6]	OT_WARNING		Over-temperature Warning. This bit is writeable 1b to clear.						
[5]	UT_WARNING		Not supported						
[4]	UT_FAULT		Not supported						
[3:0]	Reserved		Reserved						

Command Code: 7Eh Description: The STATUS_CML command returns one byte of information relating to the status of the communication-related faults of the converter.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	STATUS_CML							
Default Value	current status							
Read/Write	RW	RW	RW	RW	R	R	RW	R

Bits	Name	Description
[7]	IVC	Invalid or Unsupported Command Received. This bit is writeable to clear.
[6]	IVD	Invalid or Unsupported Data Received. This bit is writeable 1b to clear.
[5]	PEC	Packet Error Check Failed. This bit is writeable 1b to clear.
[4]	MEM	Memory Fault Detected. This bit is writeable 1b to clear.
[3]	PROC	Not supported
[2]	Reserved	Reserved
[1]	OTH	A communication fault other than the ones listed in this table has occurred.(MTP busy or upload/download in progress while PMBus attempted W/R). This bit is writeable 1b to clear.
[0]	Reserved	Reserved

Command Code: 80h Description: The STATUS_MFR_SPECIFIC commands returns one byte with the manufacturer specific status information.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	STATUS_MFR_SPECIFIC							
Default Value	current status							
Read/Write	R	R	R	R	R	R	RW	RW

Bits	Name	Description
[7:2]	Reserved	Reserved
[1]	IOUT_FAST_OC_FAULT	Output Fast Over-current Fault. This bit is writeable 1b to clear.
[0]	SPS_FAULT	Smart power stage fault. This bit is writeable 1b to clear.

Command Code: 8Bh Description: The READ_VOUT command returns the actual measured output voltage in the same format as set by the VOUT_MODE command																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	READ_VOUT															
Default Value	current status															
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
[15:0]	VOUT	VOUT = [15:0] x 2^{-9}

Command Code: 8Ch Description: The READ_IOUT command returns the average total output current in Amps.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	READ_IOUT															
Default Value	current status															
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	READ_IOUT	IOUT = [10:0] x 2^0

Command Code: 8Dh Description: The READ_TEMPERATURE_1 command returns the temperature in °C of the external sense element.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	READ_TEMPERATURE_1															
Default Value	current status															
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
[15:11]	Exponent	[15:11] = 00000: 2^(0) = 1
[10:0]	READ_TEMPERATURE_1	TEMP = [10:0] x 2^0, bit10 is sign bit (as part of two's complement).

Command Code: 98h Description: The PMBUS_REVISION command contains the revision of the PMBus to which the device is compliant.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PMBUS_REVISION							
Default Value	0x33h							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:4]	Part I Revision	[7:4] = 0011: (Rev 1.3)
[3:0]	Part II Revision	[3:0] = 0011: (Rev 1.3)

Command Code: 99h Description: The MFR_ID command indicates the manufacturer ID code is RT(Richtek).																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_ID															
Default Value	0x1214h															
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
[15:0]	MFR_ID	[15:0] = 0x1214h

Command Code: ADh Description: The IC_DEVICE_ID command indicates the device code is 8825 - code identifier for RTQ8825.																
Bits	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IC_DEVICE_ID															
Default Value	0x8825h															
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits	Name	Description
[15:0]	IC_DEVICE_ID	[15:0] = 0x8825h

Command Code: AEh Description: The IC_DEVICE_REV starts at 0 with the first silicon and is incremented with each subsequent silicon revision.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IC_DEVICE_REV							
Default Value	0x00h							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	IC_DEVICE_REV	The IC_DEVICE_REV starts at 0 with the first silicon and is incremented with each subsequent silicon revision.

Command Code: D0h Description: Adjustment phase1 current balance gain.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_PH1_Current_Balance_Gain							
Default Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	Name	Description
[7:3]	Reserved	Reserved
[2:0]	PH1 CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Command Code: D1h Description: Adjustment phase2 current balance gain.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_PH2_Current_Balance_Gain							
Default Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	Name	Description
[7:3]	Reserved	Reserved
[2:0]	PH2 CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Command Code: D2h Description: Adjustment phase3 current balance gain.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_PH3_Current_Balance_Gain							
Default Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	Name	Description
[7:3]	Reserved	Reserved
[2:0]	PH3 CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Command Code: D6h The IOUT_FAST_OC_FAULT_LIMIT command sets the value of the pre-phase output current, in Amps, that causes an fast over-current fault condition. Sets SLOW_OC delay time. The controller ignore/latched shutdown/hiccup shutdown if output current exceeds IOUT_ SLOW_OC_FAULT_LIMIT for SLOW_OC delay time.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_ IOUT_FAST_OC_FAULT_LIMIT & MFR_SLOW_OCDLY							
Default Value	0x05							
Read/Write	R	R	R	R	RW	RW	RW	RW

Bits	Name	Description
[7:4]	Reserved	Reserved
[3:2]	IOUT_FAST_OC_FAULT_LIMIT	Iout(Fast_OCth) = [3:2] = 00 : 50A, [3:2] = 01 : 60A(default), [3:2] = 10 : 70A, [3:2] = 11 : 80A.
[1:0]	SLOW_OC_DLY_Time	[1:0] = 00 : 20us, [1:0] = 01 : 32us (default), [1:0] = 10 : 44us, [1:0] = 11 : 56us

Command Code: D7h Description: Sets Kton(switching frequency). The high switching frequency range is 550kHz ~ 1MHz, and the low switching frequency range is 220kHz ~ 500kHz.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_Kton							
Default Value	0x04h							
Read/Write	R	R	R	R	RW	RW	RW	RW

Bits	Name	Description
[7:2]	Reserved	Reserved
[3:0]	KTON_freq	On-time (TON) K Factor Setting for high switching frequency [3:0] = 08h : 1.73, [3:0] = 09h : 1.91, [3:0] = 0Ah : 2.09, [3:0] = 0Bh : 2.27, [3:0] = 0Ch : 2.45, [3:0] = 0Dh : 2.82, [3:0] = 0Eh : 3.18, [3:0] = 0Fh : 3.55 On-time (TON) K Factor Setting for low switching frequency [3:0] = 00h : 0.64, [3:0] = 01h : 0.73, [3:0] = 02h : 0.82, [3:0] = 03h : 0.91, [3:0] = 04h : 1.00 (default), [3:0] = 05h : 1.18, [3:0] = 06h : 1.36, [3:0] = 07h : 1.55

Command Code: D8h Description: Sets adaptive quick response threshold for load-line > 0mΩ and QR width maximum.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_AQR							
Default Value	0x00h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	R

Bits	Name	Description
[7:3]	AQR_TH	AQR Starting Trigger Threshold AQR_TH = [7:3] x 72mV, except [7:3]=00000 is disable.
[2:1]	QR_WD_MAX	QR Width Maximum [2:1] = 00 : 60%*TON (default), 01 : 80%*TON, 10 : 120%*TON, 11 : 160%*TON
[0]	Reserved	Reserved

Command Code: D9h Description: Sets VR_HOT# hysteresis. If temperature drops below OT warning condition minus hysteresis and then VR_HOT# de-asserts.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_VR_HOT_Hys							
Default Value	0x01h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	Name	Description
[7:3]	Reserved	Reserved
[2:0]	VR_HOT# hysteresis	[2:0] = 000 : 3°C, [2:0] = 001 : 6°C (default), [2:0] = 010 : 9°C, [2:0] = 011 : 12°C, [2:0] = 100 : 15°C, [2:0] = 101 : 18°C, [2:0] = 110 : 21°C, [2:0] = 111 : 24°C

Command Code: DAh Description: Sets VOUT behavior when RESET# asserts. Sets the behavior when the channel has fault.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_RESET_RESPONSE_Rail_Fault_Mode							
Default Value	0x01h							
Read/Write	R	R	R	R	R	R	RW	RW

Bits	Name	Description
[7:2]	Reserved	Reserved
[1]	Reset# pin response	[1] = 0: When the RESET# pin is asserted low, after a short delay (greater than 2μs), the output voltage begins to transition from the current value to the VBOOT value according to the slew-rate set in the VOUT_TRANSITION_RATE command. [1] = 1: When the RESET# pin is asserted low, after a short delay (greater than 2μs), both channels are restarted.
[0]	Channel fault mode	[0] = 0: All channel shutdown [0] = 1: Just only fault channel shutdown (default)

Command Code: DBh Description: Sets OV behavior.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MFR_OV_Behavior							
Default Value		0x00h							
Read/Write		R	R	R	R	R	R	RW	RW
Bits	Name		Description						
[7:2]	Reserved		Reserved						
[1:0]	OV behavior		[1:0] = 00 : HiZ shutdown (default), [1:0] = 01 : Soft-shutdown, [1:0] = 10 : Turn on the low-side MOSFET [1:0] = 11 : Reserved						

Command Code: DCh Description: Sets DVS compensate.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MFR_DVS_Compensate							
Default Value		0x01h							
Read/Write		R	R	R	R	R	R	RW	RW
Bits	Name		Description						
[7:2]	Reserved		Reserved						
[1:0]	DVS compensate		[1:0] = 00 : Disable **While VOUT_TRANSITION rate is 1mV/us :** [1:0] = 01 : 0.625uA, [1:0] = 10 : 1.25uA, [1:0] = 01: 2.5uA **While VOUT_TRANSITION rate is 4mV/us :** [1:0] = 01 : 1.25uA, [1:0] = 10 : 2.5uA, [1:0] = 01: 5uA **While VOUT_TRANSITION rate is 8mV/us :** [1:0] = 01 : 2.5uA, [1:0] = 10 : 5uA, [1:0] = 01: 10uA **While VOUT_TRANSITION rate is 16mV/us :** [1:0] = 01 : 5uA, [1:0] = 10 : 10uA, [1:0] = 01: 20uA						

Command Code: DDh Description: Sets Ai-gain for LL.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MFR_Load_Line							
Default Value		0x03h							
Read/Write		R	R	R	R	R	R	RW	RW
Bits	Name		Description						
[7:2]	Reserved		Reserved						
[1:0]	Ai-gain		[1:0] = 00 : 0.25, [1:0] = 01 : 0.50, [1:0] = 10 : 0.75, [1:0] = 11 : 1.00 (default)						

Command Code: DEh Description: Sets IOUT gain calibration for the READ_IOUT result and the IOUT_SLOW_OC_FAULT_LIMIT & IOUT_FAST_OC_FAULT_LIMIT..									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MFR_IOUT_CAL_GAIN							
Default Value		0x00h							
Read/Write		R	R	R	R	RW	RW	RW	RW
Bits	Name			Description					
[7:4]	Reserved			Reserved					
[3:0]	IOUT gain			[3:0] = 0h : 0% (default), [3:0] = 1h : 0.78%, [3:0] = 2h : 1.56%, [3:0] = 3h : 2.34%, [3:0] = 4h : 3.13%, [3:0] = 5h : 3.91%, [3:0] = 6h : 4.69%, [3:0] = 7h : 5.47%, [3:0] = 8h : -6.25%, [3:0] = 9h : -5.47%, [3:0] = Ah : -4.69%, [3:0] = Bh : -3.91%, [3:0] = Ch : -3.13%, [3:0] = Dh : -2.34%, [3:0] = Eh : -1.56%, [3:0] = Fh : -0.78%					

Command Code: DFh **Description**: Sets absolutely quick response threshold for no load-line.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MFR_ABS_QR							
Default Value		0x00h							
Read/Write		RW	RW	RW	R	R	R	R	R
Bits	**Name**			**Description**					
[7:5]	ABS_QR_TH			**ABS_QR Starting Trigger Threshold** ABS_QR_TH = 15mV + [7:5] x 5mV, except [7:5]=000 is disable.					
[4:0]	Reserved			Reserved					

Command Code: E0h **Description**: Sets VOUT_RPT gain calibration for the READ_VOUT result.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MFR_VOUT_RPT_GAIN							
Default Value		0x00h							
Read/Write		R	R	R	R	R	RW	RW	RW
Bits	**Name**			**Description**					
[7:3]	Reserved			Reserved					
[2:0]	VOUT_RPT gain			[2:0] = 000 : 0% (default), [2:0] = 001 : -2.34%, [2:0] = 010 : -4.68%, [2:0] = 011 : -7.02%, [2:0] = 100 : -9.36%, [2:0] = 101 : -11.7%, [2:0] = 110 : -14.04%, [2:0] = 111 : -16.38%					

Command Code: E1h
Description: The MFR_IOUT_ FAST_OC _FAULT_RESPONSE command sets the response type to an over-current fault.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MFR_IOUT_ FAST_OC_FAULT_RESPONSE							
Default Value	0xB9h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:6]	Response	[7:6] = 00: No shutdown (ignore fault response mode) [7:6] = 10: The device shuts down and responds according to the retry setting in bits [5:3]. All other combinations are not defined.
[5:3]	Retry setting	[5:0] = 000 000: Latched shutdown [5:0] = 111 001: Hiccup shutdown, retry delay time is 100ms + TON_DELAY. All other combinations are not defined.
[2:0]	Retry delay time	

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-48L 7x7 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (26.5°C/W) = 3.77W for a WQFN-48L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 23 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

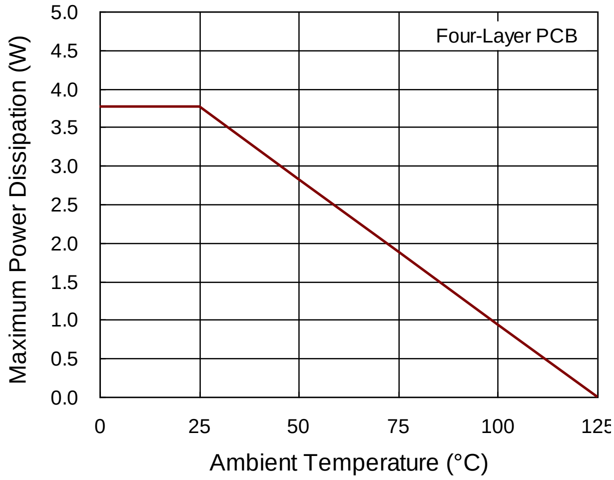
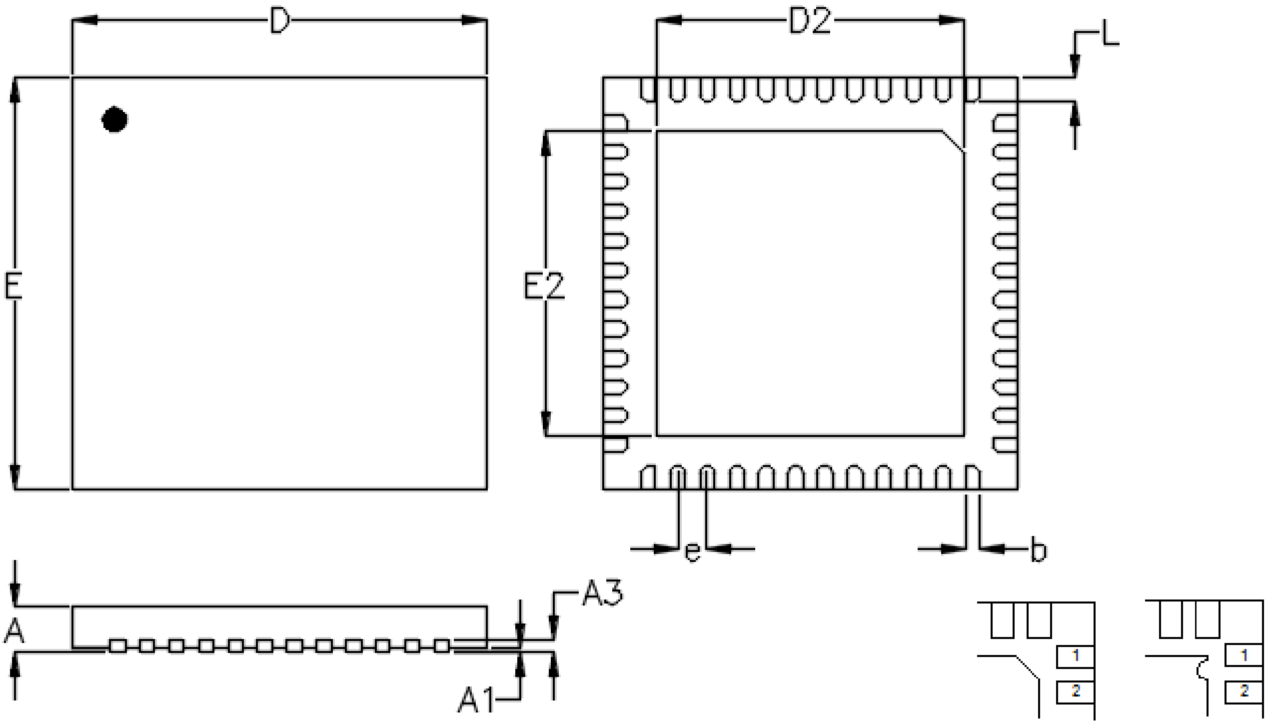


Figure 23. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

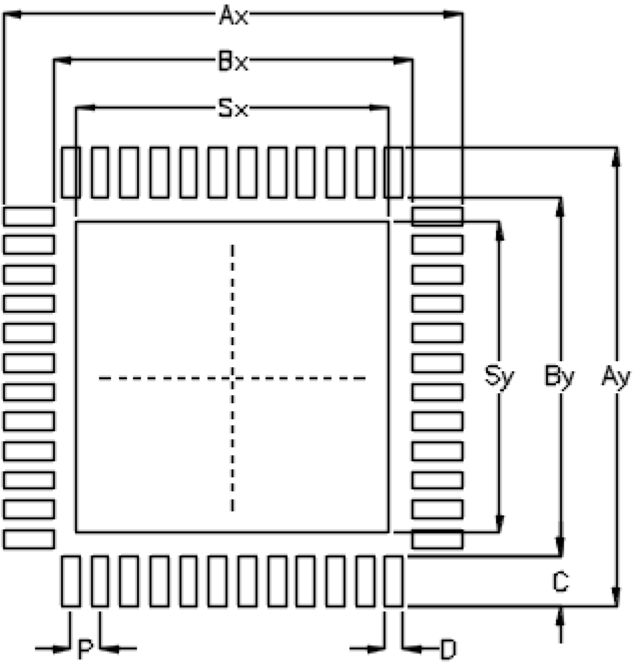
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		6.950	7.050	0.274	0.278
D2	Option1	5.050	5.250	0.199	0.207
	Option2	5.600	5.700	0.220	0.224
E		6.950	7.050	0.274	0.278
E2	Option1	5.050	5.250	0.199	0.207
	Option2	5.600	5.700	0.220	0.224
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 48L QFN 7x7 Package

Note : The package of RTQ8825 uses Option1.

Footprint Information

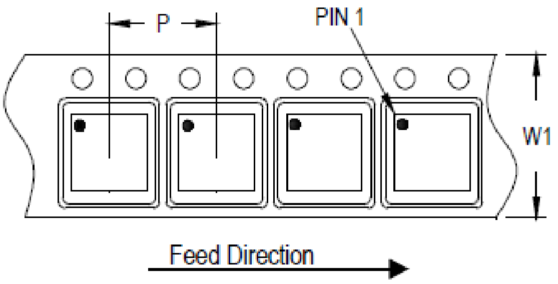


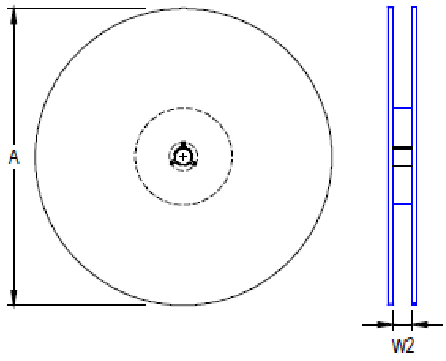
Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7*7-48	Option1	48	0.50	7.80	7.80	6.10	6.10	0.85	0.30	5.30	5.30	±0.05
	Option2									5.65	5.65	

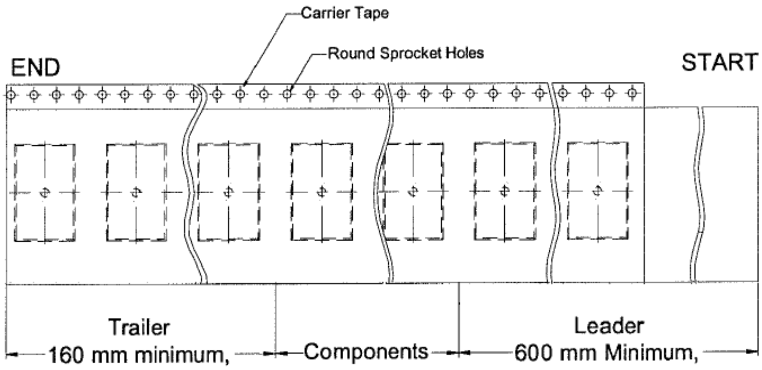
Note : The package of RTQ8825 uses Option1.

Packing Information

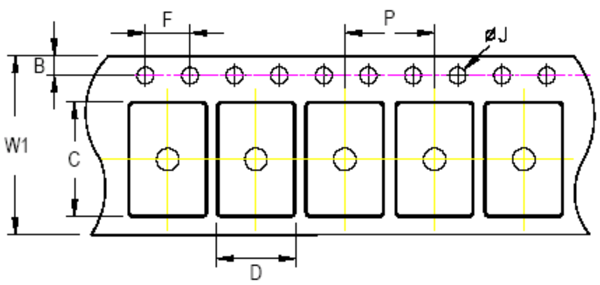
Tape and Reel Data

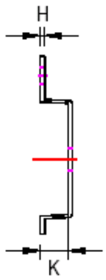






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 7x7	16	12	330	13	2,500	160	600	16.4/18.4





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Package \ Container	Reel Size	Reel Units	Box Item	Box Reels	Box Units	Carton Item	Carton Boxes	Carton Units
QFN and DFN 7x7	13”	2,500	Box G	1	2,500	Carton A	6	15,000

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
01	2024/2/6	Modify	Ordering Information on P2 Recommended Operating Conditions on P9 Application Information on P24, 34 Outline Dimension on P72 Footprint Information on P73 Packing Information on P74, 75, 76