RICHTEK®

RTQ9124T-QA

1x27W, Digital Input Automotive Audio Amplifier with Current Sense and Real-Time Load Diagnostics

1 General Description

The RTQ9124T-QA is an ultra-low output noise, high-efficiency, mono channel class-D audio power amplifier. It can achieve over 85.5% power efficiency, with an output switching frequency of up to 2.1MHz, enabling a cost-optimized solution in a very small PCB size. The switching frequency can be set either above the AM band, which eliminates AM-band interference and reduces output filter size and cost, or below the AM band to optimize efficiency.

The RTQ9124T-QA is fully configurable through the I^2C bus interface and includes a comprehensive diagnostics array specifically designed for automotive applications.

The built-in anti-pop functions reduce speaker pop noise under all scenarios. Additionally, the built-in protection circuits provide thermal fold-back, over-temperature, overcurrent, overvoltage, and undervoltage protection, and report error status.

The RTQ9124T-QA is a 3-wire device that receives all clocks from external sources using standard I^2S and TDM (Time-Division Multiplexing) formats. It supports a wide input sampling rate from 8kHz to 192kHz.

The RTQ9124T-QA is intended for various automotive audio applications, including telematics and e-call systems.

The RTQ9124T-QA is available in a TSSOP-28 (Exposed Pad) package. The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 125°C.

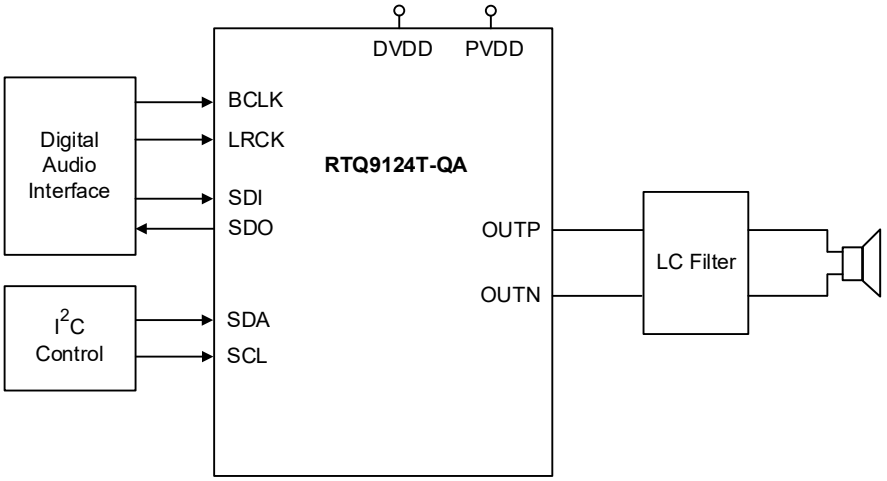
2 Features

- **AEC-Q100 Qualified**
- **I^2S and TDM Input (Up to 16CH TDM)**
- **1x27W, THD+N = 10%, 4Ω, 14.4V**
- **THD+N is 0.05%**
- **SNR up to 115dB**
- **Ultra-Low Noise = 18μV**
- **Switching Frequency up to 2.1MHz**
- **Sampling Frequency from 8kHz to 192kHz**
- **I^2C Control with 4 Address Options**
- **Built-In Anti-Pop Function**
- **Built-In Thermal Fold-Back and Clip Detection**
- **Ultra-Low Quiescent Mode (ULQM)**
- **AC-DC Load Diagnostics**
- **Real Time Load Diagnostics**
- **Temperature and Voltage Sensing via I^2C**
- **Protection Features**
  - **Output Short-Circuit**
  - **Overvoltage and Undervoltage**
  - **Overcurrent Warning**
  - **Overcurrent**
  - **Over-Temperature**
  - **DC Detection**
  - **40V Load Dump**
- **Ambient Temperature Range: –40°C to 125°C**
- **Junction Temperature Range: –40°C to 150°C**

3 Applications

- e-Call Systems
- Telematics
- AVAS

4 Simplified Application Circuit



5 Ordering Information

RTQ9124T□-QA□

Packing
A: Standard

Grade
QA: AEC-Q100 Qualified

Package Type(1)
S: TSSOP-28 (Exposed Pad)
(Exposed Pad: Option 5)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

RTQ9124
TSQA
•YMDAN

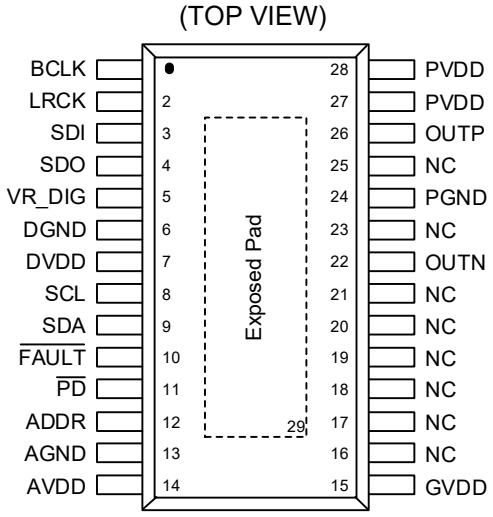
RTQ9124TSQA: Product Code
QA: Automotive Product Grade
YMDAN: Date Code

Device Option Table

Part Number	Channel Count	Supply Voltage Range	Output Power / 10%THD+N / 4Ω, 14.4V	Sampling Rate	Package
RTQ9124LTS-QAA	1	4.5V to 18V	15W	Up to 192kHz	TSSOP-28 (Exposed Pad)
RTQ9124TS-QAA	1	4.5V to 18V	27W	Up to 192kHz	TSSOP-28 (Exposed Pad)
RTQ9124DHN-QAA	1	4.5V to 18V	30W	Up to 192kHz	WET-VQFN-32L 5x5 (V-Type)
RTQ9124DLN-QAA	1	4.5V to 18V	10W	Up to 96kHz	WET-VQFN-32L 5x5 (V-Type)

Table of Contents

7 Pin Configuration



TSSOP-28 (Exposed Pad)

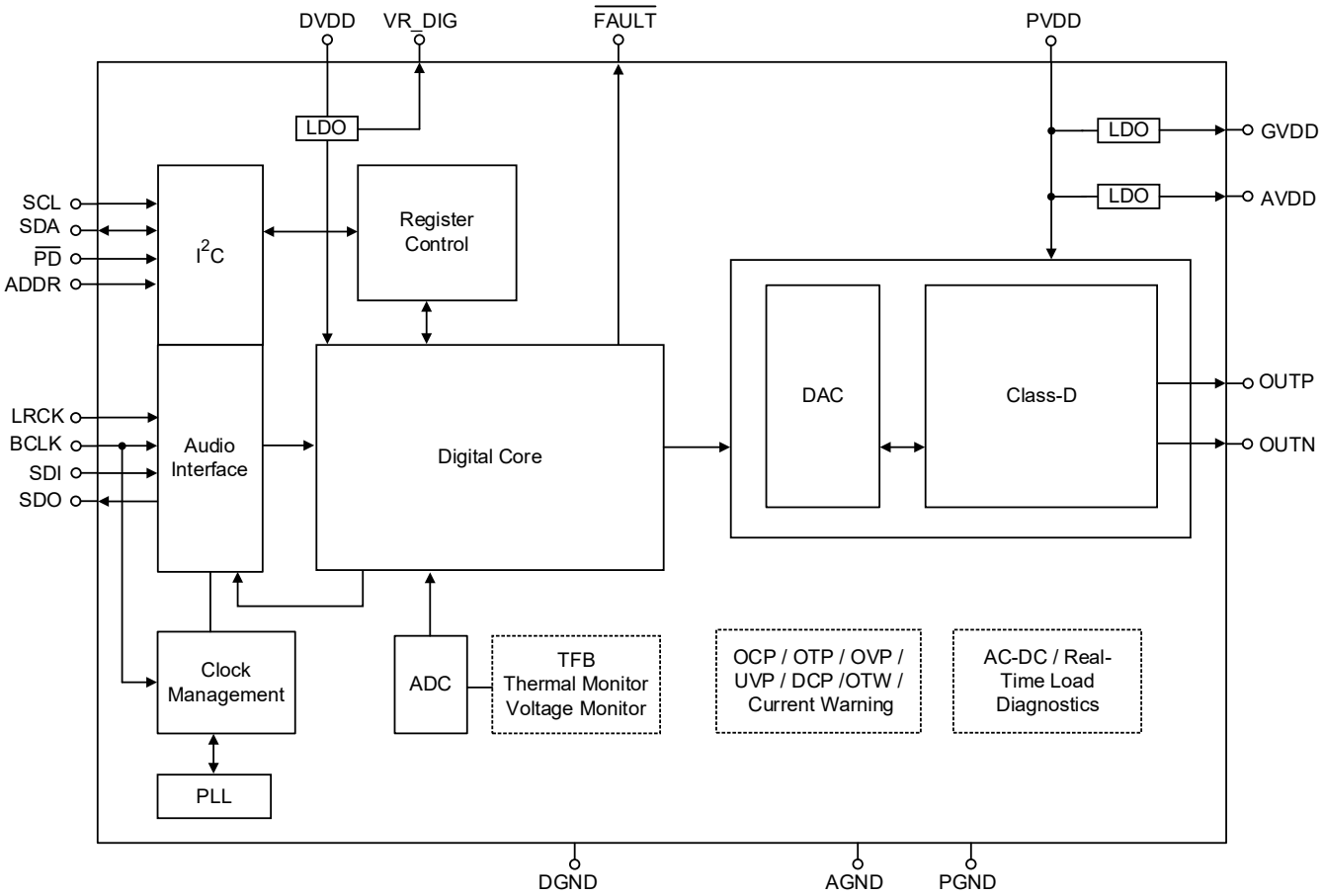
8 Functional Pin Description

Pin No.	Pin Name	IO	Pin Function
1	BCLK	DI	I^2S bit clock.
2	LRCK	DI	I^2S frame clock.
3	SDI	DI	I^2S data in.
4	SDO	DO	I^2S data out.
5	VR_DIG	PWR	Voltage regulator output is 1.8V; tie to DVDD when DVDD = 1.8V.
6	DGND	GND	Ground for digital circuit.
7	DVDD	PWR	Supply voltage for digital circuit.
8	SCL	DI	I^2C reference clock.
9	SDA	DI/DO	I^2C data.
10	$\overline{\text{FAULT}}$	DO	Fault flag, 0 = fault happens; 1 = normal.
11	$\overline{\text{PD}}$	DI	Power down pin, low active.
12	ADDR	DI	I^2C address pin.
13	AGND	GND	Ground for analog circuit.
14	AVDD	PWR	Voltage regulator output 5.1V.
15	GVDD	PWR	Gate drive voltage 5.1V.
16, 17, 18, 19, 20, 21, 23, 25	NC	NC	No internal connection.
22	OUTN	NO	Negative PWM output.
24	PGND	GND	Ground for power stage.
26	OUTP	PO	Positive PWM output.
27, 28	PVDD	PWR	Supply voltage for power stage.
29 (Exposed Pad)	Exposed Pad	EP	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

8.1 IO Type Definition

- GND: Ground
- PWR: Power
- PO: Positive Output
- NO: Negative Output
- DI: Digital Input
- DO: Digital Output
- DI/DO: Digital Input/Output
- NC: No Connection
- EP: Exposed Pad

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, PVDD ---------- –0.3V to 28V
- Vpeak, transient supply voltage, PVDD (t ≤ 400ms Exposure) ---------- –1V to 40V
- Speaker Amplifier Output Voltage, OUTP, OUTN ---------- –0.3V to 28V
- DVDD, SCL, SDA, $\overline{\text{FAULT}}$, $\overline{\text{PD}}$, BCLK, LRCK, SDI, SDO, ADDR ---------- –0.3V to 6V
- AVDD, GVDD ---------- –0.3V to 6V
- VR_DIG ---------- –0.3V to 4V

  Power Dissipation, P_D @ T_A = 25°C

  TSSOP-28 (Exposed Pad) ---------- 3.29W
- Package Thermal Resistance (Note 3)

  TSSOP-28 (Exposed Pad), θ_{JA} ---------- 30.39°C/W

  TSSOP-28 (Exposed Pad), θ_{JC} ---------- 1.41°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –55°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- ±2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, PVDD ---------- 4.5V to 18 V
- Supply Input Voltage, DVDD ---------- 1.62 to 3.6 V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(PVDD = 14.4V, DVDD = 3.3V, R_L = 4Ω, f_{SW} = 2.1MHz, AES17 filter, BTL, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DVDD Quiescent Current (Normal Mode)	I_{Q_DVDD}	Output channel playing, switch 50% duty	--	4.3	--	mA
DVDD Quiescent Current (ULQM)	I_{ULQM_DVDD}	ULQM	--	1.7	--	mA
DVDD Shutdown Current	I_{SD_DVDD}	$\overline{PD}$ = 0V	--	1.7	--	μA
PVDD Quiescent Current (Normal Mode)	I_{Q_PVDD}	Output channel playing, switch 50% duty	--	50	--	mA
PVDD Quiescent Current (ULQM)	I_{ULQM_PVDD}	ULQM	--	0.7	--	mA
PVDD Shutdown Current	I_{SD_PVDD}	$\overline{PD}$ = 0V	--	7	--	μA
AVDD	V_{AVDD}		--	5.1	--	V
GVDD	V_{GVDD}		--	5.1	--	V
VR_DIG	V_{VR_DIG}		--	1.8	--	V
Speaker Gain Variation	ΔGain	Gain variation	−0.5	--	0.5	dB
PWM Switching Frequency	f_{SW}	384kHz mode	--	384	--	kHz
		2100kHz mode	--	2100	--	
RMS Output Power Per Channel	P_O	4Ω, PVDD = 14.4V, THD+N = 1%	--	22	--	W
RMS Output Power Per Channel	P_O	4Ω, PVDD = 14.4V, THD+N = 10%	--	27	--	W
Total Harmonic Distortion + Noise	THD+N	P_O = 1W	--	0.05	--	%
Output Integrated Noise	Vn	20Hz to 20kHz, A-weighting	--	18	--	μV
Signal-to-Noise Ratio	SNR	PVDD = 14.4V, Po@THD+N = 1%	--	115	--	dB
Power Supply Rejection Ratio	PSRR	Frequency @ 1kHz	--	−75	--	dB
Dynamic Range	DR	Input level −60dBFS	--	115	--	dB
Efficiency	η	25W output, 4Ω load, PVDD = 14.4V, including inductor loss	--	85.5	--	%
Click and POP		High-Z/MUTE to Play, Play to MUTE/High-Z	--	5	--	mV
Junction Over-Temperature Warning	T_{OTW}		--	150	--	°C
Junction Over-Temperature Protection	T_{OTP}		--	170	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Overcurrent Warning	I_{OCW}		--	5	--	A
Overcurrent Protection	I_{OCP}	Any short to supply or ground	--	6	--	A
PVDD Overvoltage Protection	V_{OVP_PVDD}		--	19.5	--	V
PVDD Overvoltage Protection Hysteresis	$V_{OVP\_HYS\_PVDD}$		--	0.7	--	V
PVDD Undervoltage Protection	V_{UVP_PVDD}		--	4	--	V

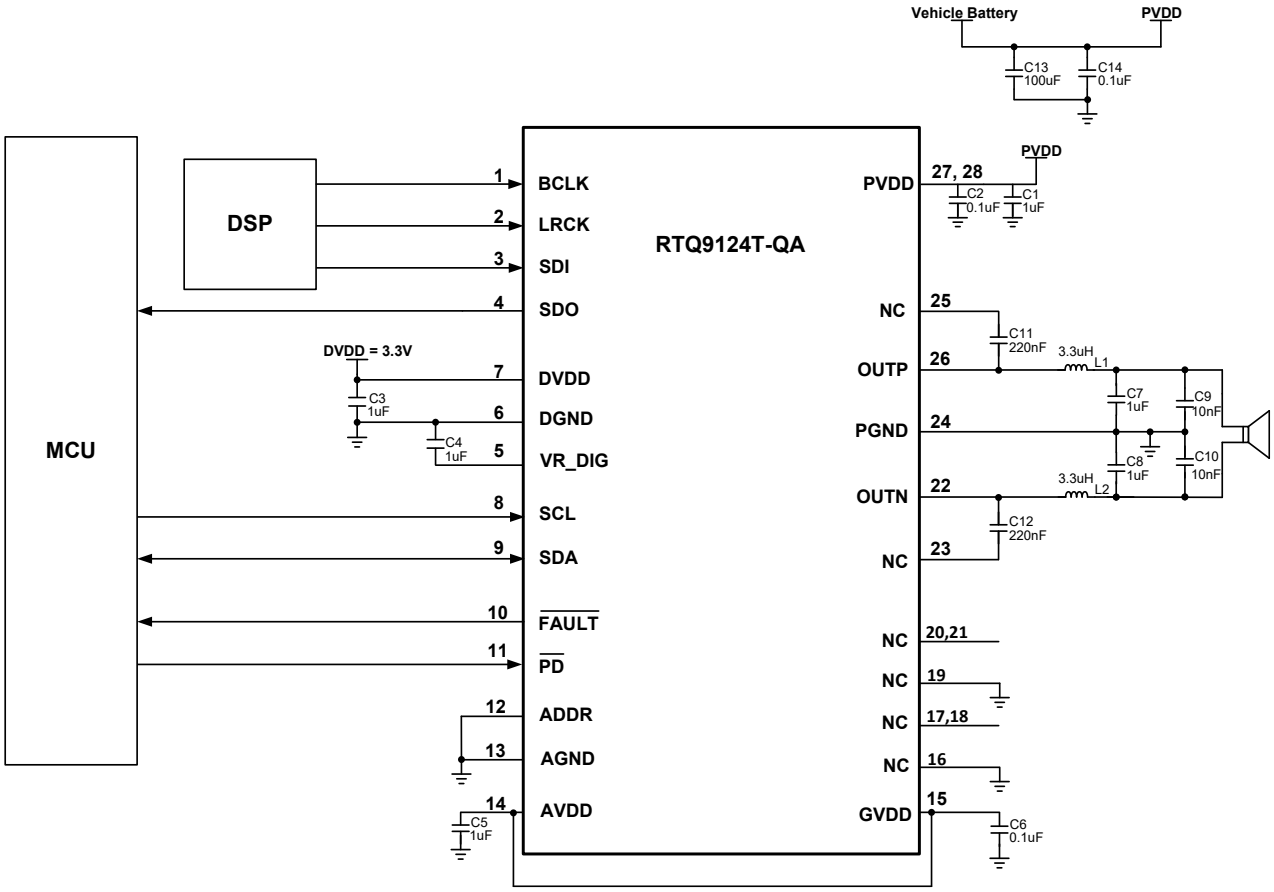
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PVDD Undervoltage Protection Hysteresis	$V_{UVP\_HYS\_PVDD}$		--	0.28	--	V
DVDD Undervoltage Protection	V_{UVP_DVDD}		--	1.4	--	V
DVDD Undervoltage Protection Hysteresis	$V_{UVP\_HYS\_DVDD}$		--	0.1	--	V
DC Detection	$DC_{\_DET}$	Output DC fault protection	--	0.9	--	V
Resistance to Detect a Short from OUT Pins to PVDD	R_{S2P}		--	400	--	Ω
Resistance to Detect a Short from OUT Pins to Ground	R_{S2G}		--	200	--	Ω
Open Load	R_{OL}		--	50	--	Ω
Short Load	R_{SL}		--	±0.5	--	Ω
DC Diagnostic Time	t_{DC_DIAG}		--	100	--	ms
AC Diagnostic Time	t_{AC_DIAG}		--	50	--	ms
ULQM Wake-Up Time	t_{ULQM_WP}		--	--	10	ms
$\overline{FAULT}$ VOL: Low-Level-Output Voltage	V_{OL}	I_O = 3mA	--	--	0.4	V
$\overline{PD}$ Function Electrical Characteristics						
High-Level Input Voltage	V_{IH}		1.4	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	0.3	V
I^2C Interface Electrical Characteristics						
High-Level Input Voltage (Belongs to the Internal 1.8V Domain)	V_{IH}		1.26	--	--	V
Low-Level Input Voltage (Belong to the Internal 1.8V Domain)	V_{IL}		--	--	0.54	V
Pull-Down Current	I_{FO2}	(Note 6)	--	2	--	μA
Clock Operating Frequency	f_{SCL}		--	--	1000	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		0.5	--	--	μs
Hold Time After (Repeated) Start Condition	$t_{HD,STA}$		0.26	--	--	μs
Repeated Start Condition Setup Time	$t_{SU,STA}$		0.26	--	--	μs
Stop Condition Time	$t_{SU,STD}$		0.26	--	--	μs
Data Setup Time	$t_{SU,DAT}$		50	--	--	ns
Clock Low Period	t_{LOW}		0.5	--	--	μs
Clock High Period	t_{HIGH}		0.26	--	--	μs
Clock Data Fall Time	t_F		20	--	120	ns
Clock Data Rise Time	t_R		20	--	120	ns

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Slave Mode I^2S Interface Electrical Characteristics							
High-Level Input Voltage		V_{IH}		1.26	--	--	V
Low-Level Input Voltage		V_{IL}		--	--	0.54	V
SDO	VOH: High-Level Output Voltage	V_{OH}		--	--	3.3	V
	VOL: Low-Level Output Voltage	V_{OL}		--	--	0.4	
Frequency		f_{BCLKIN}		1.024	--	24.576	MHz
Setup Time, LRCK to BCLK Rising Edge		t_{SU1}		10	--	--	ns
Hold Time, LRCK from BCLK Rising Edge		t_{H1}		10	--	--	ns
Setup Time, SDIN to BCLK Rising Edge		t_{SU2}		10	--	--	ns
Hold Time, SDIN from BCLK Rising Edge		t_{H2}		10	--	--	ns
Rise/Fall Time for BCLK/LRCK		t_R/t_F		--	--	8	ns
I^2S Duty Cycle for Rising		%		40	--	60	%

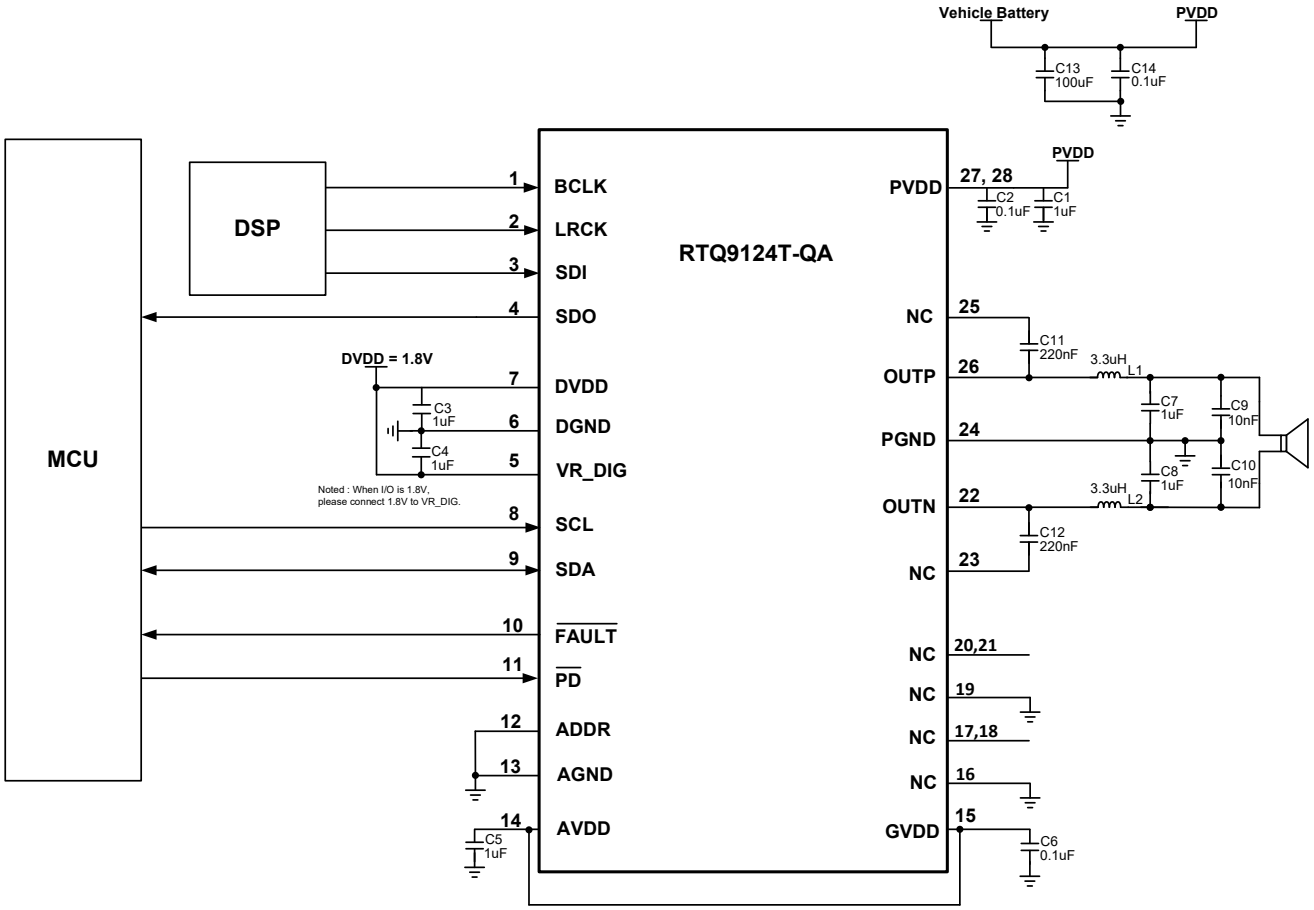
Note 6. The capability of the receiver to pull down the SDA line during the acknowledge clock pulse.

13 Typical Application Circuit

13.1 3.3V I/O Application

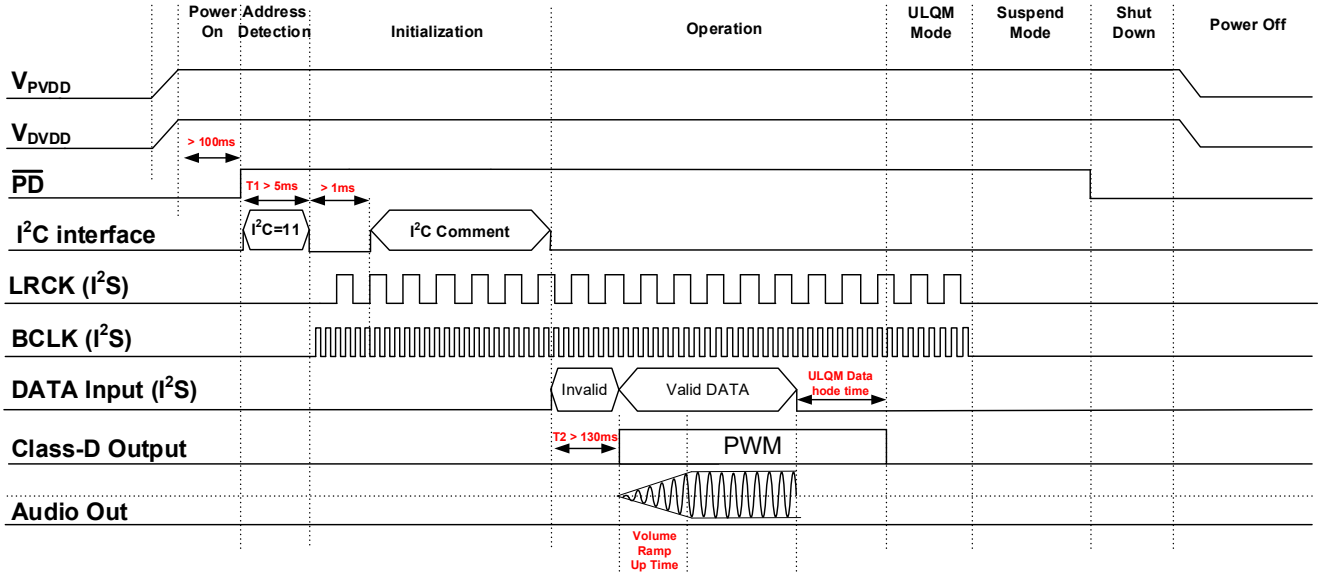


13.2 1.8V I/O Application



14 Timing Diagram

14.1 Power-On/Off Sequence



14.2 Initial Sequence

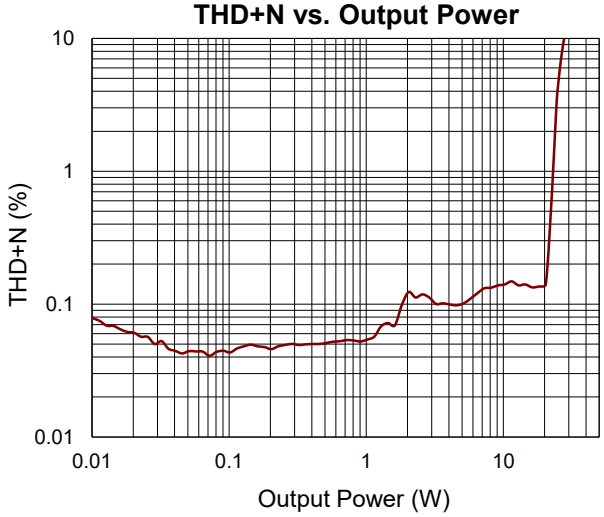
Initial Sequence (PWM = 2.1MHz)

Sequence	reg_addr	reg_size	reg_value	Description
2	0x04	2	0x3D00	Amp Turn On

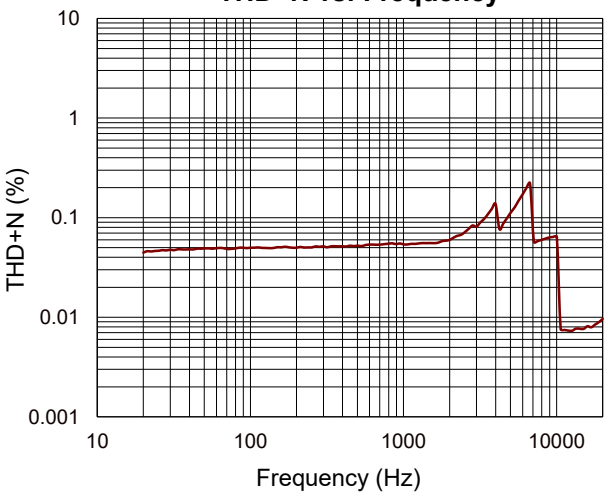
15 Typical Operating Characteristics

TA = 25°C, VBAT = PVDD = DVDD =14.4V, RL = 4Ω, fin = 1kHz, fs = 48kHz, fSW = 2.1MHz, BTL, AES17 filter, LC filter: 3.3μF –VCMT053T-3R3MN5, 1μF.

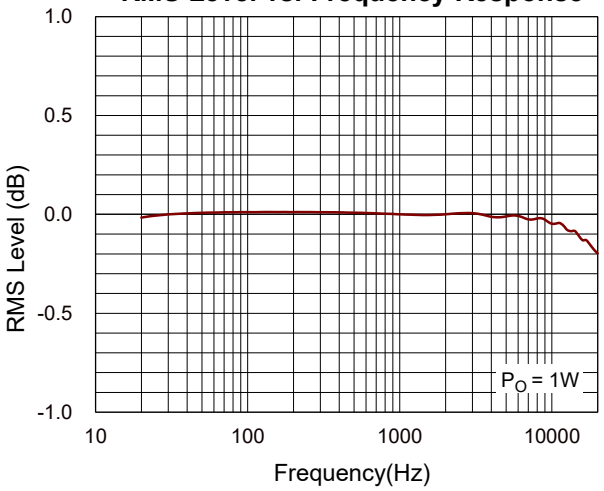
THD+N vs. Output Power



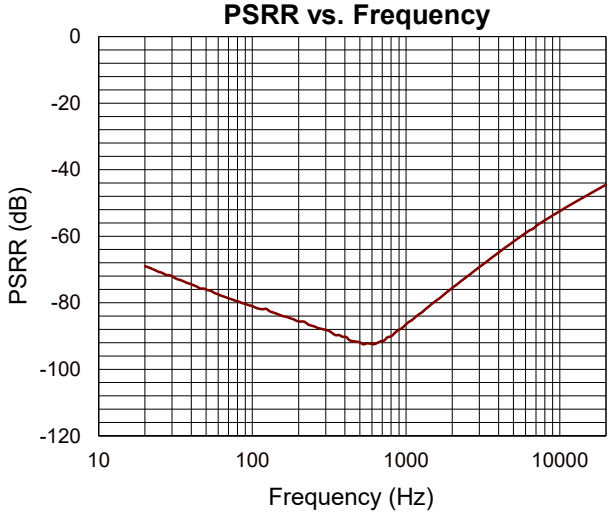
THD+N vs. Frequency

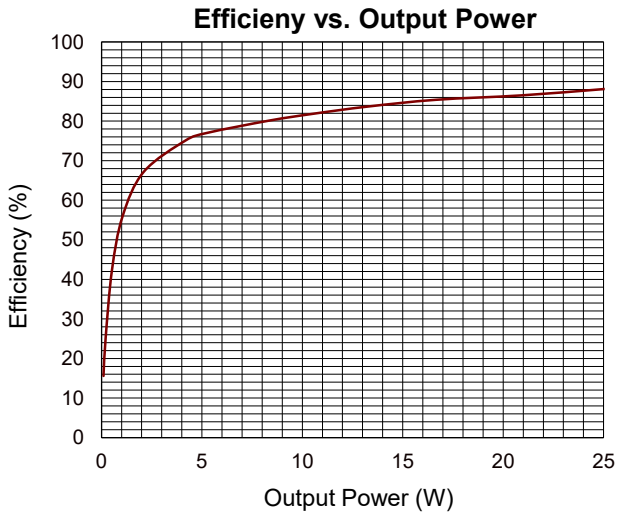


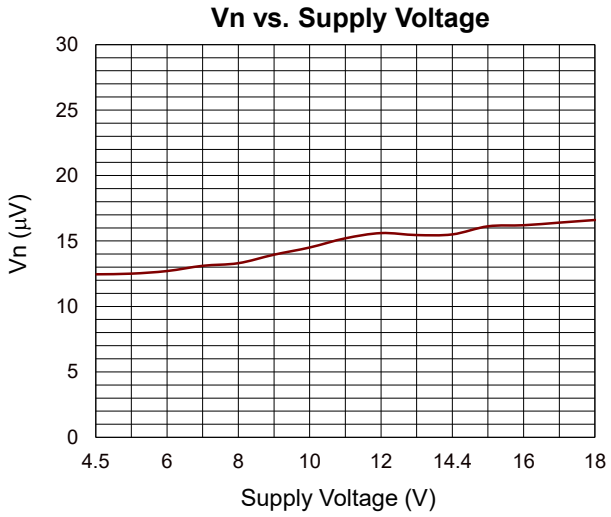
RMS Level vs. Frequency Response

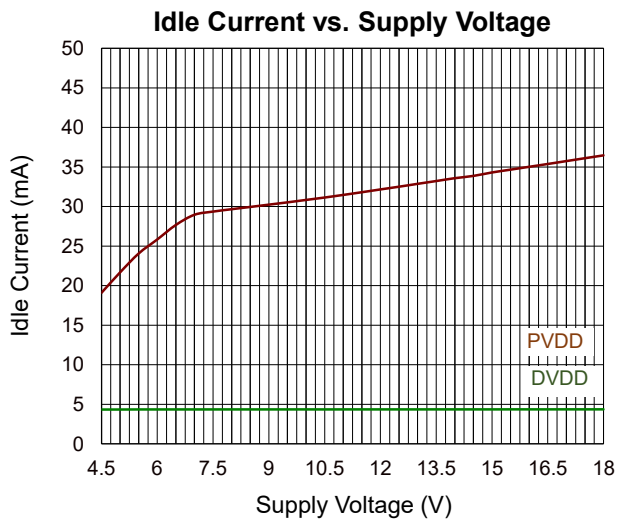


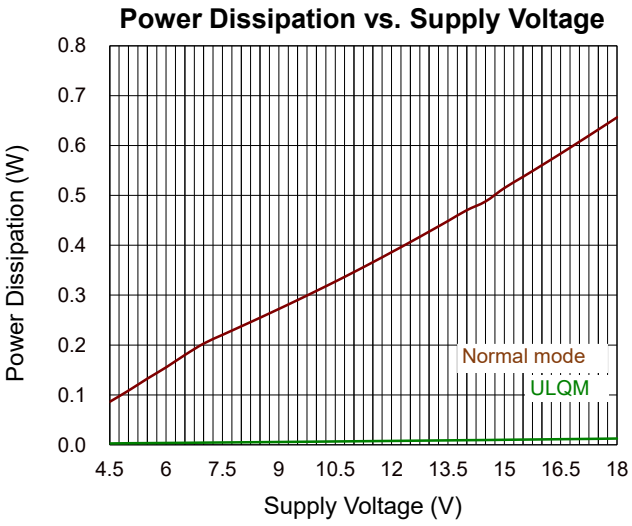
PSRR vs. Frequency











16 Application Information

(Note 7)

16.1 I²C Serial Communication Bus

The RTQ9124T-QA supports four sets of slave addresses, configurable through combinations of the ADDR pin. The pin can be set using different resistors, each with a tolerance of 5%. Refer to the table below for specific address configurations.

The 3.3V input voltage application is for the ADDR pin.

$\overline{PD}$	ADDR	Slave Address	Write	Read
Pull high	Pull high	0x10 (0010000x)	0x20	0x21
Pull high	Pull high with 24kΩ	0x11 (0010001x)	0x22	0x23
Pull high	Pull low with 24kΩ	0x12 (0010010x)	0x24	0x25
Pull high	Pull low	0x13 (0010011x)	0x26	0x27

The 1.8V input voltage application is for the ADDR pin.

$\overline{PD}$	ADDR	Slave Address	Write	Read
Pull high	Pull high	0x10 (0010000x)	0x20	0x21
Pull high	Pull low	0x13 (0010011x)	0x26	0x27

The RTQ9124T-QA is equipped with I²C communication capabilities, utilizing the SCL and SDA input ports. In the I²C protocol, devices transmitting data are designated as transmitters, while those reading the data are receivers. The master device initiates and controls the data transfer, supplying the serial clock to ensure synchronization. The RTQ9124T-QA functions exclusively as a slave device in all communications and is capable of operating at speeds of up to 1000 kB/s. Its I²C interface is designed to be slave-only.

16.2 I²C Bus Protocol

Data transitions on the SDA line are only permitted when the SCL clock signal is low. Transitions on the SDA line while the SCL signal is high indicate a START or STOP condition. A START condition is signaled by a high-to-low transition on the SDA line while the SCL line remains high and stable. This condition must be established before any data transfer command is issued. Conversely, a STOP condition is signaled by a low-to-high transition on the SDA line while the SCL line remains high and stable, marking the end of communication between the RTQ9124T-QA and the bus master. During data reception, the RTQ9124T-QA samples the SDA line at the rising edge of the SCL signal. To ensure proper operation of the device, the SDA signal must remain stable during the rising edge of the SCL signal, and data changes on the SDA line should only occur when the SCL signal is low.

16.3 Audio Interface

The RTQ9124T-QA supports four types of audio interfaces: I²S, Left-Justified, Right-Justified, and TDM. Each interface is capable of handling audio data formats of 24-bits, 20-bits, and 16-bits. The corresponding timing diagrams are provided below.

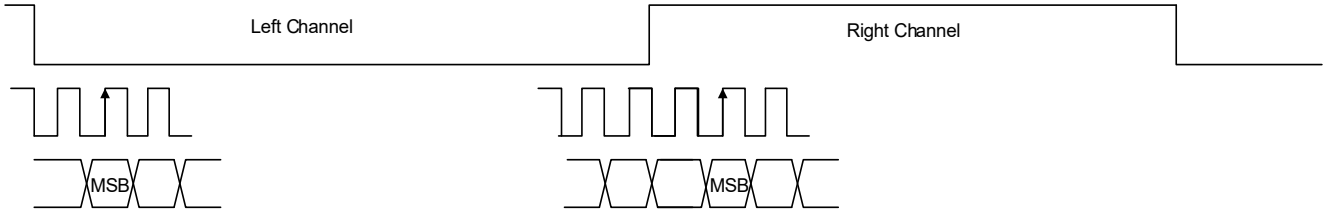


Figure 1. I²S Format

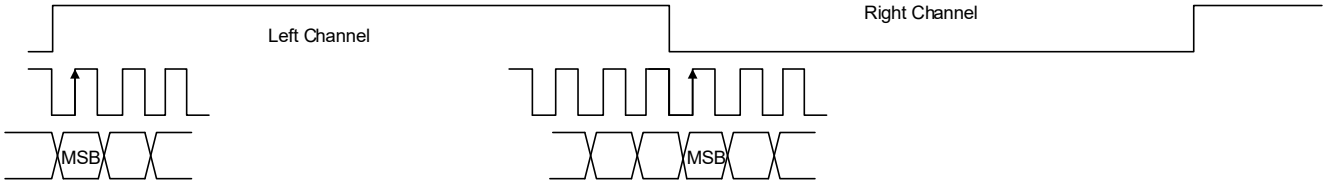


Figure 2. Left-Justified

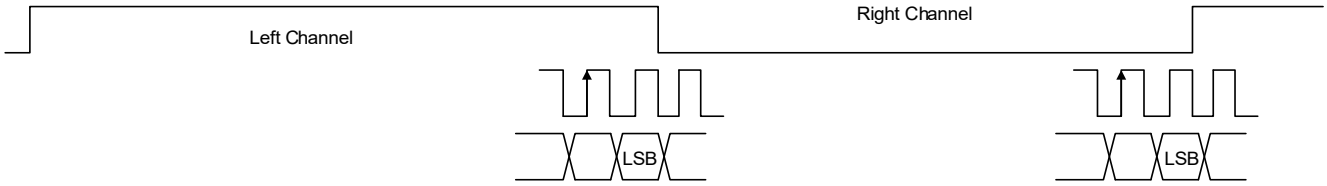


Figure 3. Right-Justified

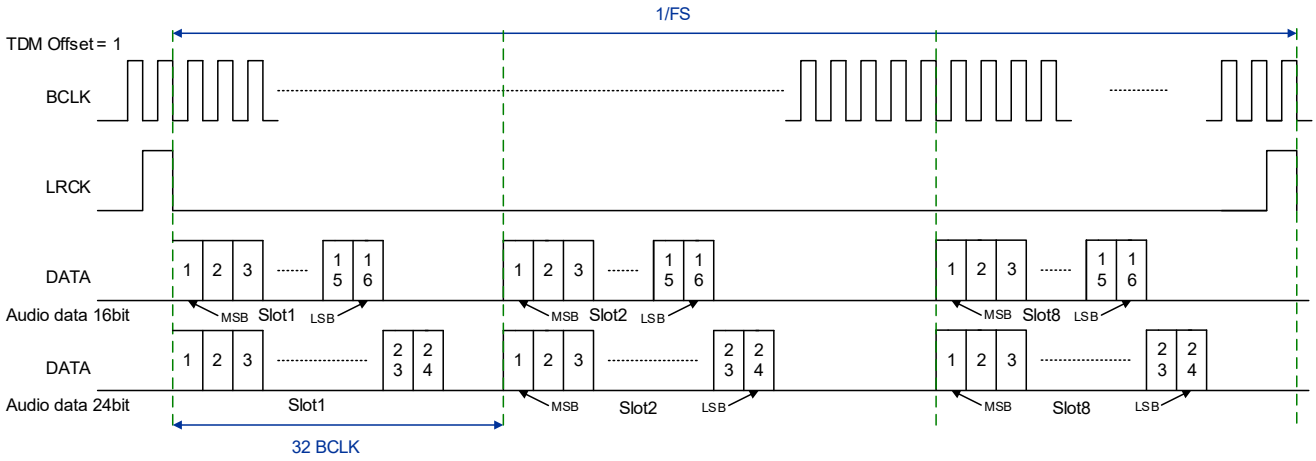


Figure 4. TDM (Offset = 1)

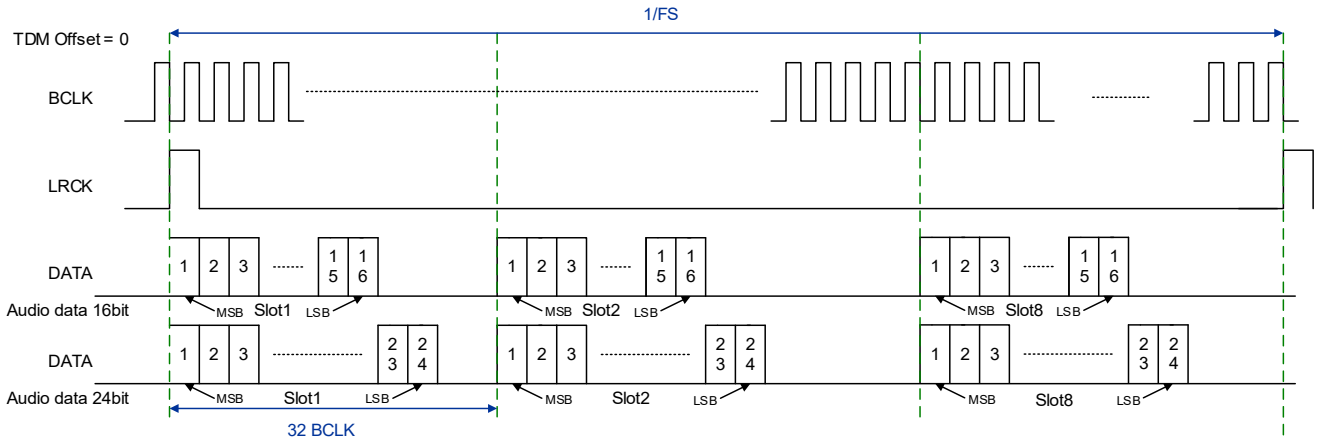


Figure 5. TDM (Offset = 0)

16.4 Time-Division Multiplexing (TDM) Mode

The TDM mode supports a maximum of 16 audio channels. The device can be configured via I²C to select different channels within the TDM data stream. Refer to Table 2. **Register Map** for details.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x02	2	2:0	RW	AUD_FMT	000: I²S (default) 001: Left-Justify 010: Right-Justify 011: DSP mode 100: EIAJ Others: TDM mode	000
0x34	2	5:0	RW	TDM_RX_LOC_CH1	TDM start receiving location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offset 111101: Start from 488+offset 111110: Not available 111111: Not available	000000

For examples:

■ TDM 8 Channels, Sampling Rate is 48KHz.

Channel Location	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8
0x34	Set to 0x00	Set to 0x04	Set to 0x08	Set to 0x0C	Set to 0x10	Set to 0x14	Set to 0x18	Set to 0x1C

■ TDM 16 Channels, Sampling Rate is 48KHz.

Channel Location	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8
0x34	Set to 0x00	Set to 0x04	Set to 0x08	Set to 0x0C	Set to 0x10	Set to 0x14	Set to 0x18	Set to 0x1C
Channel Location	**Ch9**	**Ch10**	**Ch11**	**Ch12**	**Ch13**	**Ch14**	**Ch15**	**Ch16**
0x34	Set to 0x20	Set to 0x24	Set to 0x28	Set to 0x2C	Set to 0x30	Set to 0x34	Set to 0x38	Set to 0x3C

16.5 Digital Signal Processor

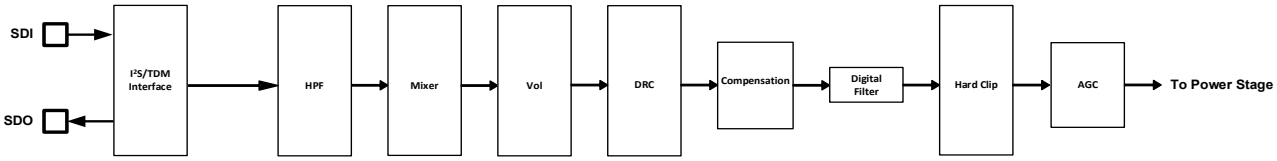


Figure 6. Digital Signal Processor

16.6 High-Pass Filter (HPF)

The RTQ9124T-QA supports an input high-pass filter (HPF) for each channel, designed to act as a DC-cut filter with a cutoff frequency of 1.5Hz.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x08	2	6	RW	HPF_EN	High-Pass filter enable 0: Disable 1: Enable (default)	1

16.7 I²S channel selection

The RTQ9124T-QA supports an input channel selection of I²S format

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x00	2	1:0	RW	CH_SI	I²S channel selection 01: L channel (default) 10: R channel others: (L+R)/2	01

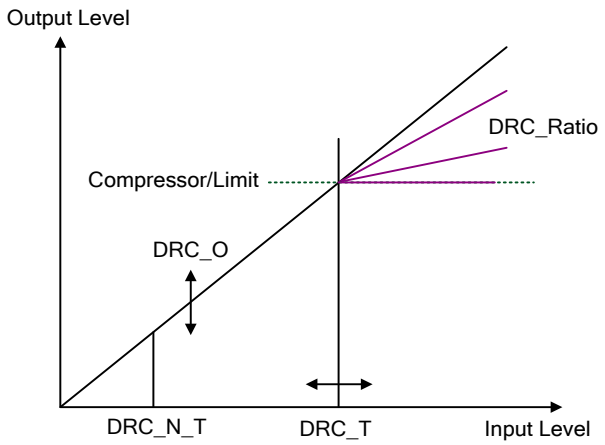
16.8 Volume

The RTQ9124DH-QA includes a volume control (VOL) feature. The volume can be adjusted in precise steps of 0.0625dB, with a range from 24dB to mute. A dedicated mute control is also provided for immediate muting of the output.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x38	2	10:0	RW	VOL	Master volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180

16.9 Dynamic Range Control (DRC)

The RTQ9124T-QA features Dynamic Range Control (DRC), which provides compression capabilities to adjust audio signals, making them sound softer or louder based on the input level.

DRC Description	Address	Description
DRC_TH: Threshold	0x3A	
DRC_O: Make up gain	0x3B	
DRC_Ratio: Compress ratio	0x3C	
DRC_NG_TH: Noise gate threshold	0x3D	
DRC_EN: DRC Enable	0x08	
DRC_N_EN: Noise gate enable	0x08	

DRC_TH

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x3A	2	10:0	RW	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: −24dB 11'h67E: −103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h000

DRC_Offset

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x3B	2	10:0	RW	DRC_ OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: −103.9375dB 0.0625dB per step	11'h180

DRC_RATIO

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x3C	2	7:0	RW	DRC_ RATIO	DRC compress ratio 8'h00: No compression 8'h80 (default) ~8'hFF: Full compression 1/128 per step	8'h80

DRC_NG_TH

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x3D	2	10:0	RW	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: −24dB 11'h640: −100dB (default) 11'h67E: −103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h640

DRC_EN/DRC_N_EN

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x08	2	4	RW	DRC_EN	DRC Enable 0: disable (default) 1: enable	0
		3	RW	DRC_N_EN	DRC Noise Gate Enable 0: disable (default) 1: enable	0

DRC Gain and Level Attack and Release Timing Settings

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x40	4	16:0	RW	DRC_AE	DRC_AE	17'h08000
0x41	4	16:0	RW	DRC_1_AE	DRC_1_AE	17'h00000
0x42	4	16:0	RW	DRC_AA	DRC_AA	17'h08000
0x43	4	16:0	RW	DRC_AD	DRC_AD	17'h08000

16.10 Compensation Filter

The compensation filter is used to adjust the internal gain from the DAC. This filter can also correct the frequency response affected by the LC filter. The recommended settings will vary based on different application circuits to achieve the desired response curve.

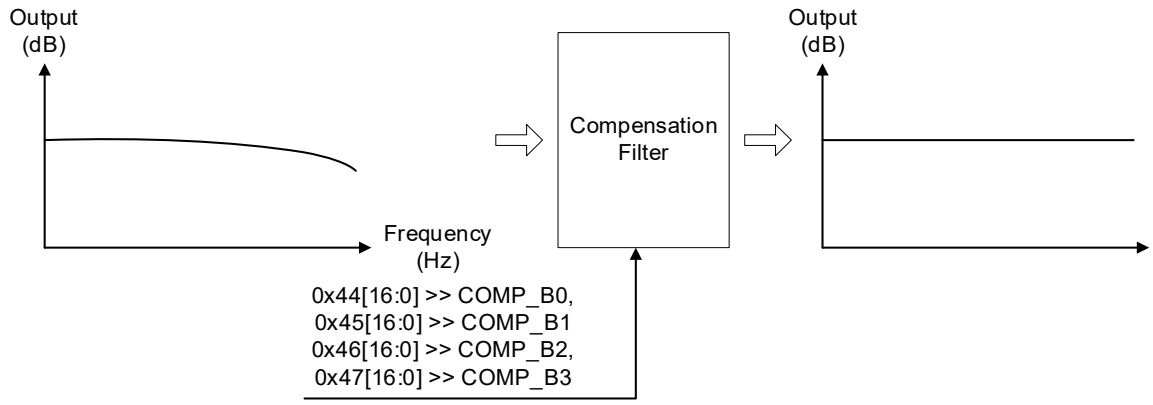


Figure 7. Compensation Filter

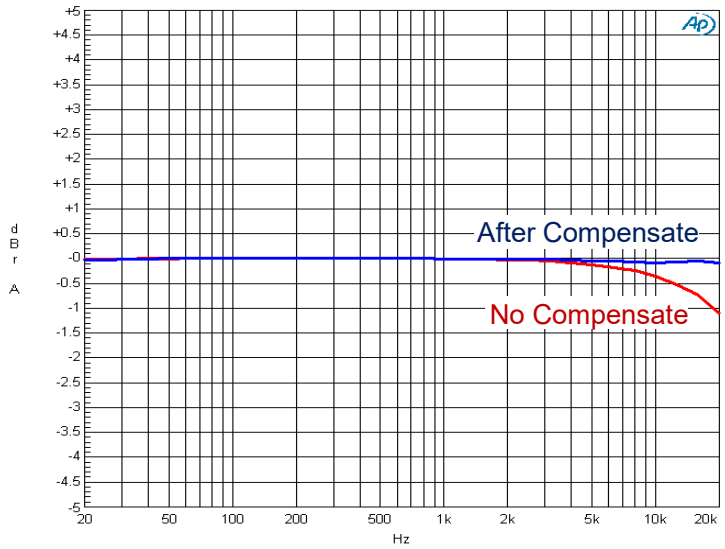


Figure 8. Compensation Filter Measured Result

Table 1. Compensation Table for fs=48kHz

	0.1dB	0.2dB	0.3dB	0.4dB	0.5dB	0.6dB	0.7dB	0.8dB	0.9dB	1.0dB
B3 (0x47)	00002	00006	00009	0000C	0000F	00012	00016	00019	0001D	00021
B2 (0x46)	00007	0000E	00014	0001B	00022	00029	00030	00037	0003B	00043
B1 (0x45)	1FF9D	1FF2F	1FEC5	1FE5A	1FDED	1FD7F	1FD10	1FC9F	1FC2C	1FBB0
B0 (0x44)	080B3	0817A	0823B	082FE	083C3	0848B	08555	08622	086F6	087D9

	-0.1dB	-0.2dB	-0.3dB	-0.4dB	-0.5dB	-0.6dB	-0.7dB	-0.8dB	-0.9dB	-1.0dB
B3 (0x47)	1FFE6	1FFE8	1FFEA	1FFED	1FFF0	1FFF2	1FFF5	1FFF8	1FFFA	1FFFE
B2 (0x46)	1FFBD	1FFC3	1FFCA	1FFD2	1FFD7	1FFDE	1FFE5	1FFEC	1FFF2	1FFF9
B1 (0x45)	003D7	0037A	0031B	002B6	00255	001F4	00193	00130	000CC	00062
B0 (0x44)	0790E	079B6	07A60	07B17	07BC9	07C77	07D27	07DDA	07E8F	07F50

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x44	4	16:0	RW	COMP_B0	Compensation filter coefficient B0.	17'h0_8000
0x45	4	16:0	RW	COMP_B1	Compensation filter coefficient B1.	17'h0_0000
0x46	4	16:0	RW	COMP_B2	Compensation filter coefficient B2.	17'h0_0000
0x47	4	16:0	RW	COMP_B3	Compensation filter coefficient B3.	17'h0_0000

16.11 Hard Clip Function

A Hard clip can be employed to digitally maintain specified THD levels without resorting to voltage clipping. This feature enables users to consistently achieve the same THD (for example, 10% THD) across various power levels (15W, 10W, and 5W) while using the same PVDD level.

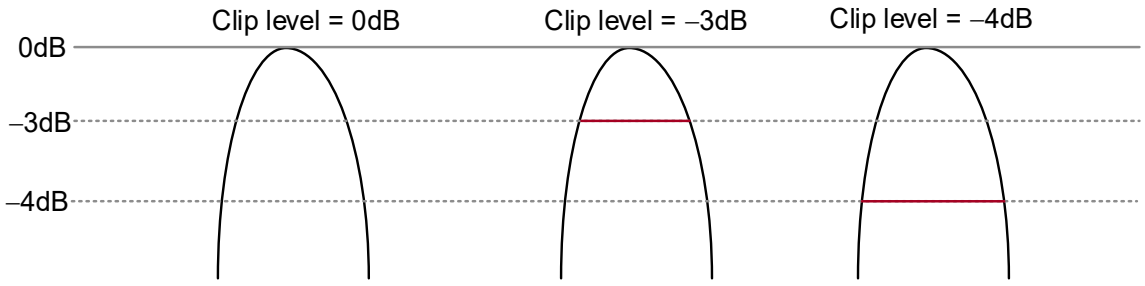


Figure 9. Hard Clip

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x39	2	10:0	RW	HC_TH	Hard clip Threshold when HARD_CLIP_EN = 1 >0dB is not allowable for hard clip threshold setting 11'h18D: -0.825dB (default) 0.0625db per step	11'h18D

16.12 Auto-Gain Control (AGC)

The RTQ9124T-QA supports AGC (Auto-Gain Control) for current limiting and clipping detection functions. The AGC enable is independently controlled by the register at address 0x5A for both current limiting and clipping detection.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x5A	2	0	RW	EN_CLIP_AGC	Enable auto gain control for CLIP detection 0: Disable (default) 1: Enable	0

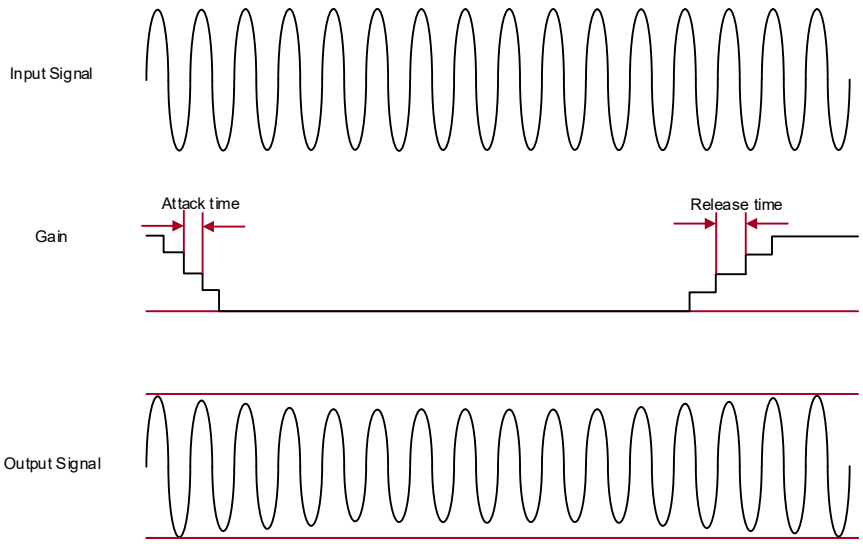


Figure 10. AGC Attack and Release

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x5B	2	3:2	RW	AGC_ATTACK_RATE	AGC attack time selection for AGC 00: 0.25dB/20μs 01: 0.25dB/40μs (default) 10: 0.25dB/80μs 11: 0.25dB/160μs	01
		1:0	RW	AGC_RELEASE_RATE	AGC release time selection for AGC 00: 0.25dB/200ms 01: 0.25dB/400ms (default) 10: 0.25dB/800ms 11: 0.25dB/1600ms	01

16.13 SDO Output Configure

The I²S/TDM digital input signal path from the input pin to the power stage is illustrated in Figure 11. There are several nodes along the digital signal transmission path where the signal can be measured to verify proper functionality. The settings in register 0x01 Bit[7:0] can be output through the SDO pin.

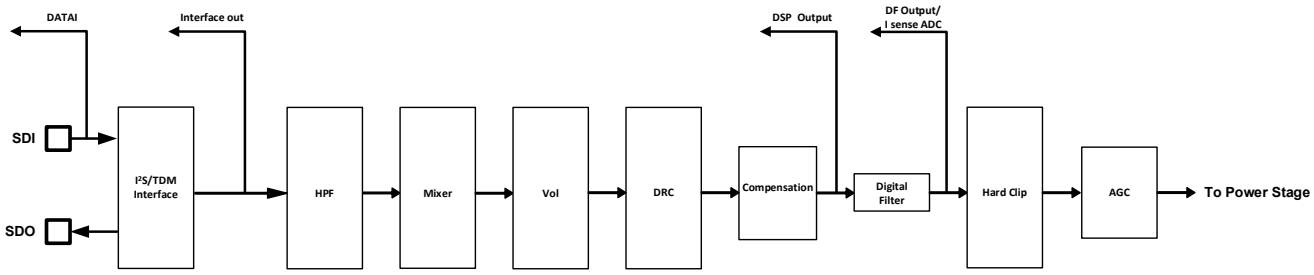


Figure 11. SDO Output Configure

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x01	2	7:4	RW	SDO_SEL_L	Left channel data 0000: no output (default) 0001: I²S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Revered	0000
		3:0	RW	SDO_SEL_R	Right channel data 0000: no output (default) 0001: I²S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Revered	0000

16.14 Hardware Control Pins

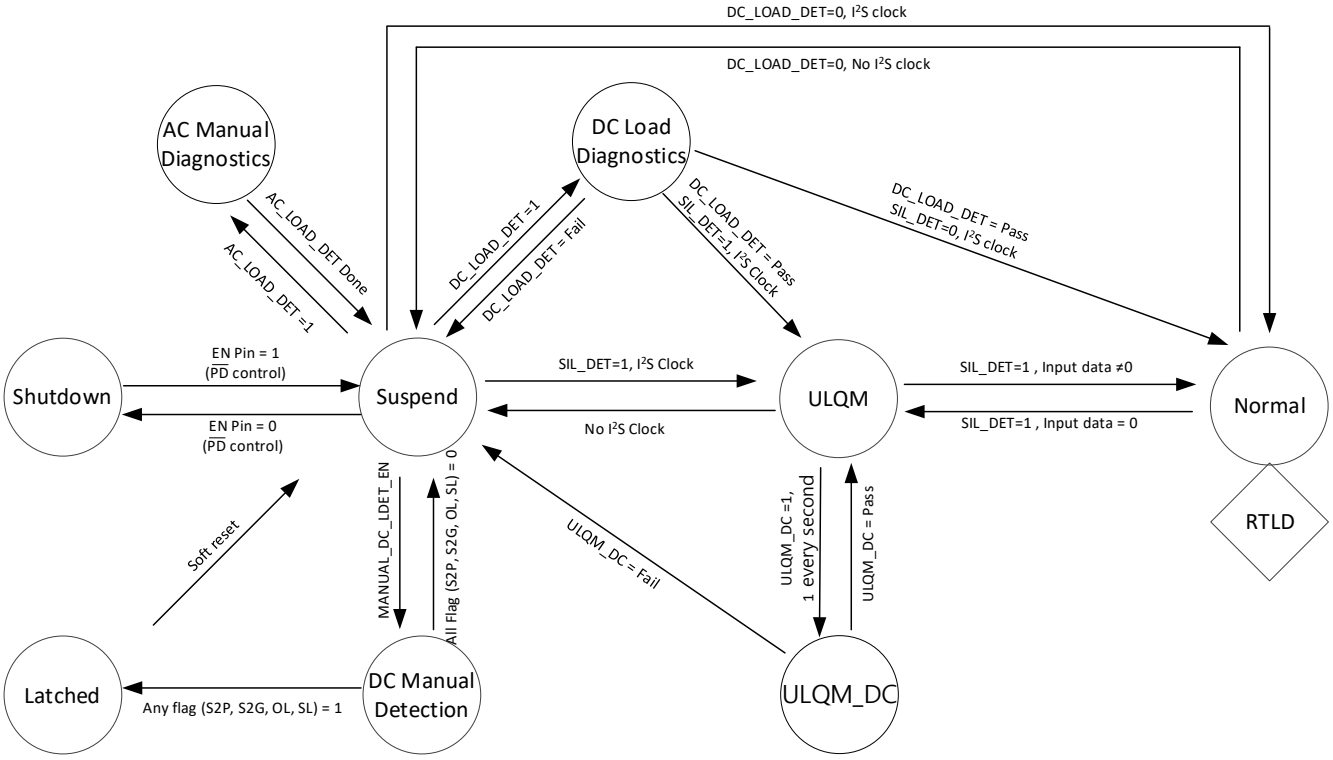
The device features four pins for control and status indication: $\overline{\text{FAULT}}$ pin reports faults and is active low under any of the following conditions:

- Any channel faults (Overcurrent or DC detection)
- Over-temperature protection
- Overvoltage or undervoltage conditions on the PVDD pin
- Undervoltage conditions on the DVDD pin
- Clock error

For all listed faults, the $\overline{\text{FAULT}}$ pin remains asserted even after the fault condition is rectified. The register reports for all faults remain asserted until the CLEAR $\overline{\text{FAULT}}$ method is executed by writing to address 0x0F = FF. At that point, all faults register reports in ERR_INT_INDEX will be cleared to their default values, and the $\overline{\text{FAULT}}$ pin will no longer remain asserted. Register bits are available to mask fault categories from being reported to the $\overline{\text{FAULT}}$ pin. These bits only mask the pin's status and do not affect the register reporting or the device's protection mechanisms. By default, all faults are reported to the pin. Refer to the Register Maps section for a description of the mask settings.

16.15 Operating Modes and Faults

STATE_CTRL	Power MOSFETS	OSCILLATOR	I²C
Normal	Switching with input signal	Active	Active
MUTE	50% duty switching	Active	Active
ULQM	Hi-Z	Active	Active
Suspend	Hi-Z	Active	Active
Hi-Z	Hi-Z	Stopped	Active
Shutdown	Hi-Z	Stopped	Inactive



Fault Event	Reporting	Result	Monitor State	Protection Active	Behavior
CLK Error	I²C+$\overline{\text{FAULT}}$ pin	Hi-Z	All	Output channel	Auto-recovery (default)
VDDA UV	I²C+$\overline{\text{FAULT}}$ pin	Hi-Z	All	Output channel	Auto-recovery (default)
PVDD/ DVDD UV	I²C+$\overline{\text{FAULT}}$ pin	Hi-Z	All	Output channel	Auto-recovery (default)
PVDD	I²C+$\overline{\text{FAULT}}$ pin	Hi-Z	All	Output channel	Auto-recovery (default)
OTP	I²C+$\overline{\text{FAULT}}$ pin	Hi-Z	All	Output channel	Auto-recovery (default)
S2P/S2G/OL/SL	I²C+$\overline{\text{FAULT}}$ pin	Hi-Z	Load detection	Output channel	Latch (default)

Fault Event	Reporting	Result	Monitor State	Protection Active	Behavior
Overcurrent	I^2C+$\overline{FAULT}$ pin	Hi-Z	Normal, Mute	Output channel	Auto-recovery (default)
DC	I^2C+$\overline{FAULT}$ pin	Hi-Z	Normal, Mute	Output channel	Latch (default)
POR	I^2C	Shutdown	All	N/A	N/A
OTW	I^2C	TFB (optional)	All	Output channel	N/A
Clip	I^2C	AGC (optional)	Normal	Output channel	N/A

16.16 Ultra Low Quiescent Mode (ULQM)

The RTQ9124T-QA implements automatic ULQM when there is no input signal and no LRCK/BCLK clock or force enter ULQM for power saving, In ULQM mode, the RTQ9124T-QA powers the FETs in Hi-Z status with low standby current, and the transition time from ULQM to Normal mode is approximately 10ms.

- Support DATAI auto detection for ULQM mode, It The hold time can be adjusted to 1, 20, 40, 80, 160, 320, 640 and 1280ms, the time required to detect input data < ULQM threshold.
- Support I^2S clock detection for suspend mode, the time required to detect both LRCK/BCLK loss.

16.17 Pulse-Width-Modulator (PWM) Frequency

The output switching rate is synchronous to the serial audio clock input and is programmed through I^2C to match the input sample rate in the register (address 0x03[6:4]). The option to switch at a high frequency allows the use of smaller and lower-cost external filtering components.

Sample Rate	Reg 0x03h, BITS 6:4 Setting				
	000	001	010	011	100
8kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
16kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
24kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
32kHz	Not support	Not support	1.28MHz	1.41MHz	1.53MHz
44.1kHz	352kHz	441kHz	1.76MHz	1.94MHz	2.1MHz
48kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
88.2kHz	352kHz	441kHz	1.76MHz	1.94MHz	Not support
96kHz	384kHz	480kHz	1.92MHz	2.1MHz	Not support
192kHz	384kHz	480kHz	1.92MHz	2.1MHz	Not support

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x03	2	6:4	RW	PWM_ FREQ	PWM frequency selection 000: 8*fs 001: 10*fs 010: 40*fs 011: 44*fs (default) 100: 48*fs Others: Reserved	011

16.18 AM-Radio Band Avoidance

By setting the switching frequency of the device above the AM frequency band, interference with AM radio frequencies can be avoided. The available switching frequency options include 38fs, 44fs, and 48fs. If the switching frequency cannot be set above the AM frequency band, the alternatives of 8fs and 10fs should be used. These settings should be adjusted to avoid active AM channels.

16.19 EMI Management Features

The RTQ9124T-QA features a Spread-Spectrum function address EMI issues.

16.20 Spread-Spectrum Function

There are two methods: varying the spread spectrum frequency and adding noise to the triangular modulation.

The spread spectrum frequency variation amplitude is controlled via the register at address 0x07[1:0], and noise can be added to the triangular modulation through the register at address 0x07[6:2].

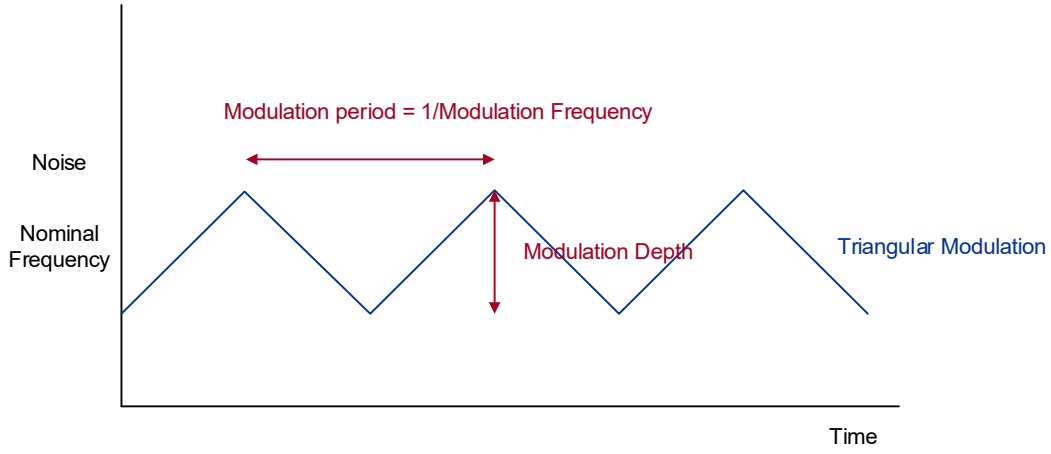


Figure 12. Spread-Spectrum Algorithm

16.21 Load Diagnostics

The device features both DC and AC load diagnostics to assess the status of the load. DC diagnostics are enabled by default via the register at address 0x04[13]. However, for a fast start-up that bypasses diagnostics, DC diagnostics can be disabled through I^2C. DC diagnostics activate when any channel transitions from the Hi-Z state to either the MUTE or Normal state. Additionally, DC diagnostics can be manually activated for any or all channels. They can commence under any operating condition; however, if a channel is in the Normal state, the diagnostic process takes longer. This delay occurs because the device must decrease the audio signal of that channel before it can switch to the Hi-Z state. DC diagnostics become available as soon as the device's power supply is within the recommended operating range. These diagnostics do not depend on the availability of audio input clocks. Results from the DC diagnostics are reported individually for each channel via the I^2C registers.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x04	2	13	RW	EN_DC_LOAD_DET	Execute DC load diagnostics before amp on sequence 0: Disable 1: Enable (default)	1

16.22 DC Load Detection

DC load detection assesses the status of the speaker side to prevent speaker damage. During this process, the device remains in a high-impedance state while playing a detection pattern. There are three types of DC load detection results: normal, S2G (short to ground), S2P (short to power), OL (open load) and SL (short load). The DC load detection method involves playing a pattern between the output channels OUTP and OUTN to diagnose the load (RL) status. DC load detection can be automatically initiated when the amplifier is powered on, as configured by bit 13 of register 0x04. It can also be manually triggered by setting bits [4] of register 0x51. The thresholds for S2G, S2P, OL and SL are controlled by registers at addresses 0x50.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x50	2	8	RW	S2P_TH	S2P threshold selection 0: 200Ω 1: 400Ω(default)	1
		7:6	RW	S2G_TH	S2P threshold selection 00: 200Ω(default) 01: 400Ω 10: 800Ω 11: reserved	00
		5:4	RW	OL_TH	OL threshold selection 00: 50Ω(default) 01: 100Ω 10: 200Ω 11: 400Ω	00
		3:0	RW	SL_TH	SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω others: reserved	0001

When the DC load detection result indicates an abnormal output channel, the device will pull the $\overline{\text{FAULT}}$ voltage low. Registers 0x17 can be read to confirm the diagnostic result and identify the abnormal output channel.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x17	2	12	RW	S2P	Output short to power 0: normal (default), 1: Warning (write 1 to clear)	0
		8	RW	S2G	Output short to ground 0: normal (default), 1: Warning (write 1 to clear)	0
		4	RW	OL	Output open load 0: normal (default), 1: Warning (write 1 to clear)	0
		0	RW	SL	Output short load 0: normal (default), 1: Warning (write 1 to clear)	0

16.23 AC Load Detection

AC load detection can help distinguish speaker types such as woofers and tweeters. For AC load detection, the device must be in the Hi-Z state. The AC load gain is configured via the volume gain register 0x38[10:0], and a recommended setting for optimal detection is -40 dB. When detection finishes, users can obtain the magnitude and phase. The method of AC diagnosis involves playing a signal frequency pattern between the output channels OUTP and OUTN to diagnose the speaker status. The diagnostic result is obtained through an internal ADC, and the parameter values can be compensated and converted internally to obtain the magnitude and phase. AC load detection can be manually executed by setting bits [4] of register 0x53. The RTQ9124DH-QA GUI provides a load diagnostics function, which allows the load detection results to be displayed through the GUI without the need for manual calculation.

16.24 Real Time Load Diagnostics

Real-time diagnostics provide an on-site monitoring function to check the speaker wire connection status, regardless of whether the RTQ9124T-QA is in ULQM or normal playback mode.

In ULQM, the RTQ9124T-QA can enable real-time DC load detection function from register 0x04, bits [11:10]. When this function is enabled, the RTQ9124T-QA automatically performs DC load detection at regular intervals. If the speaker wire is open, shorted to power, or shorted to ground, the RTQ9124T-QA can notify the system to prevent risks, even when the amplifier is not active. Faults such as open, short or short-to-power/ground are handled as interrupts, eliminating the need for continuous polling through the I^2C bus.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x04	2	11:10	RW	ULQM_DCVT	ULQM Mode DCVT Mode 00: Disable 01: DC 10: VT 11: DC+VT (default)	11

In normal playback mode, the RTQ9124T-QA features a built-in algorithm to obtain the speaker resistance in real-time from register 0x58, bits [9:8]. Unlike other products, the RTQ9124T-QA does not require DSP resources to calculate the exact speaker DCR value. With the built-in DCR algorithm, the RTQ9124T-QA can detect open load or short load by referencing the threshold settings in registers 0x4B. When the exact DCR value is available, the device can automatically reduce output gain to protect the speaker from overload. The measured DCR value is accessible via the I^2C bus for system monitoring.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x58	2	9	RW	LDET_OPEN_EN	Real Time Load Detection OPEN_EN 0: Disable 1: Enable (default)	1
0x58	2	8	RW	LDET_SHORT_EN	Real Time Load Detection SHORT_EN 0: Disable 1: Enable (default)	1

In normal playback mode, the RTQ9124T-QA has a built-in unique algorithm to obtain the speaker resistance in real-time. Unlike other products, the RTQ9124T-QA saves DSP resources by not requiring the calculation of the exact speaker DCR value. With the built-in DCR algorithm, the RTQ9124T-QA can determine open load or short load by referencing the threshold settings from registers 0x4B. Moreover, with the exact DCR value, the RTQ9124T-QA can actively decrease output gain to protect the speaker from being overloaded. The DCR value can also be read from the I²C bus for system monitoring.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x4B	2	15:8	RW	DCR_SHORT_TH	RTLD_SL_SEL = 0 (pilot only) SL_TH = X/2^3, LSB = 125mA 8'h07: 875mA (default) RTLD_SL_SEL = 1 (signal + pilot) SL_TH = X/2^4, LSB = 62.5mA 8'h07: 438mA (default)	8'h07
0x4B	2	7:0	RW	DCR_OPEN_TH	RTLD_SL_SEL = 0 (pilot only) OL_TH = X/2^11, LSB = 0.5mA 8'h10: 8mA (default) RTLD_SL_SEL = 1 (signal + pilot) OL_TH = X/2^12, LSB = 0.25mA 8'h10: 4mA (default)	8'h10

16.25 Output Voltage

There are three types of gain in the RTQ9124T-QA: digital volume gain, analog DAC gain, and speaker gain. The output voltage calculation formula is:

Output Voltage peak(Vp) = 10^ ((D + Volume Gain) / 20) x 3.5 x SPK Gain (0.5 / 1 / 2 / 4 / 5 / 6.3 / 8).

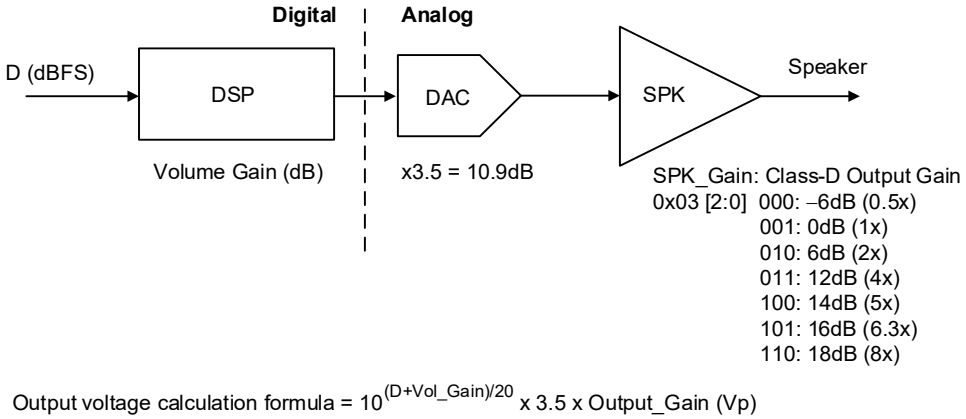


Figure 13. Output Voltage Calculation

16.26 Overcurrent Warning (IWARN)

When the overcurrent warning (IWARN) exceeds the threshold, will alert warning flag. IWARN is not reported as a fault condition to registers or the $\overline{\text{FAULT}}$ pin; instead, it is indicated as a warning condition on the WARNB pin and in the IWARN status register (address = 0x15[0]). Each channel is monitored and limited independently. Four programmable levels can be configured using two bits in the register at address 0x60[0].

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x15	2	0	RW	IWARN_Flag	Over current warning flag 0: Normal (default) 1: Warning	0

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x60	2	0	RW	IWARN_SEL	Over current warning threshold selection 0: 5A (default) 1: 5.5A	0

16.27 Overcurrent Protection (OCP)

The RTQ9124T-QA features an Overcurrent Protection (OCP) function to prevent damage to the device under overload or short-circuit conditions. This function is monitored by an internal sensing circuit. If the output current reaches the OC threshold, such as in case of an output short to GND, a peak current limit is triggered, which by default shuts down the channel in latch mode. Users can also select an auto-recovery mode for different applications.

16.28 DC Detection

During normal operation, the amplifier circuit continuously monitors the DC offset. If the DC offset exceeds a specified threshold, the channel is placed in the Hi-Z state, a fault is reported to the I^2C register, and the $\overline{\text{FAULT}}$ pin is activated. Optionally, register bits can be configured to mask this fault report to the $\overline{\text{FAULT}}$ pin. This monitoring is crucial for protecting the loudspeaker from DC at the output. The detection method involves analyzing the DC at the final PWM stage, calculating the difference between the PWM output and a Sinc filter to determine the DC level. The IC will automatically shut down upon detecting excessive DC.

16.29 Temperature and Voltage Sensing

Voltage Sensing:

Voltage sense monitors the PVDD voltage between the range from 4.5V to 18V, the output is shown in the register “0x0A with the equation battery voltage (V) = PVDD code (DEC) / 160.

Temperature Sensing:

Temperature sense monitors the temperature, the output is shown in the register 0x0B “Sense temp” with the equation code (DEC) = temperature(K) = temperature (°C) - 273.

16.30 Over-Temperature Warning (OTW) and Over-Temperature Protection (OTP)

The device offers four over-temperature warning levels (see the Register Map section for threshold values). When the junction temperature surpasses a warning level, the WARNB pin is activated unless the mask bit in the pin control register (address 0x21) is configured to disable this alert. The device operates normally until it reaches the OTSD threshold, at which point it places all channels in Hi-Z state and activates the $\overline{\text{FAULT}}$ pin. By default, the

device remains deactivated until the temperature normalizes. However, this behavior can be modified to automatic recovery by setting bits 2 in the Miscellaneous Control register (address 0x0D). Upon normalization of the junction temperature, the device automatically resumes operation and restores the channels to the configurations specified in the state control register. It is important to note that, even with automatic recovery enabled, the $\overline{\text{FAULT}}$ pin stays active until the CLEAR $\overline{\text{FAULT}}$ bit (bit 1) in the register (address 0x11) is activated.

16.31 Undervoltage (UV) and Power-On-Reset (POR)

The RTQ9124T-QA monitors the PVDD pin voltage threshold. When the voltage at the PVDD pin drops below the programmable undervoltage threshold of 4V, the Undervoltage Protection (UVP) circuit immediately shuts down the output. This device can also be configured to operate in latch mode instead.

When the DVDD voltage is set to 3.3V, the DVDD UVP (Undervoltage Protection) is configured to 2.8V. If the DVDD operating voltage is 1.8V, then the VR_DIG pin must also be supplied with 1.8V, and the register must be configured to lower the DVDD UVP to 1.4V.

16.32 Overvoltage (OV) and Load Dump

The RTQ9124T-QA monitors the voltage thresholds of the PVDD pin. When the voltage on the PVDD pin rises above the overvoltage threshold of 19.5V, the OVP circuit immediately shuts down the output. The device can then operate in auto-recovery mode or be configured to use latch mode.

16.33 Clip Detection

Clip detection is reported on the WARNB pin if a 100% duty-cycle PWM is sustained for a minimum number of PWM cycles as set by the Clip Window Register (address 0x5D). The default setting is 20 PWM cycles.

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x5A	2	0	RW	EN_CLIP_AGB	Enable auto gain control for CLIP detection, 0: Disable (default) 1: Enable	0

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x5D	2	3:0	RW	CLIP_DET_SEL	Clip detect threshold, release threshold (unit: PWM cycle) 0000: 1, 0 0001: 5, 3 0010: 10, 5 0011: 20, 5 (default) Others: Reserved	0011

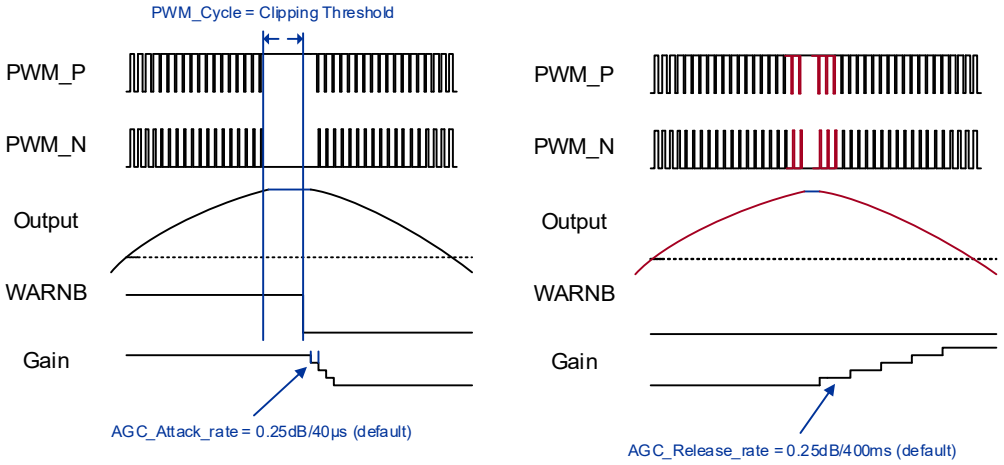


Figure 14. Clip Detection

16.34 Thermal Fold-Back (TFB)

The RTQ9124T-QA features built-in Thermal Fold-Back protection (TFB), which is activated when the average junction temperature exceeds a specified threshold. TFB decreases the amplifier gain to reduce power dissipation, maintaining the junction temperature around the threshold level. The device will not completely switch off but will remain operational at lower output power levels. If the average junction temperature continues to rise, a second built-in temperature protection threshold will shut down the amplifier completely.

16.35 Recommended Operating Conditions

The RTQ9124T-QA is designed for specific application conditions. It supports speakers with a typical impedance of 4Ω and a minimum impedance of 2Ω.

Minimum Speaker Load Impedance		
Min	**Typ**	**Max**
2Ω	4Ω	--

Based on the internal settings of the RTQ9124T-QA and the LDMOS parameters, recommended application ranges are provided for the corresponding loaded speaker impedance and PVDD voltage.

Speaker Load	**PVDD Range**		
R_L (Ω)	**Min**	**Typ**	**Max**
2	4.5V	--	14.5V

16.36 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TSSOP-28 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 30.39°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (30.39°C/W) = 3.29W for a TSSOP-28 (Exposed Pad) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}.

The derating curve in Figure 15 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

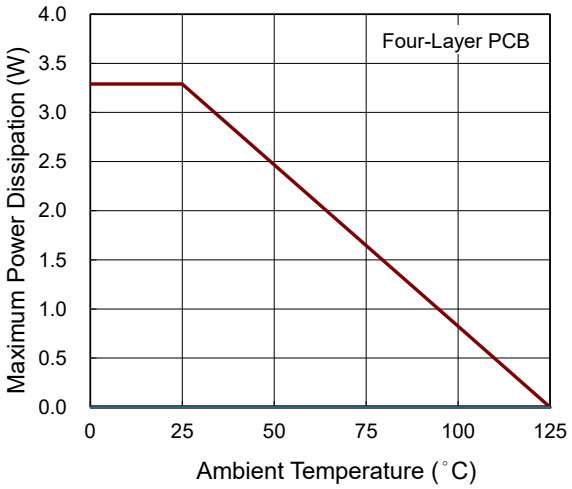
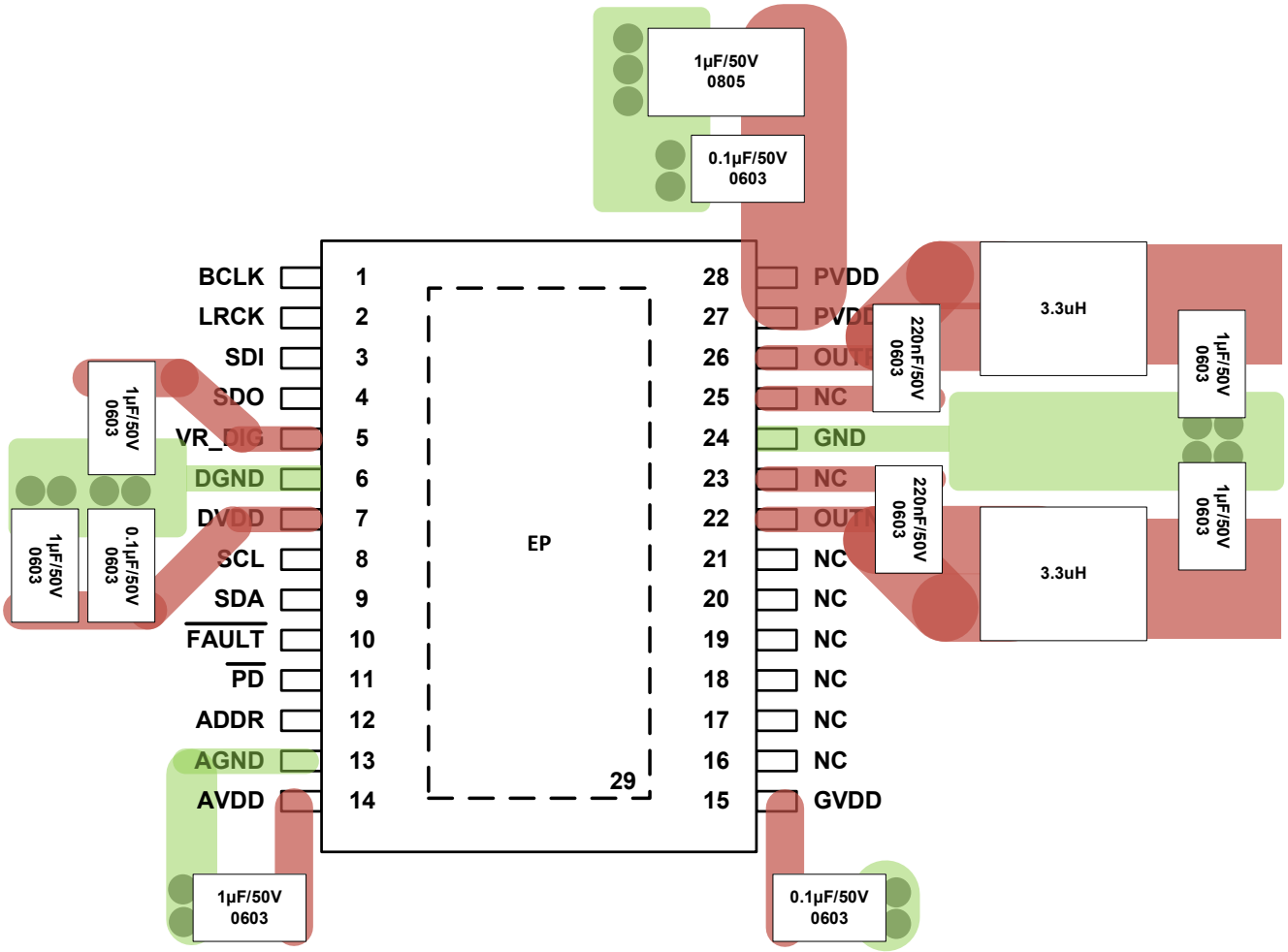


Figure 15. Derating Curve of Maximum Power Dissipation

16.37 Layout Consideration

1. In the RTQ9124T pin configuration, the digital signal pins and power pins have been separated. Digital signal traces and power traces must be separated, and layout traces should not cross. Use a star grounding structure, gathering all grounding points to a central point. The trace from VSYS or Battery side to the PVDD pin must be wide enough to meet the current demand.
2. Pins 27 and 28 are PVDD power pins for the Class-D structure application. Place the filter capacitors as close as possible to the PVDD pins and use the shortest possible traces to connect these capacitors. Capacitors with smaller capacitance should be placed near the PVDD pins. To reduce parasitic inductance and resistance, use multiple vias to connect to the main ground. The optimal approach is to use vias that are directly connected to the Main GND. Before making this connection, ensure that the vias are isolated to prevent unintended connections with other grounds.
3. The ground defined by the AVDD pin is AGND, and the ground defined by the VR_DIG pin is DGND. Place the bypass capacitors as close as possible to the reference ground pins and use the shortest possible traces to connect these capacitors.



4. The traces for OUTP and OUTN should have equal widths and lengths to ensure balanced performance. When using an inductor or a ferrite bead filter, place it close to the chip for optimal EMI performance. It is recommended to position ground vias around the output traces to enhance grounding effectiveness.
5. Due to the many external traces, the ground of the RTQ9124T is connected to the MAIN GND using vias. Copper can be placed under the IC, and additional GND vias can be used to better connect the PGND pin on the top layer to the MAIN GND. This approach can also increase the heat dissipation area.

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Functional Register Description

17.1 I²C Command

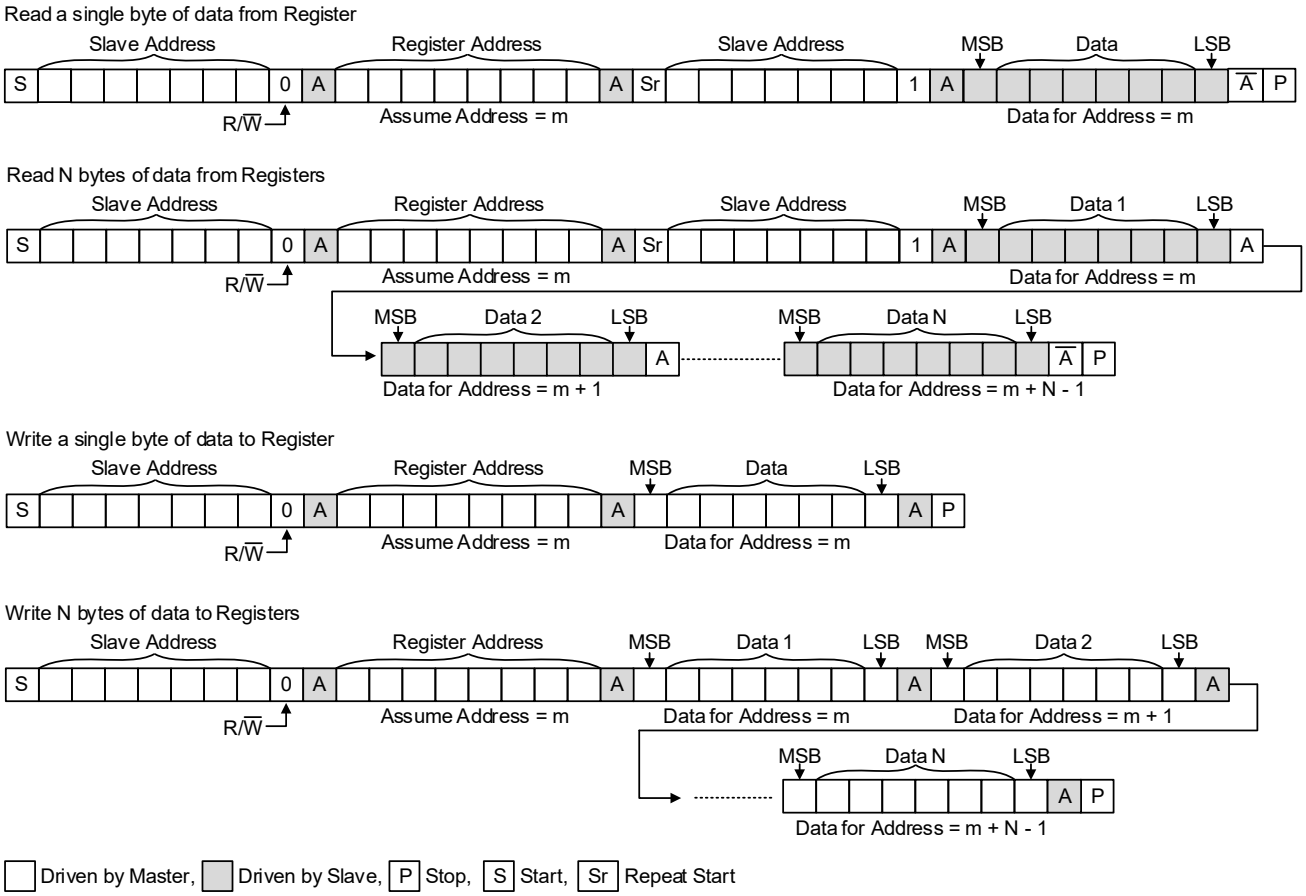


Figure 16. Read and Write Functions

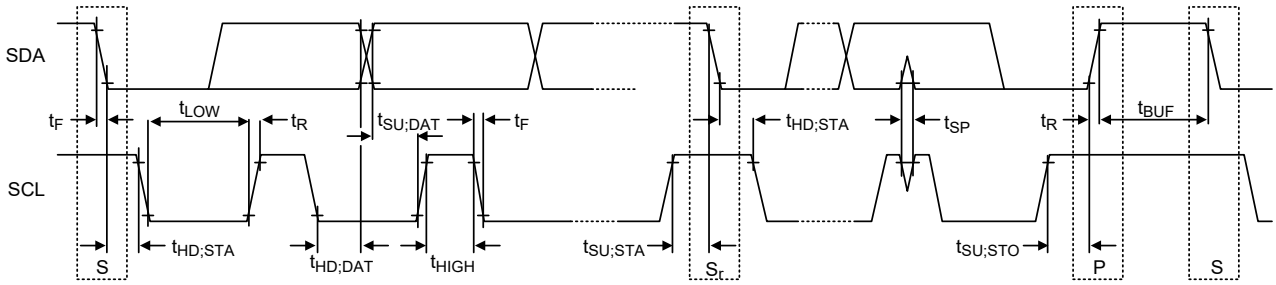


Figure 17. I²C Waveform Information

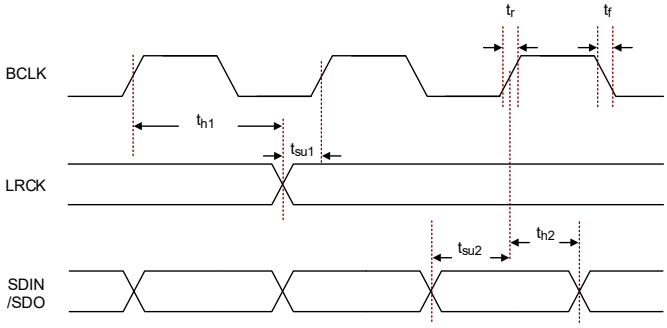


Figure 18. Timing Diagram of Slave Mode I²S Interface

Table 2. Register Map

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x00	2	8	RW	Reserved	Reserved	1
0x00	2	1:0	RW	CH_SI	I²S channel selection 01: L channel (default) 10: R channel Others: (L+R)/2	01
0x01	2	9	RW	CS_DATA_INV	Current sense data output inversion 0: Normal 1: Inverted (Default)	1
0x01	2	8	RW	Reserved	Reserved	0
0x01	2	7:4	RW	SDO_SEL_L	Left channel data 0000: No output (default) 0001: I²S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Revered	0000
0x01	2	3:0	RW	SDO_SEL_R	Right channel data 0000: No output (default) 0001: I²S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Reserved	0000
0x02	2	7	RW	BCLK_EDGE_SEL	0: LRCK transition align with BCLK falling (default) 1: LRCK transition align with BCLK rising	0
0x02	2	6	RW	SDO_EDGE_SEL	I²S data out launch edge selection 0: BCLK_EDGE_SEL=0, launch with falling edge (default) 1: BCLK_EDGE_SEL=0, launch with rising edge	0
0x02	2	5:4	RW	AUD_BITS	00: 16 bits 01: 20 bits 10: 20 bits 11: 24 bits (default)	11
0x02	2	3	RW	TDM_DSP_OFFSET	TDM or DSPM offset selection 0: Without offset (DSPMB) 1: 1 bit clock offset (DSPMA) (default)	1
0x02	2	2:0	RW	AUD_FMT	000: I²S (default) 001: Left Justify 010: Right Justify 011: DSP mode 100: EIAJ Others: TDM mode	000

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x03	2	9	RW	EN_5V_APP	Enable when PVDD=5V application 0: Disable (default) 1: Enable	0
0x03	2	8	RW	MODU_MODE	Reserved for new feature 0: BTL mode (default) 1: CMH mode	0
0x03	2	6:4	RW	PWM_FREQ	PWM frequency selection 000: 8*fs 001: 10*fs 010: 40*fs 011: 44*fs (default) 100: 48*fs Others: Reserved	011
0x03	2	2:0	RW	SPK_GAIN_SEL	Speaker gain selection 000: -6dB (0.5x) 001: 0dB (1x) 010: 6dB (2x) 011: 12dB (4x) 100: 14dB (5x) 101: 16dB (6.3x) 110: 18dB (8x) (default) 111: Reserved	110
0x04	2	15	W	SF_RESET	Write 1 to trigger software reset	0
0x04	2	13	RW	EN_DC_LOAD_DET	Execute DC load diagnostics before amp on sequence 0: Disable 1: Enable (default)	1
0x04	2	12	RW	LDET_Operatoin_EN	Real Time Load Detection Mode_EN 0: Disable 1: Enable (default)	1
0x04	2	11:10	RW	ULQM_DCVT	ULQM Mode DCVT Mode 00: Disable 01: DC 10: VT 11: DC+VT (default)	11
0x04	2	8	RW	LDET_Operatoin	Real Time Load Detection Mode 0: CS 1: DCR (default)	1
0x04	2	1:0	RW	CH_STATE	Channel Mode 00: Normal 01: Hi-Z (default) 10: MUTE 11: ULQM	01
0x05	2	2:0	RW	OUT_PHASE	PWM output phase offset 000: 0 (default) 001: 45 010: 90 011: 135 100: 180 101: 225 110: 270 111: 315	000

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x06	2	7	RW	SIL_DET_EN	ULQM detection enable 0: Disable 1: Enable (default)	1
0x06	2	5:4	RW	SIL_TH_SEL	ULQM mode detection threshold (in different AUD_BITS setting) 00: Audio data <= +/- 7 01: Audio data <= +/- 3 10: Audio data <= +/- 1 11: All data zero (default)	11
0x06	2	2:0	RW	SIL_HOLD_TIME	ULQM mode hold time selection 000: 1ms 001: 20ms 010: 40ms (default) 011: 80ms 100: 160ms 101: 320ms 110: 640ms 111: 1.28s	010
0x07	2	7	RW	FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable	0
0x07	2	6	RW	PWM_MODEWHITE	Noise selection 0: Pink noise (default) 1: White noise	0
0x07	2	5	RW	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4	0
0x07	2	4	RW	PWM_NOISE_EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable	0
0x07	2	3:2	RW	NOISE_AMP	Nosie amplitude for SSC 00: 6.3% (default) 01: 11.7% 10: 17.1% 11: 35.1%	00
0x07	2	1:0	RW	FSS_AMP	Spread spectrum frequency variation amplitude 00: 14.73% 01: 22.5% (default) 10: 22.5% 11: 30.35%	01
0x08	2	9	RW	VTMNT_EN	EN VT-monitor Gating CK_SAMPLE_SAR_ADC & CK_COMP_SAR_ADC 0: Disable 1: Enable (default)	1
0x08	2	8	RW	HPF_EN_ISNS	Digital high-pass filter for I-sense 0: Disable 1: Enable (default)	1
0x08	2	7	RW	ISENSE_EN	I-sense 0: Disable 1: Enable (default)	1

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x08	2	6	RW	HPF_EN	High-Pass filter enable 0: Disable 1: Enable (default)	1
0x08	2	5	RW	COMP_EN	Compensation filter enable 0: Disable (default) 1: Enable (not available at 192kHz sampling Rate)	0
0x08	2	4	RW	DRC_EN	DRC enable 0: Disable (default) 1: Enable	0
0x08	2	3	RW	DRC_N_EN	DRC noise gate enable 0: Disable (default) 1: Enable	0
0x08	2	2	RW	HARD_CLIP_EN	Hard clip enable 0: Disable (default) 1: Enable	0
0x08	2	1	RW	DRE_EN	DRE enable 0: Disable 1: Enable (default)	1
0x08	2	0	RW	MS_MUTE	Mute function 0: Un-mute (default) 1: Master soft mute	0
0x09	2	6	RW	FAULT_B_WARNB_EN	$\overline{\text{FAULT}}$ output status 0: Non-Active 1: Active when fault event and diagnostic(default)	1
0x09	2	5	RW	WARN_B_TYPE	WARNB status 0: Fault status (Recovery type) 1: Interrupt Reg (Latch type) (default)	1
0x09	2	4	RW	FAULT_B_TYPE	$\overline{\text{FAULT}}$ status 0: Fault status (Recovery type) 1: Interrupt Reg (Latch type) (default)	1
0x09	2	3:0	RW	RCVRY_TIME	Power Stage auto recovery time 0000: 100ms 0001: 150ms 0010: 300ms (default) 0011: 450ms 0100: 600ms 0101: 750ms 0110: 900ms 0111: 1050ms 1000: 1200ms 1001: 1350ms Others: 1500ms	0010
0x0A	2	12:0	R	PVDD_MNT_CODE	Voltage of PVDD(Volt) = PVDD_MNT_CODE/160	13'h0000
0x0B	2	8:0	R	TEMP_MNT_CODE	Temperature(K) = Temperature(°C) - 273	9'h000
0x0C	2	3	RW	I2S_FAULT_TYPE	I^2S fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0C	2	2	RV	Reserved	Reserved	0

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x0C	2	1	RW	UVP_DVDD_TYPE	UVP DVDD fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0C	2	0	RW	UVP_PVDD_28_TYPE	UVP PVDD_28 fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	7	RW	OVP_PVDD_28_TYPE	OVP PVDD_28 fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	6	RW	UVP_VDDA_TYPE	UVP VDDA fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	5	RW	UVP_PVDD_TYPE	UVP PVDD fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	4	RW	OVP_PVDD_TYPE	OVP PVDD fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	2	RW	OTP_TYPE	OTP fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	1	RW	OCP_TYPE	OCP fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0E	2	15:6	RV	Reserved	Reserved	10'h0000
0x0E	2	5	RW	RTLD_SL_SEL	Real time load detect short load selection 0: Pilot only (default) 1: Signal + Pilot	0
0x0E	2	4	RW	RTLD_OL_SEL	Real time load detect open load selection 0: Pilot only (default) 1: Signal + Pilot	0
0x0E	2	3:2	RV	Reserved	Reserved	2'h00
0x0E	2	1	RW	RTLD_PROT_SEL	RTLD protection select 0: DCR auto recovery (default) 1: DCR latch	0
0x0E	2	0	RW	LD_REF_SEL	Manual mode DC/AC load diagnostic clock source selection 0: Reference internal clock (default) 1: Reference BCLK	0
0x0F	2	7:0	R	ERR_INT_INDEX	Report ERR_INT summary from ERR_INT0 (0x10) ~ ERR_INT7 (0x17)	8'h01
0x10	2	6	RW	POR	Power-on reset 0: Normal 1: Warning (write 1 to clear) (default)	1
0x10	2	5	RW	ADS_ERR	Address R detection error I^2C_ADDR 0: R detect correct (default) 1: R detect error (write 1 to clear)	0
0x10	2	4	RW	Reserved	Reserved	0

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x10	2	3	RW	PWM_ERR	PWM frequency setting error under sampling rate 0: PWM is supported (default) 1: PWM is non-supported (write 1 to clear)	0
0x10	2	2	RW	PLL_UNLOCK	0: No PLL unlock error (default) 1: PLL Unlock error (write 1 to clear)	0
0x10	2	1	RW	BCLK_ERR	0: No BCLK error (default) 1: BCLK error (write 1 to clear flag)	0
0x10	2	0	RW	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error (write 1 to clear)	0
0x11	2	7	RW	VDDA_UV	VDDA UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	5	RV	Reserved	Reserved	0
0x11	2	4	RW	DVDD_UV	DVDD UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	3	RW	PVDD_28_UV	PVDD_28 UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	2	RW	PVDD_28_OV	PVDD_28 OVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	1	RW	OTP	OTP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	0	RW	OTW	OT warning 0: Normal (default) 1: Warning (write 1 to clear)	0
0x12	2	6	RW	PVDD_UV	PVDD UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x12	2	4	RW	PVDD_OV	PVDD OVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x12	2	0	RW	DCP	Output DC detected flag 0: Normal (default) 1: fault (write 1 to clear)	0
0x13	2	0	RW	OCP	Channel OCP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x15	2	4	RW	CLIP	Clip detection 0: Normal (default) 1: Warning (write 1 to clear)	0
0x15	2	0	RW	IWARN	Over current warning flag 0: Normal (default) 1: Warning (write 1 to clear)	0
0x16	2	8	RW	LDET_SHORT	LDET short error flag 0: Normal (default) 1: Current error is triggered (write 1 to clear)	0

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x16	2	4	RW	LDET_OPEN	LDET open error flag 0: Normal (default) 1: Open is triggered (write 1 to clear)	0
0x17	2	12	RW	S2P	Output short to power 0: Normal (default) 1: Warning (write 1 to clear)	0
0x17	2	8	RW	S2G	Output short to ground 0: Normal (default) 1: Warning (write 1 to clear)	0
0x17	2	4	RW	OL	Output open load 0: Normal (default) 1: Warning (write 1 to clear)	0
0x17	2	0	RW	SL	Output short load 0: Normal (default) 1: Warning (write 1 to clear)	0
0x20	2	3	RW	MASK_PWM_ERR	Fault mask for PWM setting error 0: Not mask (default) 1: Mask	0
0x20	2	2	RW	MASK_PLL_FAULT	Fault mask for PLL unlock error 0: Not mask (default) 1: Mask	0
0x20	2	0	RW	MASK_I2S_FAULT	Fault mask for BCLK/LRCK error 0: Not mask (default) 1: Mask	0
0x21	2	7	RW	MASK_UV_VDDA	Fault mask for VDDA UV 0: Not mask (default) 1: Mask	0
0x21	2	5	RV	Reserved	Reserved	0
0x21	2	4	RW	MASK_UV_DVDD	Fault mask for DVDD UV 0: Not mask (default) 1: Mask	0
0x21	2	3	RW	MASK_UV_PVDD_28	Fault mask for PVDD_28 UV 0: Not mask (default) 1: Mask	0
0x21	2	2	RW	MASK_OV_PVDD_28	Fault mask for PVDD_28 OV 0: Not mask 1: Mask (default)	1
0x21	2	1	RW	MASK_OTP	Fault mask for OTP 0: Not mask (default) 1: Mask	0
0x21	2	0	RW	MASK_OTW	Fault mask for OTW 0: Not mask (default) 1: Mask	0
0x22	2	6	RW	MASK_UV_PVDD	Fault mask for PVDD UV 0: Not mask (default) 1: Mask	0
0x22	2	4	RW	MASK_OV_PVDD	Fault mask for PVDD OV 0: Not mask (default) 1: Mask	0
0x22	2	0	RW	MASK_DCP	Fault mask for DCP 0: Not mask (default) 1: Mask	0

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x23	2	0	RW	MASK_OCP	Fault mask for OCP 0: Not mask (default) 1: Mask	0
0x25	2	4	RW	MASK_CLIP	Fault mask for chip detection 0: Not mask (default) 1: Mask	0
0x25	2	0	RW	MASK_IWARN	Fault mask for current limit 0: Not mask (default) 1: Mask	0
0x26	2	8	RW	MASK_LDET_SHORT	Fault mask for LDET SHORT 0: Not mask (default) 1: Mask	0
0x26	2	4	RW	MASK_LDET_OPEN	Fault mask for LDET OPEN 0: Not mask (default) 1: Mask	0
0x27	2	12	RW	MASK_S2P	Fault mask for S2P 0: Not mask (default) 1: Mask	0
0x27	2	8	RW	MASK_S2G	Fault mask for S2G 0: Not mask (default) 1: Mask	0
0x27	2	4	RW	MASK_OL	Fault mask for OL 0: Not mask (default) 1: Mask	0
0x27	2	0	RW	MASK_SL	Fault mask for SL 0: Not mask (default) 1: Mask	0
0x30	2	3	RW	I2C_TIMEOUT_TIME_SEL	I²C timeout timing selection 0: 100ms (default) 1: 150ms	0
0x30	2	2	RW	I2C_TIMEOUT_TYPE_SEL	I²C timeout check pin type 0: SCL & SDAO both keep low start timeout counting 1: SDAO keep low start timeout counting (default)	1
0x30	2	1	RW	I2C_TIME_OUT_SEL	I²C timeout reset selection 0: Reset I²C IP only (default) 1: Reset whole chip	0
0x30	2	0	RW	I2C_TIME_OUT_EN	I²C timeout function: If SDA&SCL keep low 100ms, I²C timeout reset occur. 0: Disable 1: Enable (default)	1
0x31	2	7	R	PWM_STATUS	PWM status 0: Sampling rate vs. PWM frequency is supported (default) 1: Sampling rate vs. PWM frequency is non-supported	0
0x31	2	6:4	RW	SR_MODE	Sampling rate (manual setting or report) If auto sampling rate detection, SR_MODE reports detection result. 100: 32KHz 101: 44.1/48KHz (default) 110: 88.2/96KHz	101

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
					111: 192KHz Others: Reserved	
0x31	2	3:0	RW	BCLK_MODE	BCLK mode report 0000: BCLK=32fs 0001: BCLK=48fs 0010: BCLK=64fs (default) 0011: BCLK=96fs 0100: BCLK=128fs 0101: BCLK=192fs (not support 192K-SR) 0110: BCLK=256fs (not support 192K-SR) 0111: BCLK=384fs (not support 96K-SR , 192K-SR) 1000 : BCLK=512fs (not support 96K-SR , 192K-SR) others : Reserved	0010
0x32	2	5:0	RW	TDM_TX_LOC_CH1	TDM start transmitting location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000000
0x33	2	5:0	RW	TDM_TX_LOC_CH2	TDM start transmitting location select for CH2 000000: Start from 0+offset 000001: Start from 8+offset … 000100: Start from 32+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000100
0x34	2	5:0	RW	TDM_RX_LOC_CH1	TDM start receiving location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000000
0x35	2	5:0	RW	TDM_RX_LOC_CH2	TDM start receiving location select for CH2 000000: Start from 0+offset 000001: Start from 8+offset … 000100: Start from 32+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000100
0x36	2	6	RW	DRC_IN_SEL	DRC Static Curve input selection 0: Audio input 1: DCR calibration result (default)	1

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x36	2	5	RW	DRC_PEAK	DRC mode selection 0: RMS Mode 1: Peak Mode (default)	1
0x36	2	4	RW	DRC_GAIN_HYS_EN	DRC gain hysteresis enable 0: Disable, 1: Enable (default) Gain release condition is gain difference >= 0.125dB	1
0x36	2	2	RW	VTMNT_CLK_SEL	0: t=1/96k/32 1: t=1/48k/32 (default) 96k/48k is sampling rate (LRCK)	1
0x36	2	1:0	RW	VTMNT_AVG_SEL	00: avg*1 (default) 01: avg*2 10: avg*4 11: avg*8	00
0x37	2	7	RW	SKIP_RAMP	Skip volume ramp 0: Disable (default) 1: Enable	0
0x37	2	6	RW	FAST_RAMP_MUTE	Mute pin fast mute, mute time < 1ms 0: Normal ramp time (default) 1: Fast mute time	0
0x37	2	5	RW	MUTE_MODE	Mute pin behavior 0: Mute only (default) 1: Enter ULQM	0
0x37	2	1:0	RW	VOL_RAMP_MODE	Volume slew step control 00: 4.33ms from mute to 0dB (0.5dB/20.83us) 01: 8.66ms from mute to 0dB (0.25dB/20.83us) 10: 17.33ms from mute to 0dB (0.125dB/20.83us) 11: 34.65ms from mute to 0dB (0.0625dB/20.83us) (default)	11
0x38	2	10:0	RW	VOL	Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180
0x39	2	10:0	RW	HC_TH	Hard clip threshold when HARD_CLIP_EN=1 11'h18D: -0.8125dB (default) 0.0625db per step	11'h18D
0x3A	2	10:0	RW	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: -24dB 11'h67E: -103.875dB 11'h67F~11'h7FF: not available 0.0625dB per step	11'h000
0x3B	2	10:0	RW	DRC_OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: -103.9375dB 0.0625dB per step	11'h180
0x3C	2	7:0	RW	DRC_RATIO	DRC compress ratio 8'h00: No compression 8'h80 (default) ~8'hFF: Full compression 1/128 per step	8'h80

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x3D	2	10:0	RW	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: -24dB 11'h640: -100dB (default) 1'h67E: -103.875dB 11'h67F~11'h7FF: not available 0.0625dB per step	11'h640
0x40	4	16:0	RW	DRC_AE	DRC_AE	17'h08000
0x41	4	16:0	RW	DRC_1_AE	DRC_1_AE	17'h00000
0x42	4	16:0	RW	DRC_AA	DRC_AA	17'h08000
0x43	4	16:0	RW	DRC_AD	DRC_AD	17'h08000
0x44	4	16:0	RW	COMP_B0	Compensation filter coefficient B0	17'h08000
0x45	4	16:0	RW	COMP_B1	Compensation filter coefficient B1	17'h00000
0x46	4	16:0	RW	COMP_B2	Compensation filter coefficient B2	17'h00000
0x47	4	16:0	RW	COMP_B3	Compensation filter coefficient B3	17'h00000
0x48	2	7:0	RW	PILOT_FREQ	W0 = (2*pi*fpil/fs)*2^15, Default = 18.65Hz	8'h50
0x49	2	10:0	RW	PILOT_GAIN	Gain = (24 - pilot_gain/16)dB 11'h0400: -40dB (default)	11'h400
0x4A	2	7:0	RW	DCR_EST_MU	4.4 format, Mu = x/2^4, Default = 0.75	8'h0C
0x4B	2	15:8	RW	DCR_SHORT_TH	RTLD_SL_SEL = 0 (pilot only) SL_TH = X/2^3, LSB = 125mA 8'h07: 875mA (default) RTLD_SL_SEL = 1 (signal + pilot) SL_TH = X/2^4, LSB = 62.5mA 8'h07: 438mA (default)	8'h07
0x4B	2	7:0	RW	DCR_OPEN_TH	RTLD_SL_SEL = 0 (pilot only) OL_TH = X/2^11, LSB = 0.5mA 8'h10: 8mA (default) RTLD_SL_SEL = 1 (signal + pilot) OL_TH = X/2^12, LSB = 0.25mA 8'h10: 4mA (default)	8'h10
0x4D	2	13:0	RW	DCR_INIT	Init_dcr = x/2^9, Default = 4ohm	14'h0800
0x4E	2	13:0	RW	Dmg_DCR	Dmg_dcr = x/2^9, Default = 31.99ohm	14'hFFFF
0x4F	2	13:0	R	DCR_RPT	DCR calculation result = x/2^9, Default = 4ohm	14'h0800

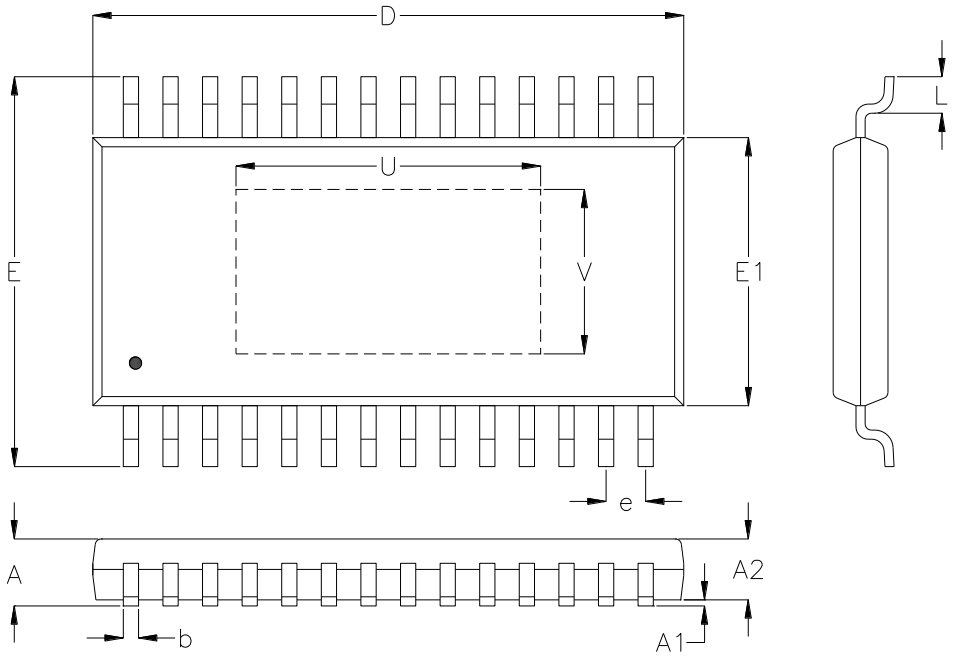
ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x50	2	8	RW	S2P_TH	S2P threshold selection 0: 200Ω 1: 400Ω (default)	1
0x50	2	7:6	RW	S2G_TH	S2G threshold selection 00: 200Ω (default) 01: 400Ω 10: 800Ω 11: Reserved	00
0x50	2	5:4	RW	OL_TH	OL threshold selection 00: 50Ω (default) 01: 100Ω 10: 200Ω 11: 400Ω	00
0x50	2	3:0	RW	SL_TH	SL threshold selection (0.5Ω each step) 0000: 0.5Ω 0001: 1Ω (default) 0010: 1.5Ω ... 1001: 5Ω Others: Reserved	0001
0x51	2	4	RW	EN_DC_DET	DC load detection enable 0: Disable (default) 1: Enable	0
0x51	2	0	R	DC_DET_DONE	DC detection done flag after enabling DC load detection 0: DC load detection not execute or not finish (default) 1: DC load detection finish	0
0x52	2	4:0	RW	AC_PHI	Generated signal frequency: 00000: no signal 00001: set 1 = 1kHz 00010: set 2 = 2kHz … 10011: set 19 = 19kHz (default) Others: Reserved	10011
0x53	2	4	RW	EN_AC_DET	AC load detection enable 0: Disable (default) 1: Enable	0

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x53	2	0	R	AC_DET_DONE	AC detection done flag after enabling AC load detection 0: AC_PHASE_R and AC_PHASE_I keep the last result if ever enabling detection (default) 1: AC_PHASE_R and AC_PHASE_I is valid	0
0x54	2	15:0	R	AC_MAG	Report magnitude	16'h0000
0x55	2	15:0	R	AC_PHA	Report phase	16'h0000
0x56	2	15:0	R	AC_SPK_R	Report the real part of speaker phase	16'h0000
0x57	2	15:0	R	AC_SPK_I	Report the imaginary part of speaker phase	16'h0000
0x58	2	9	RW	LDET_SHORT_EN	Real time load detection SHORT_EN 0: Disable 1: Enable (default)	1
0x58	2	8	RW	LDET_OPEN_EN	Real time load detection OPEN_EN 0: Disable 1: Enable (default)	1
0x58	2	6	RW	EN_OTP	Channel OT protection enable 0: Disable 1: Enable (default)	1
0x58	2	5	RW	EN_OTW	Channel OT warning enable 0: Disable 1: Enable (default)	1
0x58	2	4	RW	EN_UVOVOT	Enable UV/OV/OT 0: Disable 1: Enable (default)	1
0x58	2	3	RW	EN_IWARN	Enable over current warning function 0: Disable 1: Enable (default)	1
0x58	2	2	RW	EN_DC_PROT	DC protection enable 0: Disable 1: Enable (default)	1
0x58	2	1	RW	EN_CLIP_DET	Clip detection enable 0: Disable (default) 1: Enable	0
0x59	2	13:12	RW	OC_RCVRY_TIME	DCR OC auto recovery time 00: 50ms 01: 150ms 10: 300ms (default) 11: 450ms	10
0x59	2	11:10	RW	OPEN_DET_TIME	DCR open detection time 00: 25ms 01: 50ms (default) 10: 125ms 11: 250ms	01
0x59	2	9:8	RW	CURRENT_ERR_RCVRY_TIME	DCR current error auto recovery time 00: 50ms 01: 150ms (default) 10: 300ms 11: 450ms	01

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x5A	2	6	RW	DVDD_UV_CTRL_SEL	DVDD UV protection behavior 0: Mute discharge time then HZ_PROT (default) 1: Fast ramp mute to off sequence	0
0x5A	2	5	RW	PVDD_PVDD_28_UV_CTRL_SEL	PVDD PVDD_28 UV protection behavior 0: Mute discharge time then HZ_PROT (default) 1: Fast ramp mute to off sequence	0
0x5A	2	4	RW	OV_CTRL_SEL	DVDD PVDD PVDD_28 protection behavior 0: Mute discharge time then HZ_PROT (default) 1: HZ_PROT directly	0
0x5A	2	2	RW	EN_OTW_TFB	Enable thermal fold-back 0: Disable (default) 1: Enable	0
0x5A	2	0	RW	EN_CLIP_AGC	Enable auto gain control for CLIP detection 0: Disable (default) 1: Enable	0
0x5B	2	7:6	RW	TFB_ATTACK_RATE	Thermal foldback attack rate 00: 0.0625dB/25ms (default) 01: 0.0625dB/50ms 10: 0.0625dB/100ms 11: 0.0625dB/200ms	00
0x5B	2	5:4	RW	TFB_RELEASE_RATE	Thermal foldback release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms	00
0x5B	2	3:2	RW	AGC_ATTACK_RATE	AGC attack time selection for clip AGC 00: 0.25dB/20us 01: 0.25dB/40us (default) 10: 0.25dB/80us 11: 0.25dB/160us	01
0x5B	2	1:0	RW	AGC_RELEASE_RATE	AGC release time selection for clip AGC 00: 0.25dB/200ms 01: 0.25dB/400ms (default) 10: 0.25dB/800ms 11: 0.25dB/1600ms	01
0x5C	2	15:14	RV	Reserved	Reserved	01
0x5C	2	13:12	RW	OV_PVDD_28_SEL	OV threshold selection of PVDD_28 00: 18.8V 01: 19.5V (default) 10: 20V 11: Reserved	01
0x5C	2	11:10	RW	OV_PVDD_SEL	OV threshold selection of PVDD 00: 18.8V 01: 19.5V (default) 10: 20V 11: Reserved	01
0x5C	2	9:8	RW	UV_DVDD_SEL	UV threshold selection of DVDD 00: 1.4V (default) 01: 2.8V Others: Reserved	00

ADDR	Byte Number	BITS	Type	Reg Name	Description	Default
0x5C	2	5:4	RW	UV_PVDD_28_SEL	UV threshold selection of PVDD_28 00: 4V (default) 01: 6V 10: 7V 11: 9.1V	00
0x5C	2	1:0	RW	UV_PVDD_SEL	UV threshold selection of PVDD 00: 4V (default) 01: 6V 10: 7V 11: 9.1V	00
0x5D	2	5:4	RW	OTP_SEL	Channel OTP threshold selection 00: 160C 01: 170C (default) Others: Reserved	01
0x5D	2	3:0	RW	CLIP_DET_SEL	Clip detect threshold, release threshold (unit: PWM cycle) 0000: 1, 0 0001: 5, 3 0010: 10, 5 0011: 20, 5 (default) Others: Reserved	0011
0x60	2	0	RW	IWARN_SEL	Over current warning threshold selection 0: 5 A (default) 1: 5.5 A	0
0x61	2	2	RW	DC_TIME_SEL	DC Detection time 0: 342ms (default) 1: 684ms	0
0x61	2	1:0	RW	DC_TH	DC threshold for DC detection 00: No available 01: 12.5% (default) 10: 18.75% 11: 25%	01

18 Outline Dimension

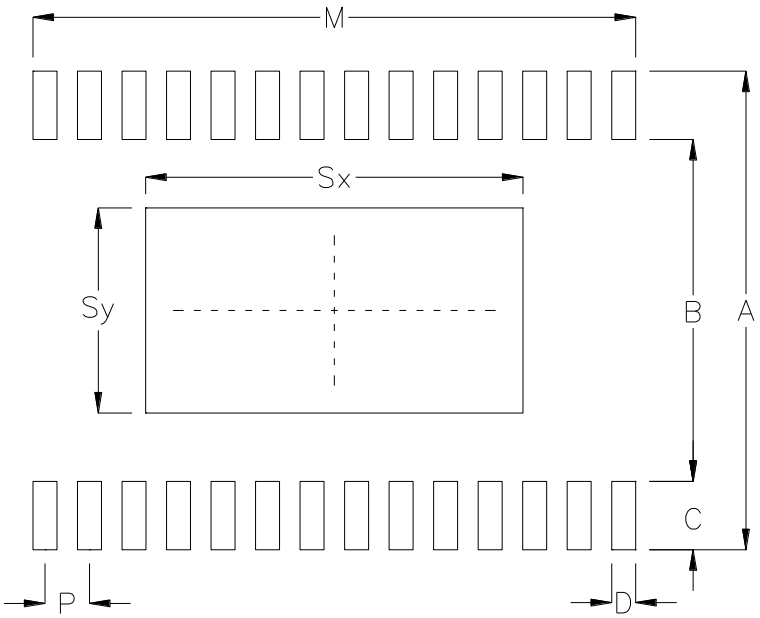


Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		1.000	1.200	0.039	0.047
A1		0.000	0.150	0.000	0.006
A2		0.800	1.050	0.031	0.041
b		0.190	0.300	0.007	0.012
D		9.600	9.800	0.378	0.386
e		0.650		0.026	
E		6.300	6.500	0.248	0.256
E1		4.300	4.500	0.169	0.177
L		0.450	0.750	0.018	0.030
Option1	U	4.410	5.510	0.174	0.217
	V	2.400	3.000	0.094	0.118
Option2	U	5.500	6.170	0.217	0.243
	V	1.600	2.210	0.063	0.087
Option3	U	5.800	6.200	0.228	0.244
	V	2.600	3.000	0.102	0.118
Option4	U	4.410	5.660	0.174	0.223
	V	2.400	3.150	0.094	0.124
Option5	U	3.650	4.050	0.144	0.159
	V	2.625	3.050	0.103	0.120

28-Lead TSSOP (Exposed Pad) Plastic Package

Note 9. The package of the RTQ9124T-QA uses Option 5.

19 Footprint Information

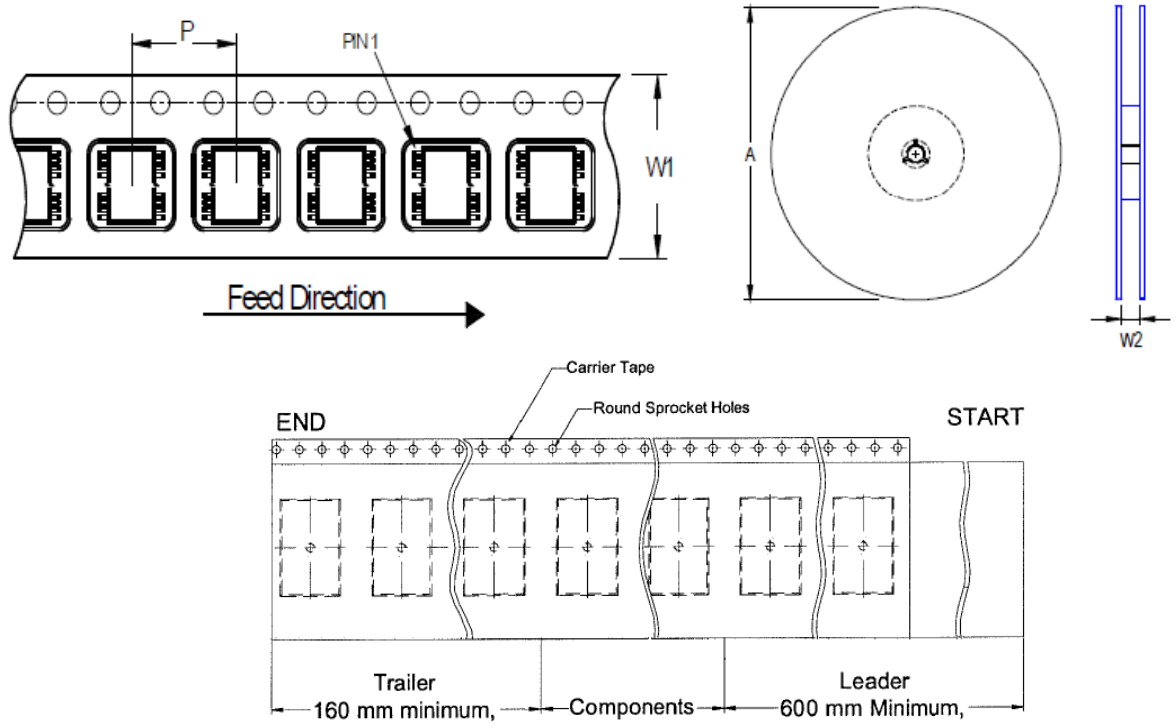


Package		Number of Pins	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
TSSOP-28(PP)	Option1	28	0.65	7.00	5.00	1.00	0.35	5.51	3.00	8.80	±0.10
	Option2							6.17	2.21		
	Option3							6.20	3.00		
	Option4							5.66	3.15		
	Option5							4.05	3.05		

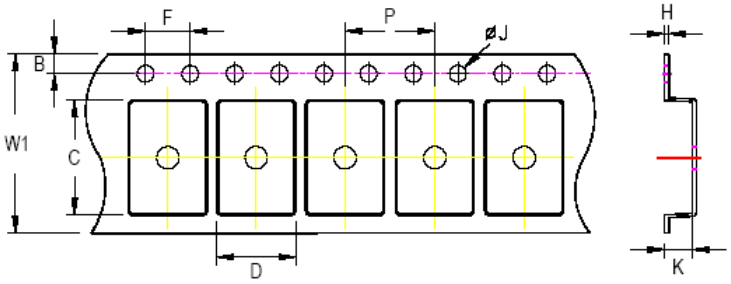
Note 10. The package of the RTQ9124T-QA uses Option 5.

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
TSSOP-28	16	8	330	13	2,500	160	600	16.4/18.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.5mm	1.7mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
TSSOP-28	13”	2,500	Box G	1	2,500	Carton A	6	15,000

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
00	2026/04/08	First Edition