# 3-Phase PWM Controller with Triple Integrated Drivers for VR12.5 CPU Core Power Supply

## General Description

The RT8889C is a three phase CPU power controller with triple integrated drivers for VR12.5 compliant. The RT8889C adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it an easy setting the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT8889C also features a quick response mechanism for optimized AVP performance during load transient. The RT8889C supports mode transition function with various operating states. A Serial VID (SVID) interface is built in the RT8889C to communicate with Intel VR12.5 compliant CPU. The RT8889C supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT8889C varies with VID, load current and input voltage to further enhance the efficiency even in CCM. Besides G-NAVP™, the CCRCOT (Constant Current Ripple Constant On Time) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0.5V to 3.04V with 10mV per step. The RT8889C integrates a high accuracy ADC for platform setting functions, such as no-load offset and over current protection level. It also features complete fault protection functions including Over Voltage (OV), Under Voltage (UV), Negative Voltage (NV), Over Current (OC) and Under Voltage Lockout (UVLO). The RT8889C is available in a WQFN-40L 5x5 small foot print package.

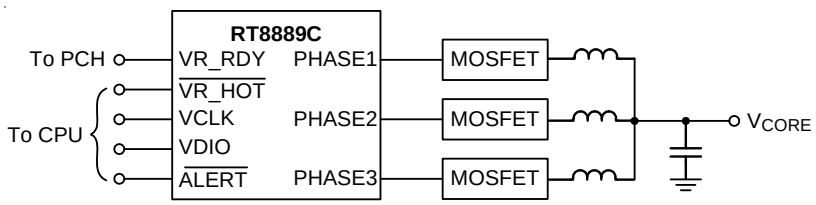
## Features

- **Intel VR12.5 Serial VID Interface Compatible Power Management States**
- **3/2/1 Phase PWM Controller with Triple Integrated Driver**
- **G-NAVP™ Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Accurate Current Balance**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Single Phase**
- **Fast transient Response**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **OVP, UVP, OCP, UVLO**
- **External No-Load Offset Setting**
- **DVID Enhancement**
- **Small 40-Lead WQFN Package**

## Applications

- VR12.5 Intel Core Supply
- Notebook/Desktop Computer/Servers Multi-phase CPU Core Supply
- AVP Step-Down Converters

## Simplified Application Circuit




Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Ordering Information

RT8889C □□

Package Type
QW : WQFN-40L 5x5 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

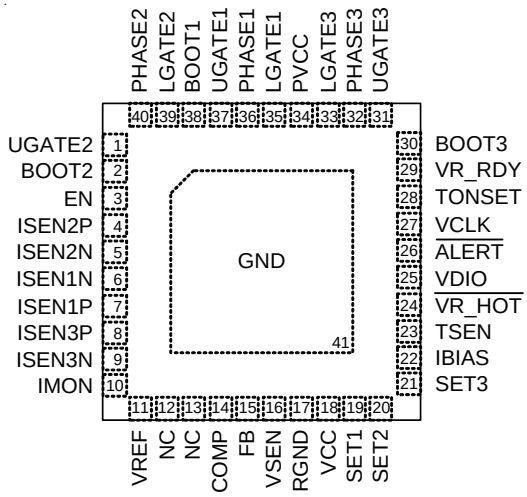
## Marking Information

RT8889CGQW : Product Number

YMDNN : Date Code

## Pin Configuration

(TOP VIEW)




WQFN-40L 5x5

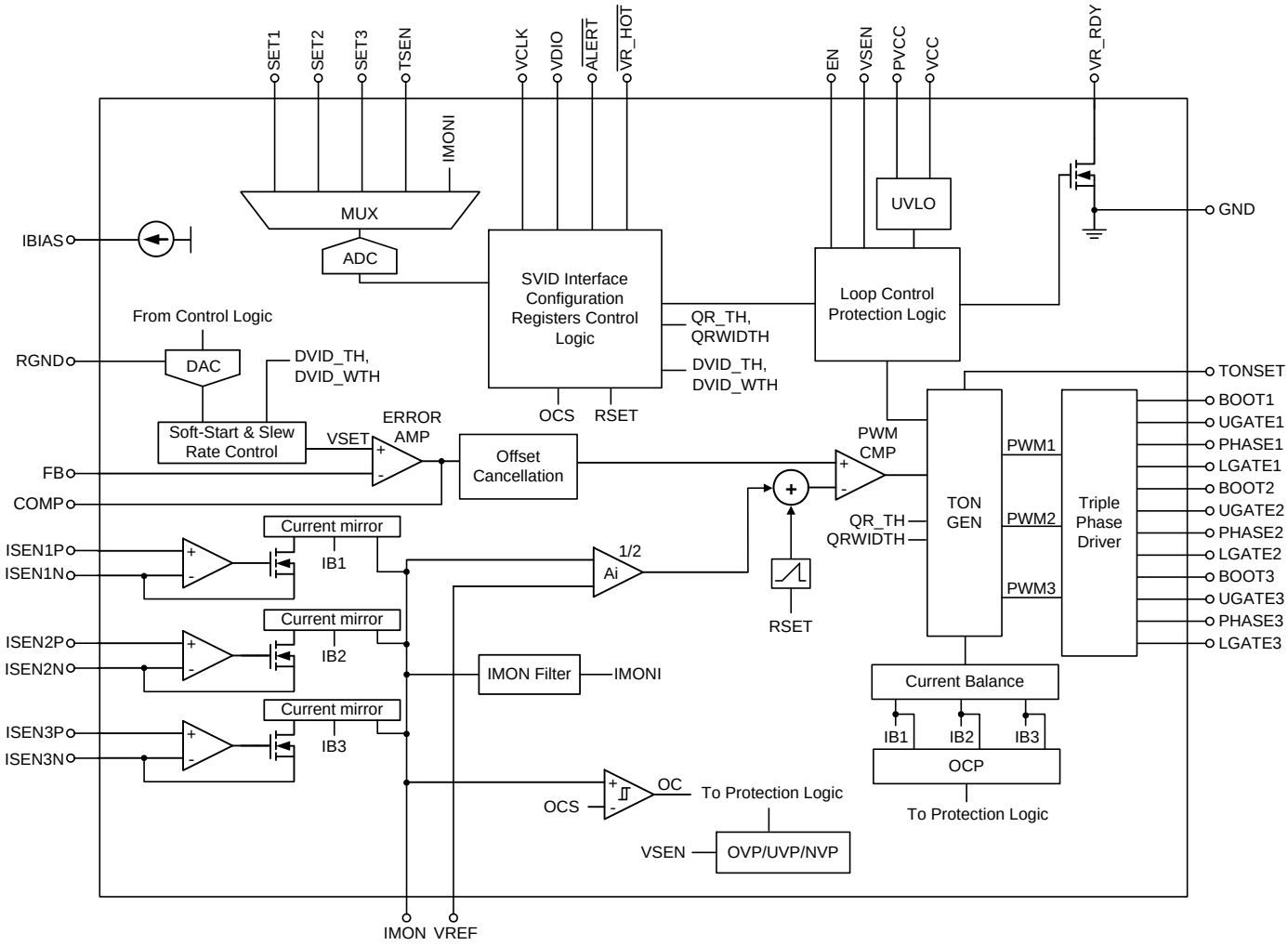
Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 3 | EN | VR enable control input. |
| 6, 5, 9 | ISEN [1:3] N | Negative current sense inputs of channel 1, 2 and 3. |
| 7, 4, 8 | ISEN [1:3] P | Positive current sense inputs of channel 1, 2 and 3. |
| 10 | IMON | CPU CORE current monitor output. This pin outputs a voltage proportional to the output current. Don't connect a bypass capacitor from this pin to GND or VREF pin. |
| 11 | VREF | Fixed 0.6V reference voltage output. This voltage is only used to offset the output voltage of IMON pin. Connect a 0.47μF decoupling capacitor between this pin and GND. |
| 12, 13 | NC | No internal connection. |
| 14 | COMP | Compensation node for VR. This pin is error amplifier output pin. |
| 15 | FB | Negative input of the error amplifier. This pin is for output voltage feedback to controller. |
| 16 | VSEN | Voltage sense input for VR. This pin is connected to the terminal of VR output voltage. |
| 17 | RGND | Return ground for VR. This pin is the negative node of the differential remote voltage sensing. |
| 18 | VCC | Power supply input for controller. Connect this pin to a 5V power supply and place a minimum 2.2μF decoupling capacitor. The decoupling capacitor should be place to PWM controller as close as possible. |
| 19 | SET1 | 1st platform setting. Platform can use this pin to set DVID compensation threshold, RSET, DVID compensation width and OCS. |
| 20 | SET2 | 2nd platform setting. Platform can use this pin to set ICCMAX, QRTH and QRSET. |
| 21 | SET3 | 3rd platform setting. Platform can use this to set output offset voltage. |
| 22 | IBIAS | Internal bias current setting. Connect a 100kΩ resistor from this pin tied to GND to set the internal current. Don't connect a bypass pass capacitor from this pin to GND. |
| 23 | TSEN | Thermal sense input for VR. |
| 24 | $\overline{\text{VR_HOT}}$ | Thermal monitor output. (active low) |
| 25 | VDIO | VR and CPU data transmission interface. |
| 26 | $\overline{\text{ALERT}}$ | SVID alert. (active low) |
| 27 | VCLK | Synchronous clock input from the CPU. |
| 28 | TONSET | On-time setting. An on-time setting resistor is connected from this pin to input voltage. |
| 29 | VR_RDY | VR ready indicator. |
| 34 | PVCC | Driver power. Connect this pin to GND by a minimum ceramic capacitor. |
| 35, 39, 33 | LGATE [1:3] | Low side drive output. This pin drives the Gate of low side MOSFET. |
| 36, 40, 32 | PHASE [1:3] | Switch node of high side driver. Connect the pin to high side MOSFET source together with the low side MOSFET Drain and the inductor. |
| 37, 1, 31 | UGATE [1:3] | High side drive output. Connect the pin to the Gate of high side MOSFET. |
| 38, 2, 30 | BOOT [1:3] | Bootstrap supply for high side gate driver. |
| 41 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Functional Block Diagram




Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Operation

The RT8889C adopts the G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning).

The RT8889C adopts the G-NAVP™ controller, which is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also can have fast transient response. For the RT8889C, when current feedback signal reaches COMP signal to generate an on-time width to achieve PWM modulation.

### TON GEN

Generate the PWM1 to PWM3 sequentially according to the phase control signal from the Loop Control Protection Logic.

### SVID Interface/Configuration Registers/Control Logic

The interface that receives the SVID signal from CPU and sends the relative signals to Loop Control Protection Logic to execute the action by CPU. The registers save the pin setting data from ADC output.

The Control Logic controls the ADC timing and generates the digital code of the VID that is relative to VSEN.

### Loop Control Protection Logic

It controls the power on sequence, the protection behavior, and the operational phase number.

### Current Balance

Each phase current sense signal is sent to the current balance circuit which adjusts the on-time of each phase to optimize current sharing.

### Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

### UVLO

Detect the PVCC and VCC voltage and issue POR signal as they are high enough.

### DAC

Generate an analog signal according to the digital code generated by Control Logic.

### Soft-Start & Slew Rate Control

Control the Dynamic VID slew rate of VSET according to the SetVID fast or SetVID slow.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Table 1. VR12.5 VID Code Table

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | 0.500 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 | 0.510 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 | 0.520 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | 0.530 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 | 0.540 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 | 0.550 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 | 0.560 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 | 0.570 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 | 0.580 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A | 0.590 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B | 0.600 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C | 0.610 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D | 0.620 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E | 0.630 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F | 0.640 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 0.650 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 | 0.660 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 | 0.670 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 | 0.680 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 | 0.690 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15 | 0.700 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 16 | 0.710 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 17 | 0.720 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 18 | 0.730 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 19 | 0.740 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1A | 0.750 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1B | 0.760 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1C | 0.770 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1D | 0.780 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E | 0.790 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1F | 0.800 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | 0.810 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 | 0.820 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22 | 0.830 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23 | 0.840 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24 | 0.850 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25 | 0.860 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26 | 0.870 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 27 | 0.880 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 | 0.890 |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 | 0.900 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A | 0.910 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2B | 0.920 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C | 0.930 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2D | 0.940 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E | 0.950 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 2F | 0.960 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 | 0.970 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31 | 0.980 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 | 0.990 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33 | 1.000 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 | 1.010 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | 1.020 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 | 1.030 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37 | 1.040 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38 | 1.050 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 | 1.060 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A | 1.070 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3B | 1.080 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C | 1.090 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 3D | 1.100 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E | 1.110 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 3F | 1.120 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | 1.130 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 | 1.140 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | 1.150 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43 | 1.160 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | 1.170 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45 | 1.180 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 46 | 1.190 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47 | 1.200 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 48 | 1.210 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 49 | 1.220 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 4A | 1.230 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 4B | 1.240 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4C | 1.250 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 4D | 1.260 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 4E | 1.270 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4F | 1.280 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 | 1.290 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 | 1.300 |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52 | 1.310 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 | 1.320 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54 | 1.330 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55 | 1.340 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56 | 1.350 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 57 | 1.360 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 58 | 1.370 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 59 | 1.380 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A | 1.390 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5B | 1.400 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5C | 1.410 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5D | 1.420 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5E | 1.430 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F | 1.440 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60 | 1.450 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 61 | 1.460 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 62 | 1.470 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 63 | 1.480 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 64 | 1.490 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 65 | 1.500 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 66 | 1.510 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 67 | 1.520 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 68 | 1.530 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 69 | 1.540 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 6A | 1.550 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 6B | 1.560 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6C | 1.570 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 6D | 1.580 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 6E | 1.590 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 6F | 1.600 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70 | 1.610 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71 | 1.620 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 72 | 1.630 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 73 | 1.640 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 74 | 1.650 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 75 | 1.660 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 76 | 1.670 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 77 | 1.680 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 78 | 1.690 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 79 | 1.700 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7A | 1.710 |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 7B | 1.720 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7C | 1.730 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 7D | 1.740 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7E | 1.750 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7F | 1.760 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | 1.770 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 | 1.780 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82 | 1.790 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 | 1.800 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 84 | 1.810 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 85 | 1.820 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 86 | 1.830 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 87 | 1.840 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 88 | 1.850 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 89 | 1.860 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 8A | 1.870 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8B | 1.880 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 8C | 1.890 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 8D | 1.900 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 8E | 1.910 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8F | 1.920 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 90 | 1.930 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 91 | 1.940 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 92 | 1.950 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 93 | 1.960 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 94 | 1.970 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 95 | 1.980 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 96 | 1.990 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 97 | 2.000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98 | 2.010 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 99 | 2.020 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 9A | 2.030 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 9B | 2.040 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 9C | 2.050 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 9D | 2.060 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 9E | 2.070 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 9F | 2.080 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0 | 2.090 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1 | 2.100 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A2 | 2.110 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | A3 | 2.120 |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A4 | 2.130 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5 | 2.140 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | A6 | 2.150 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | A7 | 2.160 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A8 | 2.170 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | A9 | 2.180 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | AA | 2.190 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | AB | 2.200 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | AC | 2.210 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | AD | 2.220 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | AE | 2.230 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | AF | 2.240 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0 | 2.250 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1 | 2.260 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2 | 2.270 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3 | 2.280 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4 | 2.290 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B5 | 2.300 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6 | 2.310 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7 | 2.320 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | B8 | 2.330 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9 | 2.340 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BA | 2.350 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | BB | 2.360 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | BC | 2.370 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | BD | 2.380 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | BE | 2.390 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | BF | 2.400 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0 | 2.410 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | C1 | 2.420 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2 | 2.430 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3 | 2.440 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4 | 2.450 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5 | 2.460 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6 | 2.470 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7 | 2.480 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | C8 | 2.490 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9 | 2.500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CA | 2.510 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | CB | 2.520 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CC | 2.530 |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | CD | 2.540 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | CE | 2.550 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | CF | 2.560 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D0 | 2.570 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D1 | 2.580 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D2 | 2.590 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D3 | 2.600 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | D4 | 2.610 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | D5 | 2.620 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | D6 | 2.630 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D7 | 2.640 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | D8 | 2.650 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | D9 | 2.660 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DA | 2.670 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DB | 2.680 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DC | 2.690 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | DD | 2.700 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | DE | 2.710 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | DF | 2.720 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0 | 2.730 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1 | 2.740 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2 | 2.750 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3 | 2.760 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | E4 | 2.770 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | E5 | 2.780 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | E6 | 2.790 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | E7 | 2.800 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | E8 | 2.810 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | E9 | 2.820 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | EA | 2.830 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | EB | 2.840 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | EC | 2.850 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | ED | 2.860 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | EE | 2.870 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | EF | 2.880 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0 | 2.890 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | F1 | 2.900 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | F2 | 2.910 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | F3 | 2.920 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | F4 | 2.930 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | F5 | 2.940 |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | F6 | 2.950 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | F7 | 2.960 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | F8 | 2.970 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | F9 | 2.980 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | FA | 2.990 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | FB | 3.000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | FC | 3.010 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FD | 3.020 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FE | 3.030 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF | 3.040 |

**Table 2. Standard Serial VID Commands**

| Code | Commands | Master Payload Contents | Slave Payload Contents | Description |
|---|---|---|---|---|
| 00h | not supported | N/A | N/A | N/A |
| 01h | SetVID_Fast | VID code | N/A | 1. Set new target VID code, VR jumps to new VID target with controlled default “fast” slew rate 12.5mV/μs.<br>2. Set VR_Settled when VR reaches target VID voltage. |
| 02h | SetVID_Slow | VID code | N/A | 1. Set new target VID code, VR jumps to new VID target with controlled default “slow” slew rate 3.125mV/μs.<br>2. Set VR_Settled when VR reaches target VID voltage. |
| 03h | SetVID_Decay | VID code | N/A | 1. Set new target VID code, VR jumps to new VID target, but doest not control the slew rate. The output voltage decays at a rate proportional to the load current.<br>2. Low side MOSFET is not allowed to sync current.<br>3. ACK 11b when target higher than current VOUT voltage.<br>4. ACK 10b when target lower than current VOUT voltage. |
| 04h | SetPS | Byte indicating power states | N/A | 1. Set power state.<br>2. ACK 11b when not support.<br>3. ACK 10b even slave not change configuration.<br>4. ACK 11b for still running SetVID command.<br>5. VR remains in lower state when receiving SetVID (decay). |
| 05h | SetRegADR | Pointer of registers in data table | N/A | 1. Set the pointer of the data register.<br>2. ACK 11b for address outside of support.<br>3. NAK 01b for SetADR (all call). |
| 06h | SetReg DAT | New data register content | N/A | 1. Write the contents to the data register.<br>2. NAK 01b for SetReg (all call). |
| 07h | GetReg | | Specified Register Contents | 1. Slave returns the contents of the specified register as the payload.<br>2. ACK 11b for non support address.<br>3. NAK 01b for GetReg (all call). |
| 08h to 1Fh | not supported | N/A | N/A | N/A |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

**Table3. SVID Data and Configuration Register**

| Index | Register Name | Description | Access | Default |
|---|---|---|---|---|
| 00h | Vendor ID | Vendor ID | RO, Vendor | 1Eh |
| 01h | Product ID | Product ID | RO, Vendor | 89 |
| 02h | Product Revision | Product Revision | RO, Vendor | 00h |
| 05h | Protocol ID | SVID Protocol ID | RO, Vendor | 02h |
| 06h | Capability | Bit mapped register, identifies the SVID VR Capabilities and which of the optional telemetry register is supported. | RO, Vendor | 81h |
| 10h | Status_1 | Data register containing the status of VR. | R-M, W-PWM | 00h |
| 11h | Status-2 | Data register containing the status of transmission. | R-M, W-PWM | 00h |
| 12h | Temperature Zone | Data register showing temperature zone that has been entered. | R-M, W-PWM | 00h |
| 15h | IOUT | The default value is 00h. When power state is PS0/1/2, the IOUT value depends on IMON voltage. When power state is PS3, the IOUT value is fixed to 04h. | R-M, W-PWM | 00h |
| 1Ch | Status_2_lastread | The register contains a copy of the status_2. | R-M, W-PWM | 00h |
| 21h | ICC Max | Data register containing the ICC max the platform supports. Binary format in A IE 64h = 100A. | RO, Platform | 7Dh |
| 22h | Temp Max | Data register containing the temperature max the platform supports.<br>Binary format in °C IE 64h = 100°C. | RO, Platform | 64h |
| 24h | SR-fast | Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/µs IE 0Ah = 10 mV/µs. | RO | 0A |
| 25h | SR-slow | Data register containing the capability of slow slew rate. Binary format in mV/µs IE 03h = 3mV/µs. | RO | 02h |
| 30h | VOUT Max | The register is programmed by master and sets the maximum VID. | RW, Master | B5h |
| 31h | VID Setting | Data register containing currently programmed VID. | RW, Master | 00h |
| 32h | Power State | Register containing the current programmed power state. | RW, Master | 00h |
| 33h | Offset | Set offset in VID steps. | RW, Master | 00h |
| 34h | Multi VR Configuration | Bit mapped data register which configures multiple VRs behavior on the same bus. | RW, Master | 00h |
| 35h | Pointer | Scratch pad register for temporary storage of the SetRegADR pointer register. | RW, Master | 30h |

Notes :

RO = Read Only

RW = Read/Write

R-M = Read by Master

W-PWM = Write by PWM Only

Vendor = Hard Coded by VR Vendor

Platform = Programmed by the Master

PWM = Programmed by the VR Control IC

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6V
- PVCC to GND ---------- –0.3V to 15V
- RGND to GND ---------- –0.3V to 0.3V
- TONSET to GND ---------- –0.3V to 6.5V
- BOOTx to PHASEx ---------- –0.3V to 15V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - < 20ns ---------- –10V to 35V
- LGATEx to GND
  - DC ---------- –0.3V to (PVCC + 0.3V)
  - < 20ns ---------- –2V to (PVCC + 0.3V)
- UGATEx to GND
  - DC ---------- ($V_{PHASE}$ – 0.3V) to ($V_{BOOT}$ + 0.3V)
  - < 20ns ---------- ($V_{PHASE}$ – 2V) to ($V_{BOOT}$ + 0.3V)
- Other Pins ---------- –0.3V to ($V_{CC}$ + 0.3V)
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  - WQFN 40L 5x5 ---------- 3.64W
- Package Thermal Resistance (Note 2)
  - WQFN 40L 5x5, $\theta_{JA}$ ---------- 27.5°C/W
  - WQFN 40L 5x5, $\theta_{JC}$ ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Voltage, PVCC ---------- 4.5V to 13.5V
- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{CC}$ = 5V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Input** | | | | | | |
| Supply Voltage | $V_{CC}$ | | 4.5 | 5 | 5.5 | V |
| Supply Current | $I_{VCC}$ | $V_{EN}$ = H, no switching | -- | 4.1 | -- | mA |
| Supply Current at PS3 | $I_{VCC_PS3}$ | $V_{EN}$ = H, no switching | -- | 2.7 | -- | mA |
| Shutdown Current | $I_{SHDN}$ | $V_{EN}$ = 0V | -- | -- | 5 | μA |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage | PVCC | | 4.5 | -- | 13.2 | V |
| Power Supply Current | $I_{PVCC}$ | | -- | 250 | -- | μA |
| **Reference and DAC** | | | | | | |
| DAC Accuracy | $V_{FB}$ | $V_{DAC}$ = 1.5V – 2.3V | –0.5 | 0 | 0.5 | % of VID |
| | | $V_{DAC}$ = 1V – 1.49V | –8 | 0 | 8 | mV |
| | | $V_{DAC}$ = 0.5V – 0.99V | –10 | 0 | 10 | |
| **PVCC Power On Reset (POR)** | | | | | | |
| POR Threshold | $V_{POR_r}$ | PVCC rising | -- | 4 | 4.4 | V |
| | $V_{POR_f}$ | PVCC falling | 3 | 3.5 | -- | |
| POR Hysteresis | $V_{POR_HYS}$ | | -- | 0.5 | -- | V |
| **Slew Rate** | | | | | | |
| Dynamic VID Slew Rate | $SR_{_VID}$ | Set VID slow | 2.5 | 3.125 | 3.75 | mV/μs |
| | | Set VID fast | 10 | 12.5 | 15 | |
| **EA Amplifier** | | | | | | |
| DC Gain | $A_{DC}$ | $R_L$ = 47kΩ | 70 | -- | -- | dB |
| Gain-Bandwidth Product | $G_{BW}$ | $C_{LOAD}$ = 5pF | 4 | 5 | -- | MHz |
| Slew Rate | SR | $C_{LOAD}$ = 10pF (Gain = –4, $R_F$ = 47kΩ, $V_{OUT}$ = 0.5V to –3V) | 5 | -- | -- | V/μs |
| Output Voltage Range | $V_{COMP}$ | $R_L$ = 47kΩ | 0.5 | -- | 3.6 | V |
| Maximum Source/Sink Current | $I_{OUTEA}$ | $V_{COMP}$ = 2V | -- | 5 | -- | mA |
| **Load-Line Current Gain Amplifier** | | | | | | |
| Input Offset Voltage | $V_{ILOFS}$ | $V_{IMON}$ = 1V | –5 | -- | 5 | mV |
| Current Gain | $A_{ILGAIN}$ | $V_{IMON} – V_{VREF}$ = 1V<br>$V_{FB} = V_{COMP}$ = 1.7V | -- | 1/2 | -- | A/A |
| **Current Sensing Amplifier** | | | | | | |
| Input Offset Voltage | $V_{OSCS}$ | | –0.8 | -- | 0.8 | mV |
| Impedance at Positive Input | $R_{ISENxP}$ | | 1 | -- | -- | MΩ |
| Current Mirror Gain | $A_{MIRROR}$ | $I_{IMON}$ / $I_{SENxN}$ | 0.97 | 1 | 1.03 | A/A |
| **TON Setting** | | | | | | |
| TON Pin Voltage | $V_{TON}$ | $I_{RTON}$ = 80μA, $V_{DAC}$ = 1.7V | 1.6 | 1.7 | 1.8 | V |
| On-Time Setting | $T_{ON}$ | $I_{RTON}$ = 80μA, $V_{DAC}$ = 1.7V | 450 | 500 | 550 | ns |
| Input Current Range | $I_{RTON}$ | $V_{DAC}$ = 1.7V | 25 | -- | 280 | μA |
| Minimum Off time | $T_{OFF}$ | $V_{DAC}$ = 1.7V | -- | 400 | -- | ns |
| **IBIAS** | | | | | | |
| IBIAS Pin Voltage | $V_{IBIAS}$ | $R_{IBIAS}$ = 100kΩ | 1.85 | 2 | -- | V |
| **OFS Setting** | | | | | | |
| Impedance | $R_{OFS}$ | | 1 | -- | -- | MΩ |
| Set OFS Voltage | $V_{OFS}$ | Enable OFS function and offset 600mV | 1.95 | 2.4 | 2.44 | V |
| | | Enable OFS function and offset 300mV | 1.76 | 1.8 | 1.84 | |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Set OFS Voltage | | $V_{OFS}$ | Enable OFS function and offset 0V | 1.16 | 1.2 | 1.24 | V |
| | | | Enable OFS function and offset –50mV | 1.06 | 1.1 | 1.14 | |
| | | | Enable OFS function and offset –250mV | 0.66 | 0.7 | 0.74 | |
| | | | Disable | -- | -- | 0.55 | |
| **Protections** | | | | | | | |
| Under Voltage Lockout Threshold | | $V_{UVLO}$ | | 4.1 | 4.3 | 4.45 | V |
| | | $\Delta V_{UVLO}$ | Falling edge hysteresis | -- | 200 | -- | mV |
| Over Voltage Protection Threshold | | $V_{OV}$ | VID higher than 1.5V | VID + 300 | VID + 350 | VID + 400 | mV |
| | | | VID lower than 1.5V | 1800 | 1850 | 1900 | |
| Under Voltage Protection Threshold | | $V_{UV}$ | with respect to VID voltage | –400 | –350 | –300 | mV |
| Negative Voltage Protection Threshold | | $V_{NV}$ | | –100 | –70 | -- | mV |
| **EN and VR_READY** | | | | | | | |
| EN Input Voltage | Logic-High | $V_{EN_H}$ | | 0.7 | -- | -- | V |
| | Logic-Low | $V_{EN_L}$ | | -- | -- | 0.3 | |
| Leakage Current of EN | | | | –1 | -- | 1 | μA |
| VR_READY Delay | | $T_{VR_RD}$ | $V_{SEN}$ = $V_{BOOT}$ to VR_READY High | 3 | 4.5 | 6 | μs |
| VR_READY Pull Low Voltage | | $V_{PGOOD}$ | $I_{VR_READY}$ = 10mA | -- | -- | 0.13 | V |
| **Serial VID and $\overline{\text{VR_HOT}}$** | | | | | | | |
| VCLK, VDIO Input Voltage | Logic-High | $V_{IH}$ | With Respect to INTEL Spec. with 50mV hysteresis | 0.65 | -- | -- | V |
| | Logic-Low | $V_{IL}$ | | -- | -- | 0.45 | |
| Leakage Current of VCLK, VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR_HOT}}$ | | $I_{LEAK_IN}$ | | –1 | -- | 1 | μA |
| VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR_HOT}}$ Pull Low Voltage | | | $I_{VDIO}$ = 10mA | -- | -- | 0.13 | V |
| | | | $I_{\overline{ALERT}}$ = 10mA | | | | |
| | | | $I_{\overline{VR_HOT}}$ = 10mAs | | | | |
| **$V_{REF}$ and $V_{BOOT}$** | | | | | | | |
| $V_{REF}$ Voltage | | $V_{REF}$ | | 0.55 | 0.6 | 0.65 | V |
| $V_{BOOT}$ Voltage | | $V_{BOOT}$ | $V_{BOOT}$ Voltage set to 1.7V | 1.692 | 1.7 | 1.708 | V |
| **ADC** | | | | | | | |
| Digital IMON Set | | $V_{IMON}$ | $V_{IMON}$ – $V_{IMON_INI}$ = 1.6V | 252 | 255 | 258 | Decimal |
| | | | $V_{IMON}$ – $V_{IMON_INI}$ = 0.8V | 125 | 128 | 131 | |
| | | | $V_{IMON}$ – $V_{IMON_INI}$ = 0V | 0 | 0 | 3 | |
| Update Period of IMON | | $T_{IMON}$ | | 320 | 400 | 480 | μs |
| TSEN Threshold for Tmp_Zone [7] transition | | $V_{TSEN}$ | 100°C | -- | 1.887 | -- | V |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TSEN Threshold for Tmp_Zone [6] transition | $V_{TSEN}$ | 97°C | -- | 1.837 | -- | V |
| TSEN Threshold for Tmp_Zone [5] transition | $V_{TSEN}$ | 94°C | -- | 1.784 | -- | V |
| TSEN Threshold for Tmp_Zone [4] transition | $V_{TSEN}$ | 91°C | -- | 1.729 | -- | V |
| TSEN Threshold for Tmp_Zone [3] transition | $V_{TSEN}$ | 88°C | -- | 1.672 | -- | V |
| TSEN Threshold for Tmp_Zone [2] transition | $V_{TSEN}$ | 85°C | -- | 1.612 | -- | V |
| TSEN Threshold for Tmp_Zone [1] transition | $V_{TSEN}$ | 82°C | -- | 1.551 | -- | V |
| TSEN Threshold for Tmp_Zone [0] transition | $V_{TSEN}$ | 75°C | -- | 1.402 | -- | V |
| Update Period of TSEN | $t_{TSEN}$ | | 40 | 50 | 60 | μs |
| Digital Code of ICCMAX | $C_{ICCMAX1}$ | $V_{ICCMAX}$ = 0.403V | 58 | 64 | 70 | Decimal |
| | $C_{ICCMAX2}$ | $V_{ICCMAX}$ = 0.806V | 122 | 128 | 134 | |
| | $C_{ICCMAX3}$ | $V_{ICCMAX}$ = 1.6V | 248 | 256 | 260 | |
| **Timing** | | | | | | |
| UGATEx Rising Time | $t_{UGATEr}$ | 3nF load | -- | 25 | -- | ns |
| UGATEx Falling Time | $t_{UGATEf}$ | 3nF load | -- | 12 | -- | ns |
| LGATEx Rising Time | $t_{LGATEr}$ | 3nF load | -- | 24 | -- | ns |
| LGATEx Falling Time | $t_{LGATEf}$ | 3nF load | -- | 10 | -- | ns |
| Propagation Delay | $t_{UGATEpgh}$ | $V_{BOOTx} - V_{PHASEx}$ = 12V<br>See Timing Diagram | -- | 60 | -- | ns |
| | $t_{UGATEpdl}$ | | -- | 22 | -- | |
| | $t_{LGATEpdh}$ | See Timing Diagram | -- | 30 | -- | ns |
| | $t_{LGATEpdl}$ | | -- | 8 | -- | |
| **Output** | | | | | | |
| UGATEx Drive Source | $R_{UGATEsr}$ | $V_{BOOT} - V_{PHASE}$ = 12V,<br>$I_{Source}$ = 100mA | -- | 1.7 | -- | Ω |
| UGATEx Drive Sink | $R_{UGATEsk}$ | $V_{BOOT} - V_{PHASE}$ = 12V,<br>$I_{Sink}$ = 100mA | -- | 1.4 | -- | Ω |
| LGATEx Drive Source | $R_{LGATEsr}$ | $I_{Source}$ = 100mA | -- | 1.6 | -- | Ω |
| LGATEx Drive Sink | $R_{LGATEsk}$ | $I_{Sink}$ = 100mA | -- | 1.1 | -- | Ω |

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

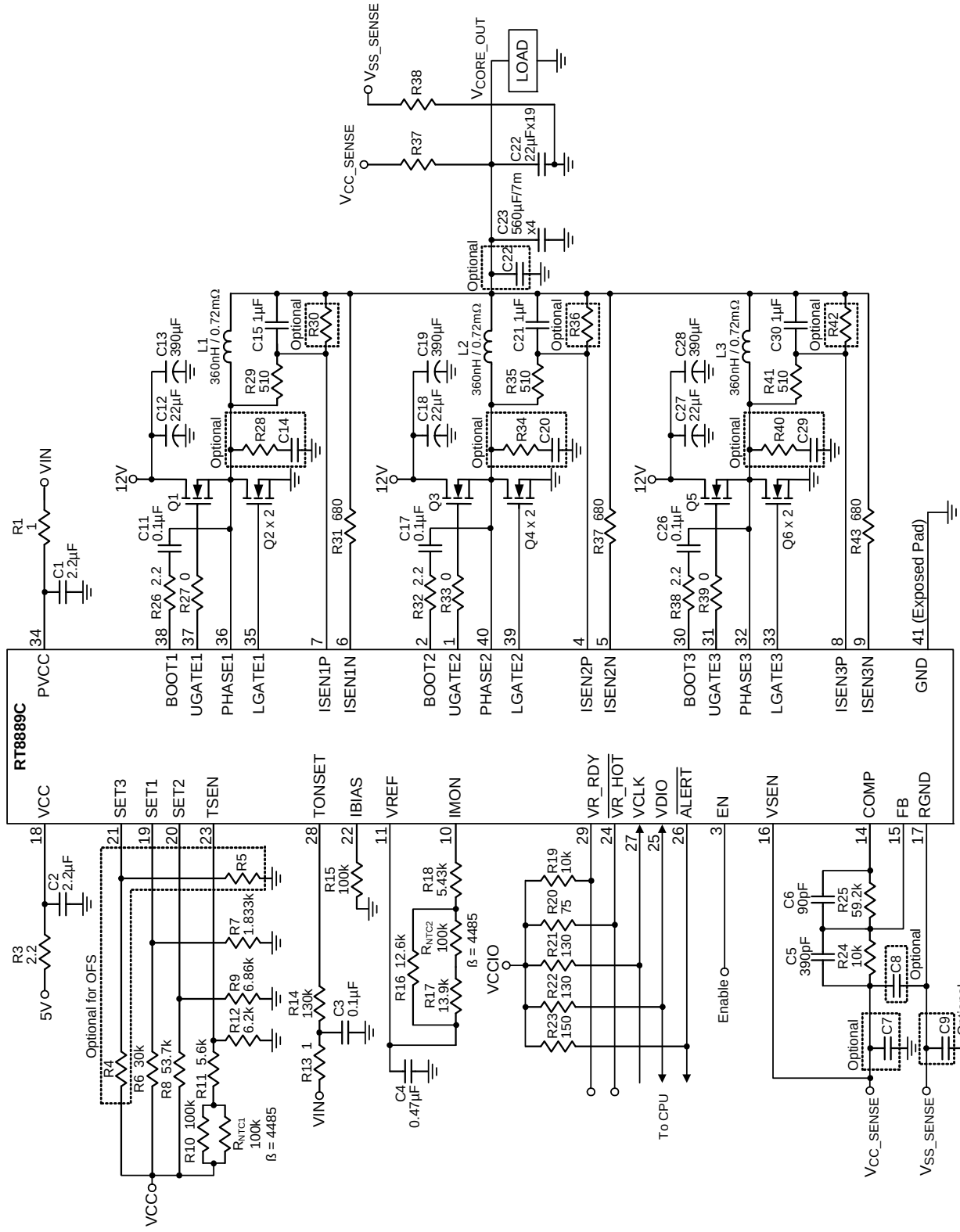
**Note 2.** $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

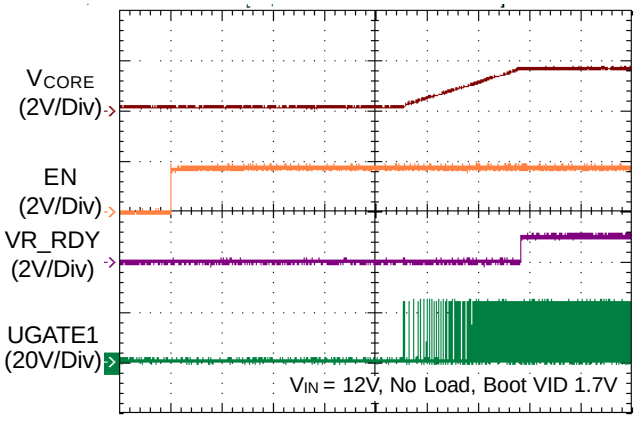
## Typical Application Circuit



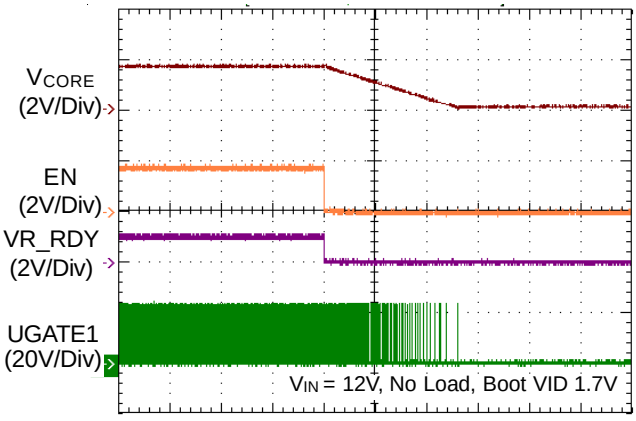

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Typical Operating Characteristics

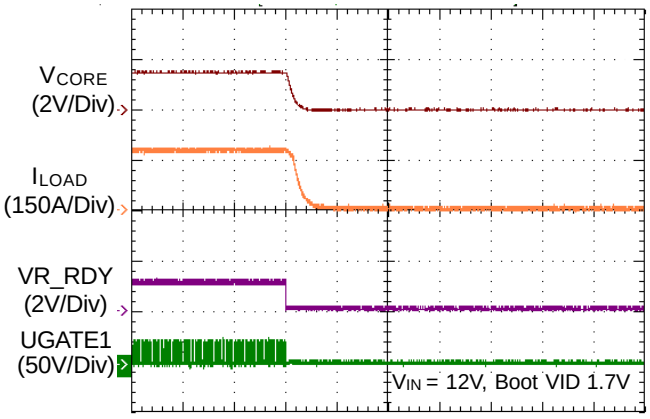
### CORE VR Power On from EN



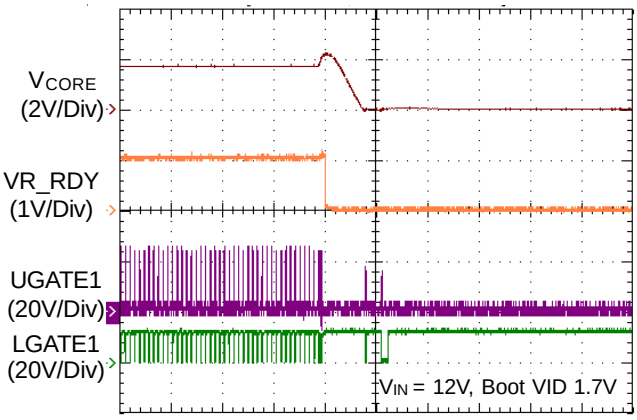

### CORE VR Power Off from EN



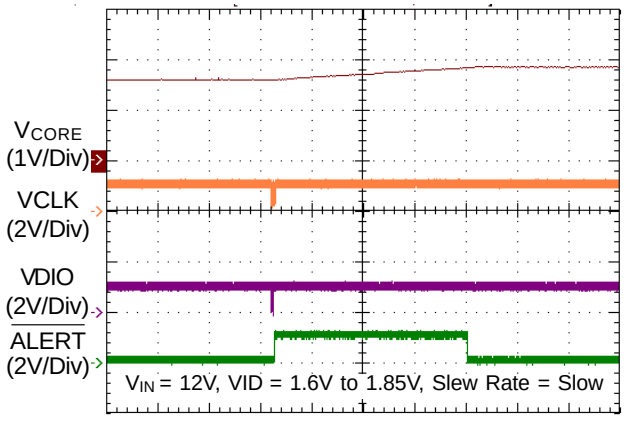

### CORE VR OCP



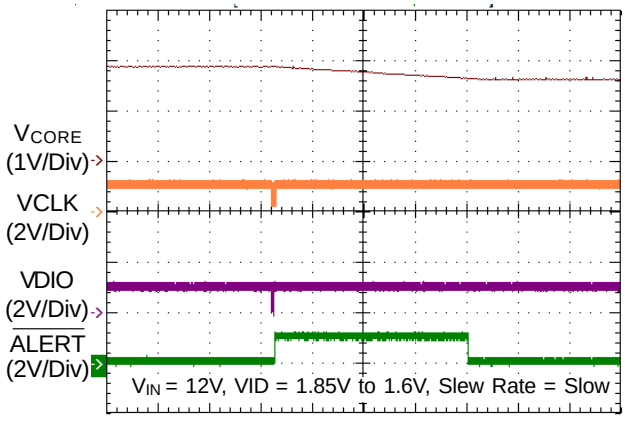

### CORE VR OVP




### CORE VR Dynamic VID Up

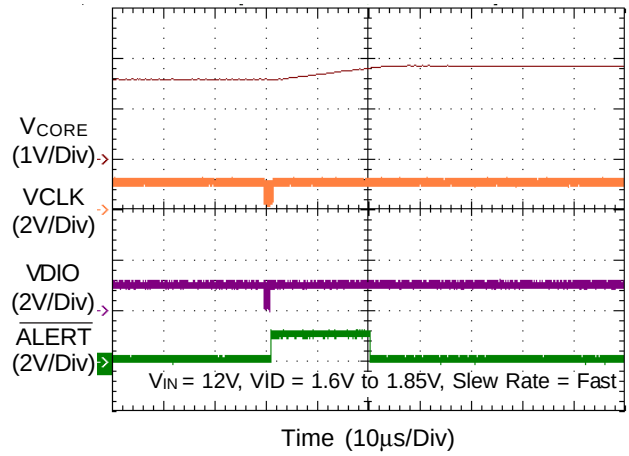



### CORE VR Dynamic VID Down

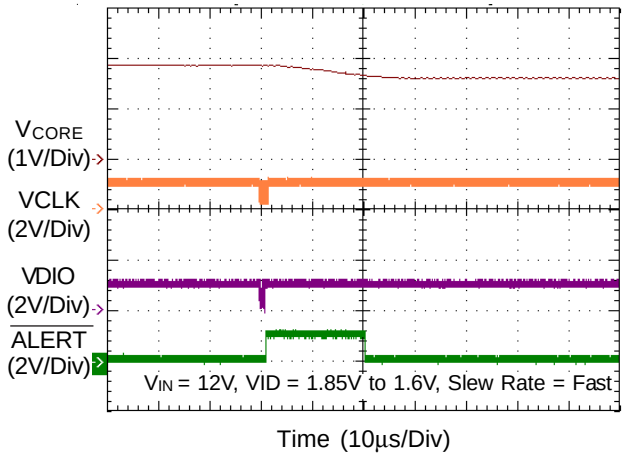



Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

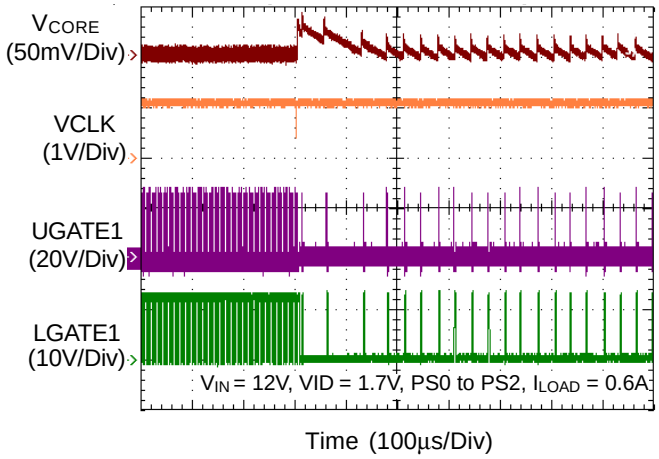
### CORE VR Dynamic VID Up



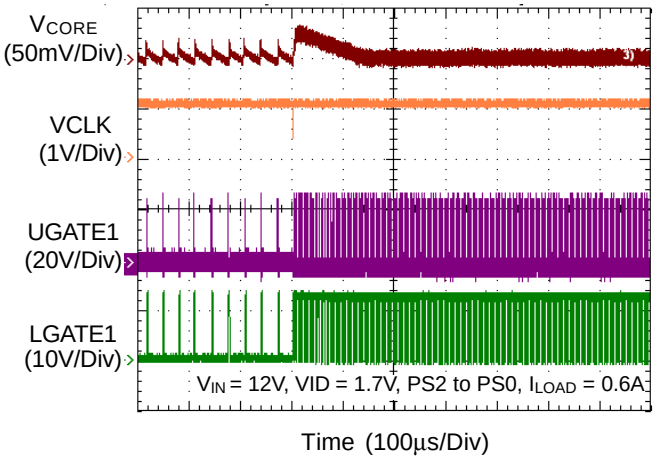

### CORE VR Dynamic VID Down



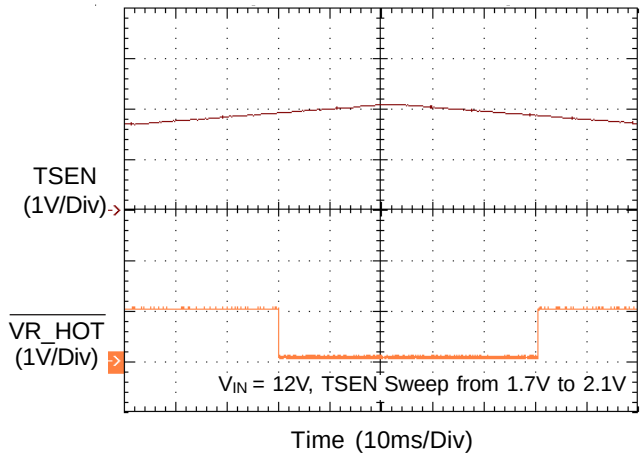

### CORE VR Mode Transient



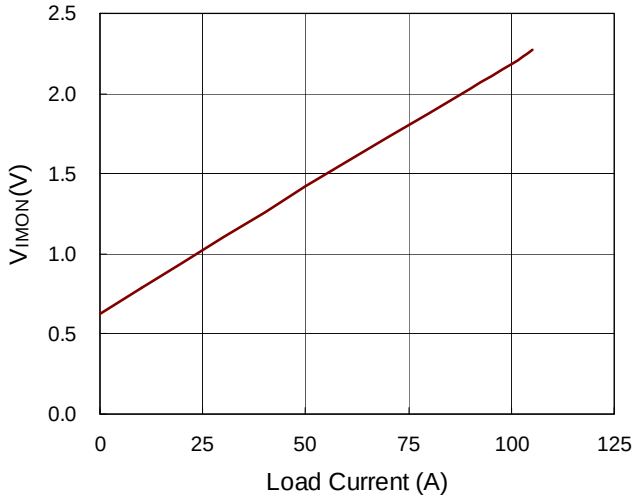

### CORE VR Mode Transient




### CORE VR Thermal Monitoring




### VIMON vs. Load Current




Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Applications information

The RT8889C is a 3/2/1 multiphase synchronous Buck controller designed to meet Intel VR12.5 compatible CPU specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save a total number of pins for easily using and increasing PCB space utilization. The RT8889C is suitable for the applications of notebook, desktop computer and server.

### G-NAVP™ Control Mode

The RT8889C adopts the G-NAVP™ control topology, which is a current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. Figure 1 shows the basic G-NAVP™ behavior waveforms in Continuous Conduct Mode (CCM).

When the current feedback signal reaches Comp signal, an on-time pulse will be generated to achieve PWM modulation.

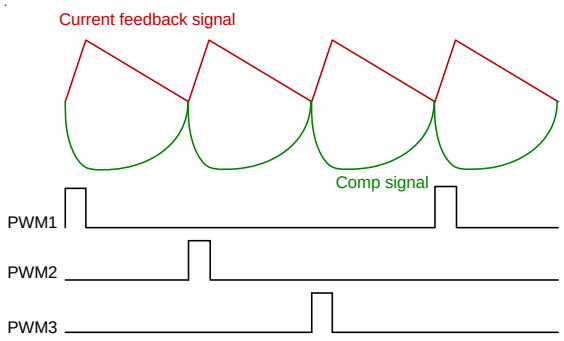



Figure 1 (a). G-NAVP™ Behavior Waveforms in CCM in Steady State

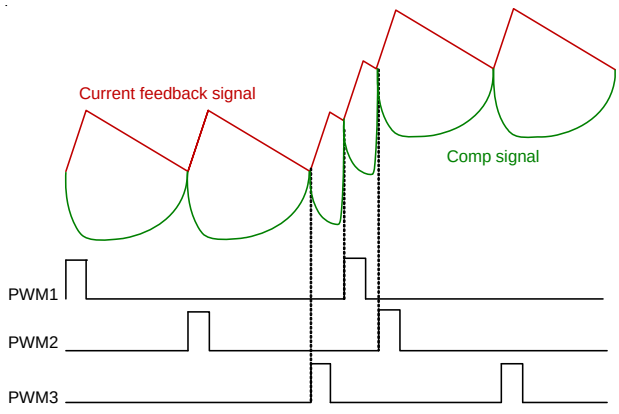



Figure 1 (b). G-NAVP™ Behavior Waveforms in CCM in Load Transient

### Diode Emulation Mode (DEM)

As well-known, the dominate power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduct mode, DCM) to reduce switching related loss. Since switching frequency is dependent on loading in the asynchronous mode, the RT8889C can operate in Diode Emulation Mode (DEM) to improve light load efficiency. In DEM operation, the behavior of the low side MOSFET(s) needs to work like a diode, that is, the low side MOSFET(s) will be turned on when the phase voltage is a negative value, i.e. the inductor current follows from source to drain in the low side MOSFET(s). The low side MOSFET(s) will be turned off when phase voltage is a positive value, i.e. reversed current is not allowed. Figure 2 shows the control behavior in DEM. Figure 3 shows the G-NAVP™ operation in DEM to illustrate the control behaviors. When the load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switch loss will be reduced to improve the efficiency in light load condition.

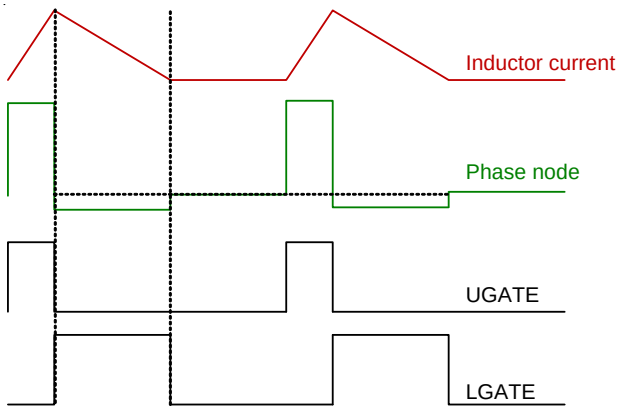
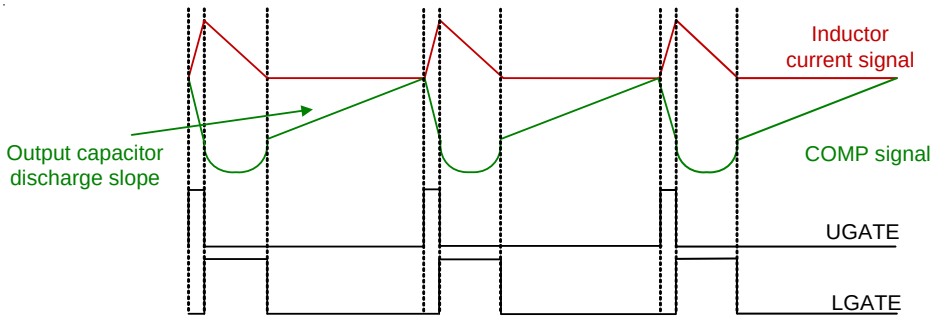


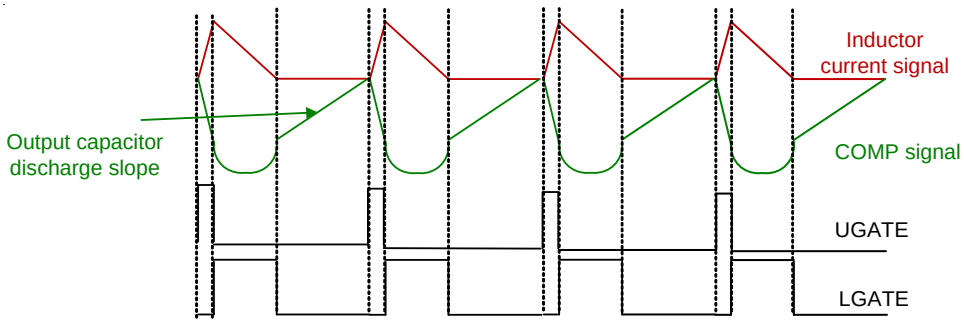

Figure 2. Diode Emulation Mode (DEM) in Steady State

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.




(a). Lighter Load Condition

Capacitor discharge slope is lower than Figure 3 (b).




(b). Load Increased Condition

Capacitor discharge slope is higher than Figure 3 (a).

Figure 3. G-NAVP™ Operation in DEM.

### VR Power State

The RT8889C supports power state change by CPU command through SVID protocol. As the RT8889C receives a set PSx command, the VR changes the power state to meet the operation current. In the RT8889C, PS0 means the full phase CCM operation; PS1 means the one phase CCM operation; PS2 means the one phase DEM operation; PS3 means the one phase DEM operation with low quiescent current, as shown in Table 4.

**Table 4 : Set PSx Command and Operation Mode**

| Set PSx Command | Operation Mode | Operation Phase Number |
|---|---|---|
| PS0 | CCM | 3 |
| PS1 | CCM | 1 |
| PS2 | DEM | 1 |
| PS3 | DEM | 1 |

### Phase Interleaving Function

The RT8889C is a multiphase controller, which has a phase interleaving function, 120 degree phase shift for 3-phase operation and 180 degree phase shift for 2-phase operation which can reduce output voltage ripple and EMI problem.

### Switching Frequency (TON) Setting

The RT8889C is one kind of constant on-time control. The patented CCRCOT (Constant Current Ripple COT) technology can generate an adaptive on-time with input voltage and VID code to obtain a constant current ripple. So that the output voltage ripple can be controlled nearly like a constant as different input and output voltage change. Connect a resistor $R_{TON}$ between input terminal and TONSET pin to set the on-time width.

$$T_{ON} = \frac{R_{TON} \times C \times 2.2}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 2.2V)$$

$$T_{ON} = \frac{R_{TON} \times C \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (V_{DAC} \geq 2.2V)$$

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Where C = 18.2pF, $V_{REF}$ = 2.2V. By using the relationship between $T_{ON}$ and $f_{SW}$, the switching frequency $f_{SW}$ is :

$$f_{SW(MAX)} = \left(\frac{1}{T_{ON(MAX)}}\right) \times \left(\frac{V_{DAC(MAX)}}{V_{IN(MAX)}}\right)$$

$f_{SW(MAX)}$ is the maximum switching frequency.

$V_{DAC(MAX)}$ is the maximum $V_{DAC}$ of application.

$V_{IN(MAX)}$ is the maximum application input voltage.

$T_{ON(MAX)}$ is derived from $T_{ON}$ equation with maximum parameters ($V_{IN(MAX)}$, $V_{DAC(MAX)}$).

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence the loading current increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

### Per Phase Current Sense

In the RT8889C, the current signal is used for load-line setting and OC (Over Current) protections. The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in the Figure 4. When inductance and DCR time constant is equal to $R_XC_X$ filter network time constant, a voltage $I_{LX}$ x DCR will drop on $C_X$ to generate inductor current signal. According to the Figure 4, the ISENxN is as follows :

$$ISENxN = \frac{I_{LX} \times DCR}{R_{CSx}}$$

Where LX / DCR = $R_XC_X$ is held. The method can get high efficiency performance, but DCR value will be drifted by temperature, a NTC resistor should add in the resistor network in the IMON pin to achieve DCR thermal compensation.

In the RT8889C design, the resistance of the $R_{CSx}$ is restricted to 680Ω; moreover, the accuracy of $R_{CS}$ is recommended to be 1% or higher.

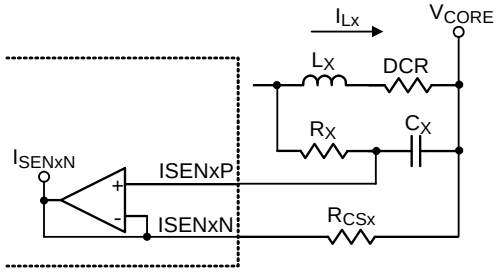



Figure 4. Lossless Current Sense Method

### Total Current Sense

Total current sense method is a patented topology, unlike conventional current sense method requiring a NTC resistor in per phase current loop for thermal compensation. The RT8889C adopts the total current sense method requiring only one NTC resistor for thermal compensation, and NTC resistor cost can be saved by using this method. Figure 5 shows the total current sense method which connects the resistor network between the IMON and VREF pins to set a part of current loop gain for load-line (droop) setting and set accurate over current protection.

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times (I_{L1} + I_{L2} + I_{L3})$$

$R_{EQ}$ includes a NTC resistor to compensate DCR thermal drifting for high accuracy load-line (droop).

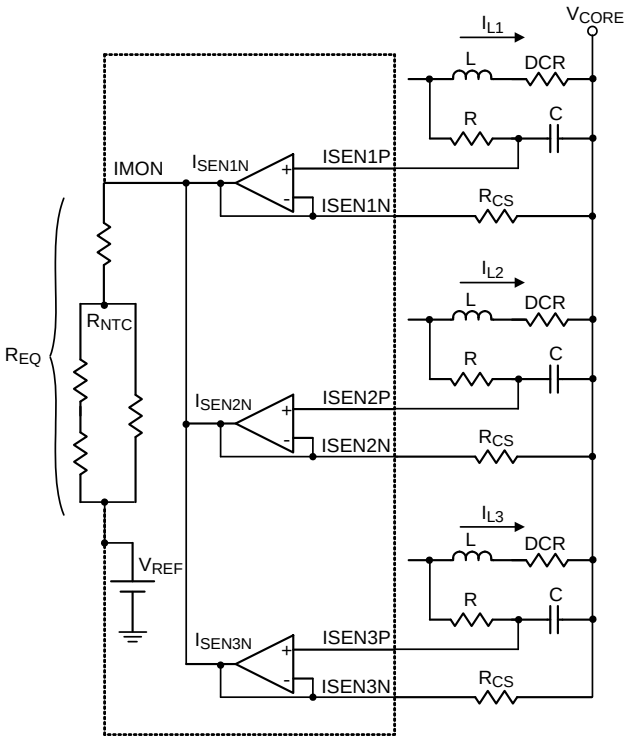



Figure 5. Total Current Sense Method

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

### Load-Line (Droop) Setting

The G-NAVP™ topology can set load-line (droop) via the current loop and the voltage loop, the load-line is a slope between load current $I_{CC}$ and output voltage $V_{CORE}$ as shown in Figure 6. Figure 7 shows the voltage control and current loop. By using both loops, the load-line (droop) can easily be set. The load-line set equation is :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{1}{2} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} \ (m\Omega)$$

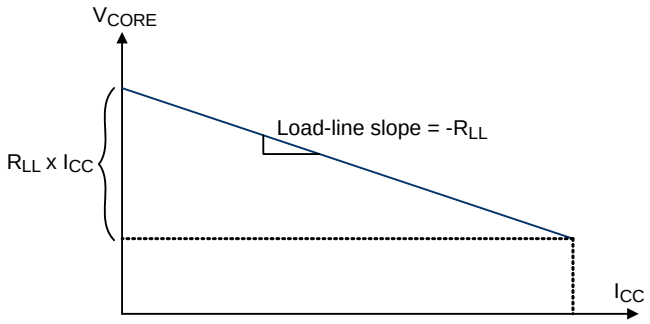



Figure 6. Load-Line (Droop)

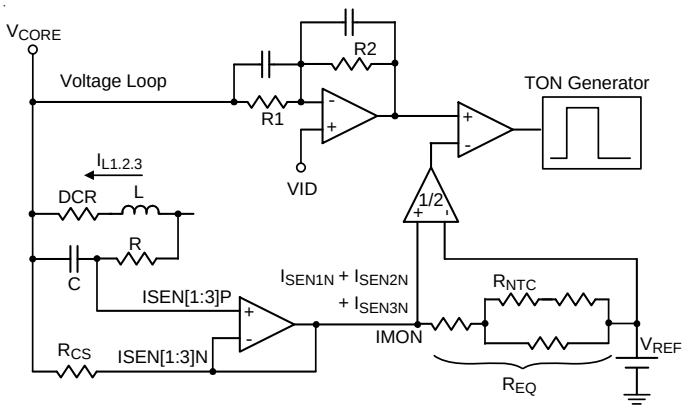



Figure 7. Voltage Loop and Current Loop

### Compensator Design

The compensator of the RT8889C doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in G-NAVP™ topology to achieve constant output impedance design for Intel VR12.5 ACLL specification. The one pole one zero compensator is showed as Figure 8, the transfer function of compensator should be designed as the following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range :

$$G_{CON}(s) \approx \frac{A_I}{R_{LL}} \times \frac{1 + \frac{s}{\pi \times fsw}}{1 + \frac{s}{\omega_{ESR}}}$$

Where $A_I$ is current loop gain, $R_{LL}$ is load-line, $f_{SW}$ is switching frequency and $\omega_{ESR}$ is a pole that should be located at 1 / ($C_{OUT}$ x ESR). Then the C1 and C2 should be designed as follows :

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}}$$

$$C2 = \frac{C_{OUT} \times ESR}{R2}$$

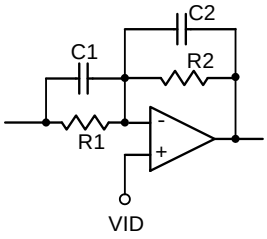



Figure 8. Type I Compensator

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

### Multi-Function Pin Setting Mechanism

For reducing total pin number of package, the SET[1:2] pins adopt the multi-function pin setting mechanism in the RT8889C. Figure 9 illustrates this operating mechanism. First, external voltage divider is to set the Function 1 and then internal current source 80μA is to set the Function 2. The setting voltage of Function 1 and Function 2 can be represented as follows :

$$V_{Function\ 1} = \frac{R2}{R1 + R2} \times V_{CC}$$

$$V_{Function\ 2} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$$

All function setting will be done within 500μs after power ready (POR).

If $V_{Function\ 1}$ and $V_{Function\ 2}$ are determined, R1 and R2 can be calculated as follows :

$$R1 = \frac{V_{CC} \times V_{Function\ 2}}{80\mu A \times V_{Function\ 1}}$$

$$R2 = \frac{R1 \times V_{Function\ 1}}{V_{CC} - V_{Function\ 1}}$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the SETx resistor network for the RT8889C.

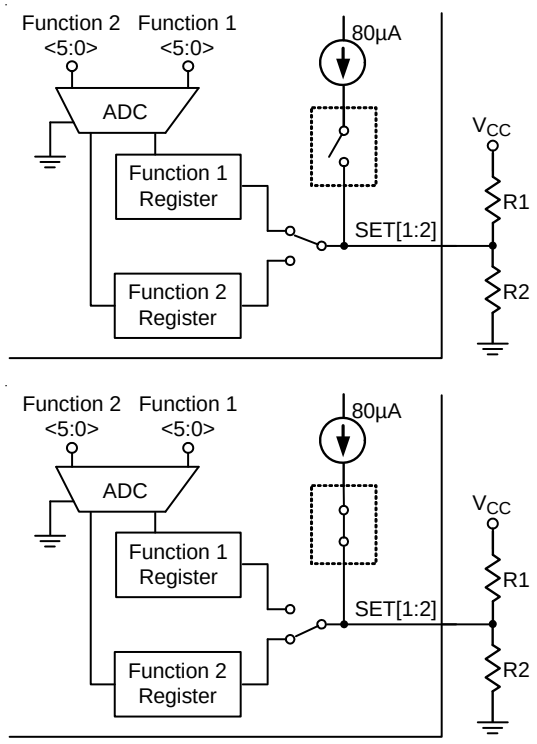



Figure 9. Multi-Function Pin Setting Mechanism

Connecting a R3 resistor from the SET[1:2] pin to the middle node of voltage divider can help to fine tune the set voltage of Function 1, which does not affect the set voltage of Function 1. The Figure 10 shows the setting method and the set voltage of Function 1 and Function 2 can be represented as :

$$V_{Function\ 1} = \frac{R2}{R1 + R2} \times V_{CC}$$

$$V_{Function\ 2} = 80\mu A \times \left( R3 + \frac{R1 \times R2}{R1 + R2} \right)$$

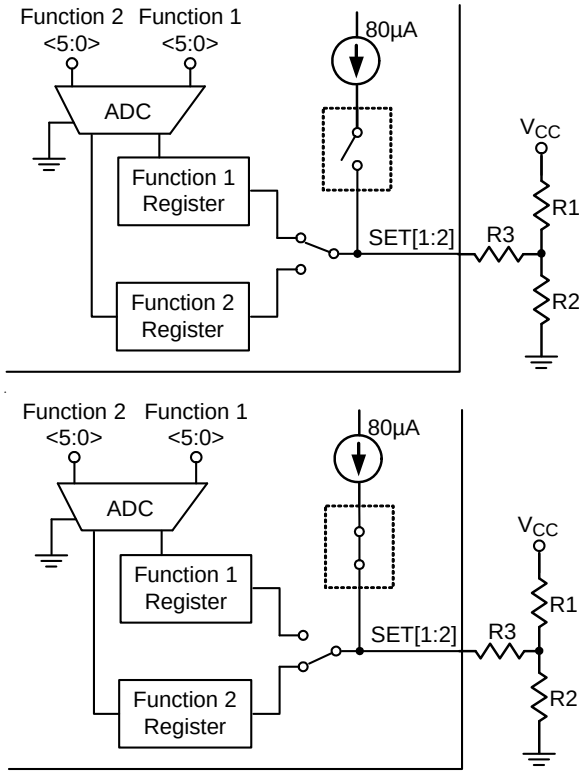



Figure 10. Multi-Function Pin Setting Mechanism with a R3 resistor to fine tune the set voltage of Function 2

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

### Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, that output voltage generate undershoot to fail specification. The RT8889C has Quick Response (QR) mechanism being able to improve this issue. It adopts a nonlinear control mechanism which can disable interleaving function and simultaneously to turn on one all UGATE pulse at instantaneous step-up transient load to restrain the output voltage drooping, Figure 11 shows the QR behavior.

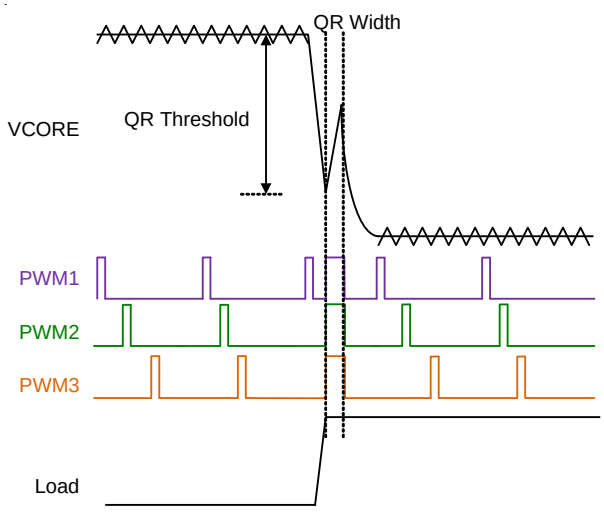



Figure 11. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at the VSEN pin that is shown in Figure 12. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 9. A proper QR mechanism set can meet different applications. The SET2 pin is a multi-function pin which can set QR threshold, QR width and ICCMAX.

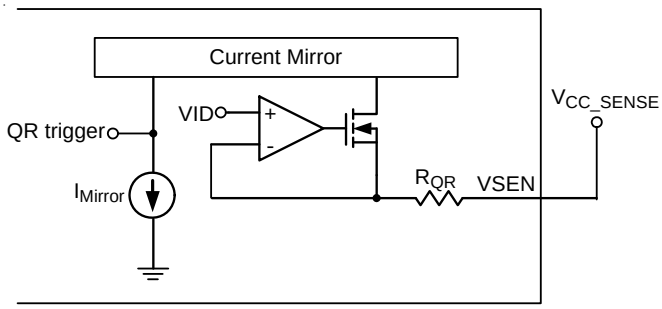



Figure 12. Simplified QR Trigger Schematic

An internal current source 80μA is used in multi-function pin setting mechanism. For example, 35mV QR threshold and 1.3 x TON QR width are set. According to the Table 5, the set voltage should be between 0.4504V and 0.4723V. Please note that a high accuracy resistor is needed for this setting accuracy, <1% error tolerance is recommended.

In the Table 5, there are some "No Use" marks in QRWIDTH section. It means that user should not use it to avoid the possibility of shift digital code due to tolerance concern.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

**Table 5 : SET2 Pin Setting for QR Threshold and QR Width**

| $V_{QR_SET} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$ | | | | | | QR Threshold | QR Width (%TON) |
|---|---|---|---|---|---|---|---|
| Min | Typical | Max | unit | QR_TH <2:0> | QRWIDTH <2:0> | | |
| 0.000 | 10.948 | 21.896 | mV | 000 | 000 | Disable | No Use |
| 25.024 | 35.973 | 46.921 | mV | | 001 | | 155% |
| 50.049 | 60.997 | 71.945 | mV | | 010 | | 133% |
| 75.073 | 86.022 | 96.970 | mV | | 011 | | 111% |
| 100.098 | 111.046 | 121.994 | mV | | 100 | | 89% |
| 125.122 | 136.070 | 147.019 | mV | | 101 | | 67% |
| 150.147 | 161.095 | 172.043 | mV | | 110 | | 44% |
| 175.171 | 186.119 | 197.067 | mV | | 111 | | No Use |
| 200.196 | 211.144 | 222.092 | mV | 001 | 000 | 30mV | No Use |
| 225.220 | 236.168 | 247.116 | mV | | 001 | | 155% |
| 250.244 | 261.193 | 272.141 | mV | | 010 | | 133% |
| 275.269 | 286.217 | 297.165 | mV | | 011 | | 111% |
| 300.293 | 311.241 | 322.190 | mV | | 100 | | 89% |
| 325.318 | 336.266 | 347.214 | mV | | 101 | | 67% |
| 350.342 | 361.290 | 372.239 | mV | | 110 | | 44% |
| 375.367 | 386.315 | 397.263 | mV | | 111 | | No Use |
| 400.391 | 411.339 | 422.287 | mV | 010 | 000 | 35mV | No Use |
| 425.415 | 436.364 | 447.312 | mV | | 001 | | 155% |
| 450.440 | 461.388 | 472.336 | mV | | 010 | | 133% |
| 475.464 | 486.413 | 497.361 | mV | | 011 | | 111% |
| 500.489 | 511.437 | 522.385 | mV | | 100 | | 89% |
| 525.513 | 536.461 | 547.410 | mV | | 101 | | 67% |
| 550.538 | 561.486 | 572.434 | mV | | 110 | | 44% |
| 575.562 | 586.510 | 597.458 | mV | | 111 | | No Use |
| 600.587 | 611.535 | 622.483 | mV | 011 | 000 | 40mV | No Use |
| 625.611 | 636.559 | 647.507 | mV | | 001 | | 155% |
| 650.635 | 661.584 | 672.532 | mV | | 010 | | 133% |
| 675.660 | 686.608 | 697.556 | mV | | 011 | | 111% |
| 700.684 | 711.632 | 722.581 | mV | | 100 | | 89% |
| 725.709 | 736.657 | 747.605 | mV | | 101 | | 67% |
| 750.733 | 761.681 | 772.630 | mV | | 110 | | 44% |
| 775.758 | 786.706 | 797.654 | mV | | 111 | | No Use |
| 800.782 | 811.730 | 822.678 | mV | 100 | 000 | 45mV | No Use |
| 825.806 | 836.755 | 847.703 | mV | | 001 | | 155% |
| 850.831 | 861.779 | 872.727 | mV | | 010 | | 133% |
| 875.855 | 886.804 | 897.752 | mV | | 011 | | 111% |
| 900.880 | 911.828 | 922.776 | mV | | 100 | | 89% |
| 925.904 | 936.852 | 947.801 | mV | | 101 | | 67% |
| 950.929 | 961.877 | 972.825 | mV | | 110 | | 44% |
| 975.953 | 986.901 | 997.849 | mV | | 111 | | No Use |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| $V_{QR_SET} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$ | | | | | | QR Threshold | QR Width (%TON) |
|---|---|---|---|---|---|---|---|
| Min | Typical | Max | unit | QR_TH <2:0> | QRWIDTH <2:0> | | |
| 1000.978 | 1011.926 | 1022.874 | mV | 101 | 000 | 50mV | No Use |
| 1026.002 | 1036.950 | 1047.898 | mV | | 001 | | 155% |
| 1051.026 | 1061.975 | 1072.923 | mV | | 010 | | 133% |
| 1076.051 | 1086.999 | 1097.947 | mV | | 011 | | 111% |
| 1101.075 | 1112.023 | 1122.972 | mV | | 100 | | 89% |
| 1126.100 | 1137.048 | 1147.996 | mV | | 101 | | 67% |
| 1151.124 | 1162.072 | 1173.021 | mV | | 110 | | 44% |
| 1176.149 | 1187.097 | 1198.045 | mV | | 111 | | No Use |
| 1201.173 | 1212.121 | 1223.069 | mV | 110 | 000 | 55mV | No Use |
| 1226.197 | 1237.146 | 1248.094 | mV | | 001 | | 155% |
| 1251.222 | 1262.170 | 1273.118 | mV | | 010 | | 133% |
| 1276.246 | 1287.195 | 1298.143 | mV | | 011 | | 111% |
| 1301.271 | 1312.219 | 1323.167 | mV | | 100 | | 89% |
| 1326.295 | 1337.243 | 1348.192 | mV | | 101 | | 67% |
| 1351.320 | 1362.268 | 1373.216 | mV | | 110 | | 44% |
| 1376.344 | 1387.292 | 1398.240 | mV | | 111 | | No Use |
| 1401.369 | 1412.317 | 1423.265 | mV | 111 | 000 | 60mV | No Use |
| 1426.393 | 1437.341 | 1448.289 | mV | | 001 | | 155% |
| 1451.417 | 1462.366 | 1473.314 | mV | | 010 | | 133% |
| 1476.442 | 1487.390 | 1498.338 | mV | | 011 | | 111% |
| 1501.466 | 1512.414 | 1523.363 | mV | | 100 | | 89% |
| 1526.491 | 1537.439 | 1548.387 | mV | | 101 | | 67% |
| 1551.515 | 1562.463 | 1573.412 | mV | | 110 | | 44% |
| 1576.540 | 1587.488 | 1598.436 | mV | | 111 | | No Use |

### Dynamic VID (DVID) Compensation

When VID transition event occurs, a charge current will be generated in the loop to cause that DVID performance is deteriorated by this induced charge current, the phenomenon is called droop effect. The droop effect is shown in Figure 13. When VID up transition occurs, the output capacitor will be charged by inductor current. Since current signal is sensed in inductor, an induced charge current will appear in control loop. The induced charge current will produce a voltage drop in R1 to cause output voltage to have a droop effect. Due to this, VID transition performance will be deteriorated.

The RT8889C provides a DVID compensation function. A virtual charge current signal can be established by the SET1 pin to cancel the real induced charge current signal and the virtual charge current signal is defined in Figure 15. Figure 14 shows the operation of canceling droop effect. A virtual charge current signal is established first and then VID signal plus virtual charge current signal is generated in FB pin. Hence, an induced charge current signal flows to R1 and is cancelled to reduce droop effect.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

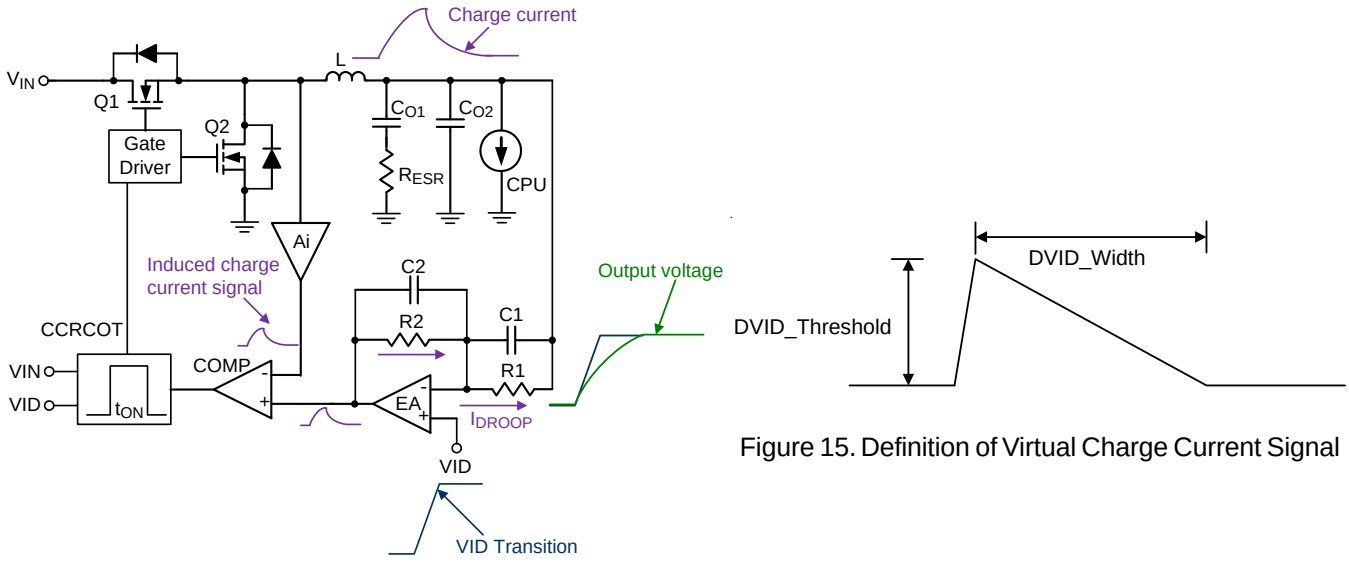



Figure 15. Definition of Virtual Charge Current Signal

Figure 13. Droop Effect in VID Transition

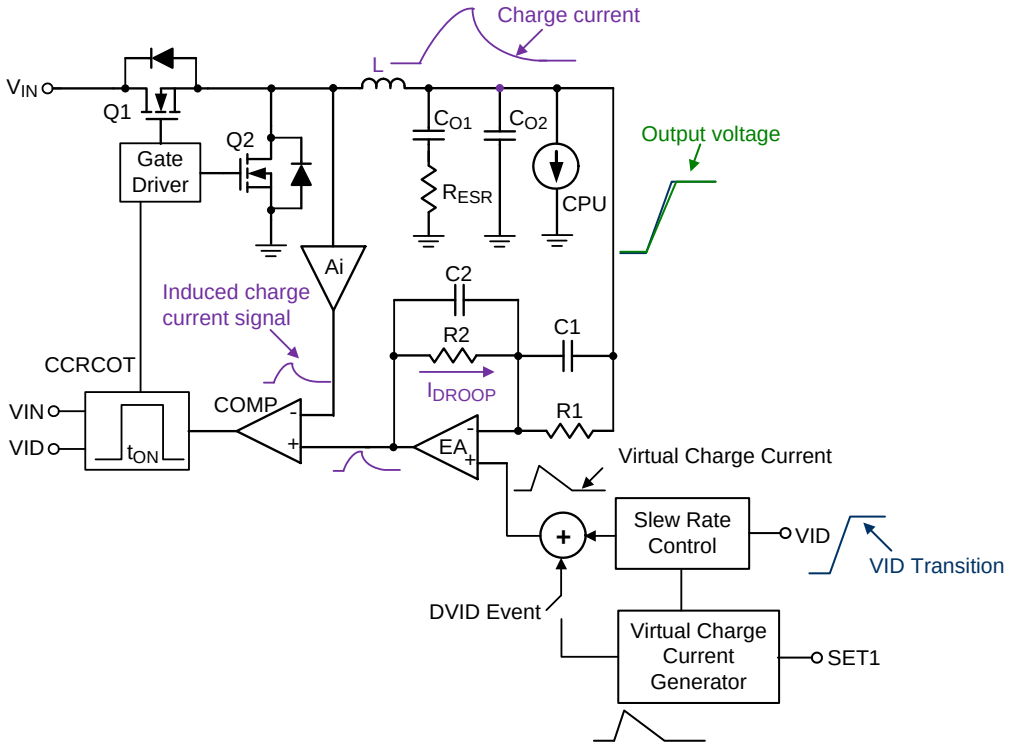



Figure 14. DVID Compensation

Table 6 and Table 7 show the DVID_Threshold and DVID_Width settings in SET1 pin. For example, 25mV DVID_Threshold and 72µs DVID_Width are designed (OCP sets as 100% ICCMAX, and RSET sets as 100% Ramp current). The DVID_Width is set by an external voltage divider to set and the DVID_Threshold is set by an internal current source 80µA by the multi-function pin setting mechanism. According to the Table 6 and Table 7, the DVID_Threshold set voltage should be between 0.225V and 0.247V and the DVID_Width set voltage should be between 0.275V and 0.297V. Please note that a high accuracy resistor is needed for this setting, <1% error tolerance is recommended.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

**Table 6 : SET1 Pin Setting for DVID_Threshold**

| $V_{DVID_Threshold} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$ | | | | | | DVID_Threshold | OCP = %ICCMAX |
|---|---|---|---|---|---|---|---|
| Min | Typical | Max | unit | DVID_TH <2:0> | OCS <2:0> | | |
| 0.000 | 10.948 | 21.896 | mV | 000 | 000 | 15mV | No Use |
| 25.024 | 35.973 | 46.921 | mV | | 001 | | 100% |
| 50.049 | 60.997 | 71.945 | mV | | 010 | | 110% |
| 75.073 | 86.022 | 96.970 | mV | | 011 | | 120% |
| 100.098 | 111.046 | 121.994 | mV | | 100 | | 130% |
| 125.122 | 136.070 | 147.019 | mV | | 101 | | 140% |
| 150.147 | 161.095 | 172.043 | mV | | 110 | | 150% |
| 175.171 | 186.119 | 197.067 | mV | | 111 | | No Use |
| 200.196 | 211.144 | 222.092 | mV | 001 | 000 | 25mV | No Use |
| 225.220 | 236.168 | 247.116 | mV | | 001 | | 100% |
| 250.244 | 261.193 | 272.141 | mV | | 010 | | 110% |
| 275.269 | 286.217 | 297.165 | mV | | 011 | | 120% |
| 300.293 | 311.241 | 322.190 | mV | | 100 | | 130% |
| 325.318 | 336.266 | 347.214 | mV | | 101 | | 140% |
| 350.342 | 361.290 | 372.239 | mV | | 110 | | 150% |
| 375.367 | 386.315 | 397.263 | mV | | 111 | | No Use |
| 400.391 | 411.339 | 422.287 | mV | 010 | 000 | 35mV | No Use |
| 425.415 | 436.364 | 447.312 | mV | | 001 | | 100% |
| 450.440 | 461.388 | 472.336 | mV | | 010 | | 110% |
| 475.464 | 486.413 | 497.361 | mV | | 011 | | 120% |
| 500.489 | 511.437 | 522.385 | mV | | 100 | | 130% |
| 525.513 | 536.461 | 547.410 | mV | | 101 | | 140% |
| 550.538 | 561.486 | 572.434 | mV | | 110 | | 150% |
| 575.562 | 586.510 | 597.458 | mV | | 111 | | No Use |
| 600.587 | 611.535 | 622.483 | mV | 011 | 000 | 45mV | No Use |
| 625.611 | 636.559 | 647.507 | mV | | 001 | | 100% |
| 650.635 | 661.584 | 672.532 | mV | | 010 | | 110% |
| 675.660 | 686.608 | 697.556 | mV | | 011 | | 120% |
| 700.684 | 711.632 | 722.581 | mV | | 100 | | 130% |
| 725.709 | 736.657 | 747.605 | mV | | 101 | | 140% |
| 750.733 | 761.681 | 772.630 | mV | | 110 | | 150% |
| 775.758 | 786.706 | 797.654 | mV | | 111 | | No Use |
| 800.782 | 811.730 | 822.678 | mV | 100 | 000 | 55mV | No Use |
| 825.806 | 836.755 | 847.703 | mV | | 001 | | 100% |
| 850.831 | 861.779 | 872.727 | mV | | 010 | | 110% |
| 875.855 | 886.804 | 897.752 | mV | | 011 | | 120% |
| 900.880 | 911.828 | 922.776 | mV | | 100 | | 130% |
| 925.904 | 936.852 | 947.801 | mV | | 101 | | 140% |
| 950.929 | 961.877 | 972.825 | mV | | 110 | | 150% |
| 975.953 | 986.901 | 997.849 | mV | | 111 | | No Use |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| $V_{DVID_Threshold} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$ | | | | | | DVID_Threshold | OCP = %ICCMAX |
|---|---|---|---|---|---|---|---|
| **Min** | **Typical** | **Max** | **unit** | **DVID_TH <2:0>** | **OCS <2:0>** | | |
| 1000.978 | 1011.926 | 1022.874 | mV | 101 | 000 | 65mV | No Use |
| 1026.002 | 1036.950 | 1047.898 | mV | | 001 | | 100% |
| 1051.026 | 1061.975 | 1072.923 | mV | | 010 | | 110% |
| 1076.051 | 1086.999 | 1097.947 | mV | | 011 | | 120% |
| 1101.075 | 1112.023 | 1122.972 | mV | | 100 | | 130% |
| 1126.100 | 1137.048 | 1147.996 | mV | | 101 | | 140% |
| 1151.124 | 1162.072 | 1173.021 | mV | | 110 | | 150% |
| 1176.149 | 1187.097 | 1198.045 | mV | | 111 | | No Use |
| 1201.173 | 1212.121 | 1223.069 | mV | 110 | 000 | 75mV | No Use |
| 1226.197 | 1237.146 | 1248.094 | mV | | 001 | | 100% |
| 1251.222 | 1262.170 | 1273.118 | mV | | 010 | | 110% |
| 1276.246 | 1287.195 | 1298.143 | mV | | 011 | | 120% |
| 1301.271 | 1312.219 | 1323.167 | mV | | 100 | | 130% |
| 1326.295 | 1337.243 | 1348.192 | mV | | 101 | | 140% |
| 1351.320 | 1362.268 | 1373.216 | mV | | 110 | | 150% |
| 1376.344 | 1387.292 | 1398.240 | mV | | 111 | | No Use |
| 1401.369 | 1412.317 | 1423.265 | mV | 111 | 000 | 85mV | No Use |
| 1426.393 | 1437.341 | 1448.289 | mV | | 001 | | 100% |
| 1451.417 | 1462.366 | 1473.314 | mV | | 010 | | 110% |
| 1476.442 | 1487.390 | 1498.338 | mV | | 011 | | 120% |
| 1501.466 | 1512.414 | 1523.363 | mV | | 100 | | 130% |
| 1526.491 | 1537.439 | 1548.387 | mV | | 101 | | 140% |
| 1551.515 | 1562.463 | 1573.412 | mV | | 110 | | 150% |
| 1576.540 | 1587.488 | 1598.436 | mV | | 111 | | No Use |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

**Table 7 : SET1 Pin Setting for DVID_Width**

| $V_{DVID_Width} = \frac{R2}{R1+R2} \times V_{CC}$ | | | | | | DVID_Width | RSET % 130k $R_{TON}$ |
|---|---|---|---|---|---|---|---|
| Min | Typical | Max | unit | DVID_WTH <2:0> | RSET <2:0> | | |
| 0.000 | 10.948 | 21.896 | mV | 000 | 000 | 48µs | No Use |
| 25.024 | 35.973 | 46.921 | mV | | 001 | | 75% |
| 50.049 | 60.997 | 71.945 | mV | | 010 | | 87.5% |
| 75.073 | 86.022 | 96.970 | mV | | 011 | | 100% |
| 100.098 | 111.046 | 121.994 | mV | | 100 | | 112.5% |
| 125.122 | 136.070 | 147.019 | mV | | 101 | | 125% |
| 150.147 | 161.095 | 172.043 | mV | | 110 | | 137.5% |
| 175.171 | 186.119 | 197.067 | mV | | 111 | | No Use |
| 200.196 | 211.144 | 222.092 | mV | 001 | 000 | 72µs | No Use |
| 225.220 | 236.168 | 247.116 | mV | | 001 | | 75% |
| 250.244 | 261.193 | 272.141 | mV | | 010 | | 87.5% |
| 275.269 | 286.217 | 297.165 | mV | | 011 | | 100% |
| 300.293 | 311.241 | 322.190 | mV | | 100 | | 112.5% |
| 325.318 | 336.266 | 347.214 | mV | | 101 | | 125% |
| 350.342 | 361.290 | 372.239 | mV | | 110 | | 137.5% |
| 375.367 | 386.315 | 397.263 | mV | | 111 | | No Use |
| 400.391 | 411.339 | 422.287 | mV | 010 | 000 | 96µs | No Use |
| 425.415 | 436.364 | 447.312 | mV | | 001 | | 75% |
| 450.440 | 461.388 | 472.336 | mV | | 010 | | 87.50% |
| 475.464 | 486.413 | 497.361 | mV | | 011 | | 100% |
| 500.489 | 511.437 | 522.385 | mV | | 100 | | 112.5% |
| 525.513 | 536.461 | 547.410 | mV | | 101 | | 125% |
| 550.538 | 561.486 | 572.434 | mV | | 110 | | 137.5% |
| 575.562 | 586.510 | 597.458 | mV | | 111 | | No Use |
| 600.587 | 611.535 | 622.483 | mV | 011 | 000 | 120µs | No Use |
| 625.611 | 636.559 | 647.507 | mV | | 001 | | 75% |
| 650.635 | 661.584 | 672.532 | mV | | 010 | | 87.50% |
| 675.660 | 686.608 | 697.556 | mV | | 011 | | 100% |
| 700.684 | 711.632 | 722.581 | mV | | 100 | | 112.50% |
| 725.709 | 736.657 | 747.605 | mV | | 101 | | 125% |
| 750.733 | 761.681 | 772.630 | mV | | 110 | | 137.5% |
| 775.758 | 786.706 | 797.654 | mV | | 111 | | No Use |
| 800.782 | 811.730 | 822.678 | mV | 100 | 000 | 144µs | No Use |
| 825.806 | 836.755 | 847.703 | mV | | 001 | | 75% |
| 850.831 | 861.779 | 872.727 | mV | | 010 | | 87.5% |
| 875.855 | 886.804 | 897.752 | mV | | 011 | | 100% |
| 900.880 | 911.828 | 922.776 | mV | | 100 | | 112.50% |
| 925.904 | 936.852 | 947.801 | mV | | 101 | | 125% |
| 950.929 | 961.877 | 972.825 | mV | | 110 | | 137.5% |
| 975.953 | 986.901 | 997.849 | mV | | 111 | | No Use |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| $V_{DVID_Width} = \frac{R2}{R1+R2} \times V_{CC}$ | | | | | | DVID_Width | RSET % 130k $R_{TON}$ |
|---|---|---|---|---|---|---|---|
| **Min** | **Typical** | **Max** | **unit** | **DVID_WTH <2:0>** | **RSET <2:0>** | | |
| 1000.978 | 1011.926 | 1022.874 | mV | 101 | 000 | 168µs | No Use |
| 1026.002 | 1036.950 | 1047.898 | mV | | 001 | | 75% |
| 1051.026 | 1061.975 | 1072.923 | mV | | 010 | | 87.5% |
| 1076.051 | 1086.999 | 1097.947 | mV | | 011 | | 100% |
| 1101.075 | 1112.023 | 1122.972 | mV | | 100 | | 112.5% |
| 1126.100 | 1137.048 | 1147.996 | mV | | 101 | | 125% |
| 1151.124 | 1162.072 | 1173.021 | mV | | 110 | | 137.5% |
| 1176.149 | 1187.097 | 1198.045 | mV | | 111 | | No Use |
| 1201.173 | 1212.121 | 1223.069 | mV | 110 | 000 | 192µs | No Use |
| 1226.197 | 1237.146 | 1248.094 | mV | | 001 | | 75% |
| 1251.222 | 1262.170 | 1273.118 | mV | | 010 | | 87.5% |
| 1276.246 | 1287.195 | 1298.143 | mV | | 011 | | 100% |
| 1301.271 | 1312.219 | 1323.167 | mV | | 100 | | 112.5% |
| 1326.295 | 1337.243 | 1348.192 | mV | | 101 | | 125% |
| 1351.320 | 1362.268 | 1373.216 | mV | | 110 | | 137.5% |
| 1376.344 | 1387.292 | 1398.240 | mV | | 111 | | No Use |
| 1401.369 | 1412.317 | 1423.265 | mV | 111 | 000 | 216µs | No Use |
| 1426.393 | 1437.341 | 1448.289 | mV | | 001 | | 75% |
| 1451.417 | 1462.366 | 1473.314 | mV | | 010 | | 87.50% |
| 1476.442 | 1487.390 | 1498.338 | mV | | 011 | | 100% |
| 1501.466 | 1512.414 | 1523.363 | mV | | 100 | | 112.5% |
| 1526.491 | 1537.439 | 1548.387 | mV | | 101 | | 125% |
| 1551.515 | 1562.463 | 1573.412 | mV | | 110 | | 137.5% |
| 1576.540 | 1587.488 | 1598.436 | mV | | 111 | | No Use |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

### Ramp Compensation

The G-NAVP™ topology is one type of ripple based control that has fast transient response, no beat frequency issue in high repetitive load frequency operation and lower BOM cost. However, ripple based control usually has no good noise immunity. The RT8889C provides a ramp compensation to increase noise immunity and reduce jitter at the switching node. Figure 16 shows the ramp compensation.

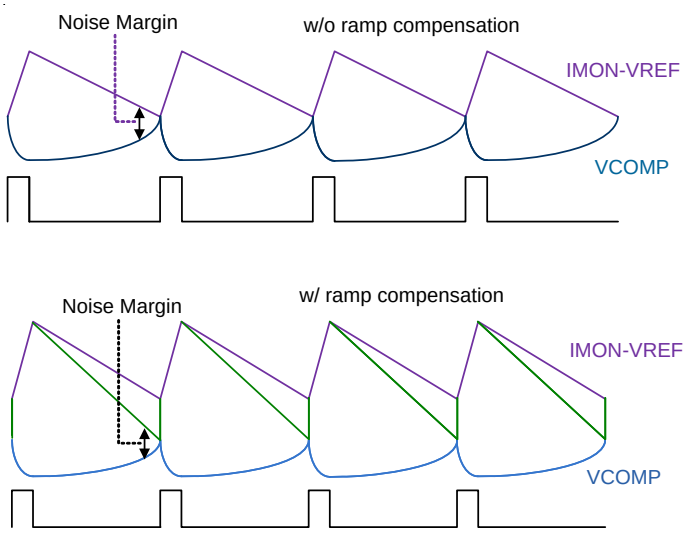



Figure 16. Ramp Compensation

For the RT8889C, the ramp compensation also needs to be considered during mode transition from PS0/1 to PS2. For achieving smooth mode transition into PS2, a proper ramp compensation design is necessary. Since the ramp compensation needs to be proportional to the on-time, in others words, ramp compensation is dependent on $R_{TON}$ design. Table 7 shows the relationship between $R_{TON}$ and ramp compensation. For example, when designed $R_{TON}$ is 100kΩ, the RAMP is set as $\frac{130k}{100k} \times 100\%$.

### Current Monitor, IMON

The RT8889C includes a current monitor (IMON) function which can be used to detect over current protection and the maximum processor current ICCMAX, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMON and the VREF pins.

The calculation for IMON-VREF voltage is shown as below :

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times (I_{L1} + I_{L2} + I_{L3})$$

Where $I_{L1} + I_{L2} + I_{L3}$ are output current and the definitions of DCR, $R_{CS}$ and $R_{EQ}$ can refer to Figure 6.

### Maximum Processor Current Setting, ICCMAX

The maximum processor current ICCMAX can be set by the SET2 pin. ICCMAX register is set by an external voltage divider by the multi-function mechanism. The Table 8 shows the ICCMAX setting in the SET2 pin. For example, $I_{CCMAX}$ = 106A, the $V_{ICCMAX}$ needs to be set as 0.67 typically. Additionally, $V_{IMON} - V_{REF}$ needs to be set as 1.6V when $I_{L1} + I_{L2} + I_{L3}$ = 106A. The ICCMAX alert signal will be pulled to low level if $V_{IMON} - V_{REF}$ = 1.6V.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

**Table 8 : SET2 Pin Setting for ICCMAX**

| $V_{ICCMAX} = \frac{R2}{R1+R2} \times V_{CC}$ | | | | ICCMAX | Unit |
|---|---|---|---|---|---|
| Min | Typical | Max | Unit | | |
| 0.000 | 3.128 | 6.256 | mV | 0 | A |
| 12.512 | 15.640 | 18.768 | mV | 2 | A |
| 25.024 | 28.152 | 31.281 | mV | 4 | A |
| 37.537 | 40.665 | 43.793 | mV | 6 | A |
| 50.049 | 53.177 | 56.305 | mV | 8 | A |
| 62.561 | 65.689 | 68.817 | mV | 10 | A |
| 75.073 | 78.201 | 81.329 | mV | 12 | A |
| 87.586 | 90.714 | 93.842 | mV | 14 | A |
| 100.098 | 103.226 | 106.354 | mV | 16 | A |
| 112.610 | 115.738 | 118.866 | mV | 18 | A |
| 125.122 | 128.250 | 131.378 | mV | 20 | A |
| 137.634 | 140.762 | 143.891 | mV | 22 | A |
| 150.147 | 153.275 | 156.403 | mV | 24 | A |
| 162.659 | 165.787 | 168.915 | mV | 26 | A |
| 175.171 | 178.299 | 181.427 | mV | 28 | A |
| 187.683 | 190.811 | 193.939 | mV | 30 | A |
| 200.196 | 203.324 | 206.452 | mV | 32 | A |
| 212.708 | 215.836 | 218.964 | mV | 34 | A |
| 225.220 | 228.348 | 231.476 | mV | 36 | A |
| 237.732 | 240.860 | 243.988 | mV | 38 | A |
| 250.244 | 253.372 | 256.500 | mV | 40 | A |
| 262.757 | 265.885 | 269.013 | mV | 42 | A |
| 275.269 | 278.397 | 281.525 | mV | 44 | A |
| 287.781 | 290.909 | 294.037 | mV | 46 | A |
| 300.293 | 303.421 | 306.549 | mV | 48 | A |
| 312.805 | 315.934 | 319.062 | mV | 50 | A |
| 325.318 | 328.446 | 331.574 | mV | 52 | A |
| 337.830 | 340.958 | 344.086 | mV | 54 | A |
| 350.342 | 353.470 | 356.598 | mV | 56 | A |
| 362.854 | 365.982 | 369.110 | mV | 58 | A |
| 375.367 | 378.495 | 381.623 | mV | 60 | A |
| 387.879 | 391.007 | 394.135 | mV | 62 | A |
| 400.391 | 403.519 | 406.647 | mV | 64 | A |
| 412.903 | 416.031 | 419.159 | mV | 66 | A |
| 425.415 | 428.543 | 431.672 | mV | 68 | A |
| 437.928 | 441.056 | 444.184 | mV | 70 | A |
| 450.440 | 453.568 | 456.696 | mV | 72 | A |
| 462.952 | 466.080 | 469.208 | mV | 74 | A |
| 475.464 | 478.592 | 481.720 | mV | 76 | A |
| 487.977 | 491.105 | 494.233 | mV | 78 | A |
| 500.489 | 503.617 | 506.745 | mV | 80 | A |

| $V_{ICCMAX} = \frac{R2}{R1+R2} \times V_{CC}$ | | | | ICCMAX | Unit |
|---|---|---|---|---|---|
| Min | Typical | Max | Unit | | |
| 513.001 | 516.129 | 519.257 | mV | 82 | A |
| 525.513 | 528.641 | 531.769 | mV | 84 | A |
| 538.025 | 541.153 | 544.282 | mV | 86 | A |
| 550.538 | 553.666 | 556.794 | mV | 88 | A |
| 563.050 | 566.178 | 569.306 | mV | 90 | A |
| 575.562 | 578.690 | 581.818 | mV | 92 | A |
| 588.074 | 591.202 | 594.330 | mV | 94 | A |
| 600.587 | 603.715 | 606.843 | mV | 96 | A |
| 613.099 | 616.227 | 619.355 | mV | 98 | A |
| 625.611 | 628.739 | 631.867 | mV | 100 | A |
| 638.123 | 641.251 | 644.379 | mV | 102 | A |
| 650.635 | 653.763 | 656.891 | mV | 104 | A |
| 663.148 | 666.276 | 669.404 | mV | 106 | A |
| 675.660 | 678.788 | 681.916 | mV | 108 | A |
| 688.172 | 691.300 | 694.428 | mV | 110 | A |
| 700.684 | 703.812 | 706.940 | mV | 112 | A |
| 713.196 | 716.325 | 719.453 | mV | 114 | A |
| 725.709 | 728.837 | 731.965 | mV | 116 | A |
| 738.221 | 741.349 | 744.477 | mV | 118 | A |
| 750.733 | 753.861 | 756.989 | mV | 120 | A |
| 763.245 | 766.373 | 769.501 | mV | 122 | A |
| 775.758 | 778.886 | 782.014 | mV | 124 | A |
| 788.270 | 791.398 | 794.526 | mV | 126 | A |
| 800.782 | 803.910 | 807.038 | mV | 128 | A |
| 813.294 | 816.422 | 819.550 | mV | 130 | A |
| 825.806 | 828.935 | 832.063 | mV | 132 | A |
| 838.319 | 841.447 | 844.575 | mV | 134 | A |
| 850.831 | 853.959 | 857.087 | mV | 136 | A |
| 863.343 | 866.471 | 869.599 | mV | 138 | A |
| 875.855 | 878.983 | 882.111 | mV | 140 | A |
| 888.368 | 891.496 | 894.624 | mV | 142 | A |
| 900.880 | 904.008 | 907.136 | mV | 144 | A |
| 913.392 | 916.520 | 919.648 | mV | 146 | A |
| 925.904 | 929.032 | 932.160 | mV | 148 | A |
| 938.416 | 941.544 | 944.673 | mV | 150 | A |
| 950.929 | 954.057 | 957.185 | mV | 152 | A |
| 963.441 | 966.569 | 969.697 | mV | 154 | A |
| 975.953 | 979.081 | 982.209 | mV | 156 | A |
| 988.465 | 991.593 | 994.721 | mV | 158 | A |
| 1000.978 | 1004.106 | 1007.234 | mV | 160 | A |
| 1013.490 | 1016.618 | 1019.746 | mV | 162 | A |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

| $V_{ICCMAX} = \frac{R2}{R1+R2} \times V_{CC}$ | | | | ICCMAX | Unit |
|---|---|---|---|---|---|
| Min | Typical | Max | Unit | | |
| 1026.002 | 1029.13 | 1032.258 | mV | 164 | A |
| 1038.514 | 1041.642 | 1044.770 | mV | 166 | A |
| 1051.026 | 1054.154 | 1057.283 | mV | 168 | A |
| 1063.539 | 1066.667 | 1069.795 | mV | 170 | A |
| 1076.051 | 1079.179 | 1082.307 | mV | 172 | A |
| 1088.563 | 1091.691 | 1094.819 | mV | 174 | A |
| 1101.075 | 1104.203 | 1107.331 | mV | 176 | A |
| 1113.587 | 1116.716 | 1119.844 | mV | 178 | A |
| 1126.100 | 1129.228 | 1132.356 | mV | 180 | A |
| 1138.612 | 1141.740 | 1144.868 | mV | 182 | A |
| 1151.124 | 1154.252 | 1157.380 | mV | 184 | A |
| 1163.636 | 1166.764 | 1169.892 | mV | 186 | A |
| 1176.149 | 1179.277 | 1182.405 | mV | 188 | A |
| 1188.661 | 1191.789 | 1194.917 | mV | 190 | A |
| 1201.173 | 1204.301 | 1207.429 | mV | 192 | A |
| 1213.685 | 1216.813 | 1219.941 | mV | 194 | A |
| 1226.197 | 1229.326 | 1232.454 | mV | 196 | A |
| 1238.710 | 1241.838 | 1244.966 | mV | 198 | A |
| 1251.222 | 1254.350 | 1257.478 | mV | 200 | A |
| 1263.734 | 1266.862 | 1269.990 | mV | 202 | A |
| 1276.246 | 1279.374 | 1282.502 | mV | 204 | A |
| 1288.759 | 1291.887 | 1295.015 | mV | 206 | A |
| 1301.271 | 1304.399 | 1307.527 | mV | 208 | A |

| $V_{ICCMAX} = \frac{R2}{R1+R2} \times V_{CC}$ | | | | ICCMAX | Unit |
|---|---|---|---|---|---|
| Min | Typical | Max | Unit | | |
| 1313.783 | 1316.911 | 1320.039 | mV | 210 | A |
| 1326.295 | 1329.423 | 1332.551 | mV | 212 | A |
| 1338.807 | 1341.935 | 1345.064 | mV | 214 | A |
| 1351.320 | 1354.448 | 1357.576 | mV | 216 | A |
| 1363.832 | 1366.960 | 1370.088 | mV | 218 | A |
| 1376.344 | 1379.472 | 1382.600 | mV | 220 | A |
| 1388.856 | 1391.984 | 1395.112 | mV | 222 | A |
| 1401.369 | 1404.497 | 1407.625 | mV | 224 | A |
| 1413.881 | 1417.009 | 1420.137 | mV | 226 | A |
| 1426.393 | 1429.521 | 1432.649 | mV | 228 | A |
| 1438.905 | 1442.033 | 1445.161 | mV | 230 | A |
| 1451.417 | 1454.545 | 1457.674 | mV | 232 | A |
| 1463.930 | 1467.058 | 1470.186 | mV | 234 | A |
| 1476.442 | 1479.570 | 1482.698 | mV | 236 | A |
| 1488.954 | 1492.082 | 1495.210 | mV | 238 | A |
| 1501.466 | 1504.594 | 1507.722 | mV | 240 | A |
| 1513.978 | 1517.107 | 1520.235 | mV | 242 | A |
| 1526.491 | 1529.619 | 1532.747 | mV | 244 | A |
| 1539.003 | 1542.131 | 1545.259 | mV | 246 | A |
| 1551.515 | 1554.643 | 1557.771 | mV | 248 | A |
| 1564.027 | 1567.155 | 1570.283 | mV | 250 | A |
| 1576.540 | 1579.668 | 1582.796 | mV | 252 | A |
| 1589.052 | 1592.180 | 1595.308 | mV | 254 | A |

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

### Over Current Protection

The RT8889C provides Over Current Protection (OCP) which is adjustable by the SET1 pin. The OCP threshold setting can refer to ICCMAX current in the Table 8. For example, if ICCMAX is set as 120A, user can set voltage by using the external voltage divider in SET1 pin as 0.466V typically if DVID_Threshold = 35mV, then 144A OCP (120% x ICCMAX) threshold will be set. When output current is higher than the OCP threshold, the OCP will be triggered with a 40µs delay time to prevent false trigger. Besides, the OCP function is masked when dynamic VID transient occurs and after dynamic VID transition, OCP is masked for 80µs.

### Over Output Voltage Protection

An OVP condition is detected when the VSEN pin is 350mV higher than VID. When OVP is detected, the high side gate voltage UGATEx is pulled-low and the low side gate voltage LGATEx is pulled-high, OVP is latched with a 0.5µs delay time to prevent false trigger.

### Negative Voltage Protection

Since the OVP latch continuously turns on all low side MOSFETs of the VR, the VR will suffer negative output voltage. When the VSEN detects a voltage below –0.05V after triggering OVP, the VR will trigger NVP to turn off all low side MOSFETs of the VR while the high side MOSFETs remains off. After triggering NVP, if the output voltage rises above 0V, the OVP latch will restart to turn on all low side MOSFETs. Therefore, the output voltage may bounce between 0V and –0.05V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered.

### Under Voltage Protection

When the VSEN pin voltage is 350mV lower than the VID voltage, a UVP will be triggered. When UVP is latched, both the UGATEx and LGATEx will be pulled-low. A 3µs delay is used in UVP detection circuit to prevent false trigger. Besides, the UVP function is masked when dynamic VID transient occurs and after dynamic VID transition, UVP is masked for 80µs.

### Under Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below POR threshold 4.1V (min), the VR will trigger UVLO. The UVLO protection forces all high side MOSFETs and low side MOSFETs off by shutting down internal PWM logic drivers.

### Power Ready (POR) Detection

During start-up, the RT8889C will detect the voltage at the voltage input pins : $V_{CC}$ ,EN and PVCC. When $V_{CC}$ > 4.45V and PVCC > 4.4V the RT8889C will recognize the power state of system to be ready (POR = high) and wait for enable command at the EN pin. After POR = high and $V_{EN}$ > 0.7V, the RT8889C will enter start-up sequence. If the voltage at any voltage pin drops below low threshold (POR = low), the RT8889C will enter power down sequence and all the functions will be disabled. Normally, connecting system voltage $V_{TT}$ (1.05V) to the EN pin is recommended.1ms (max) after the chip has been enabled, the SVID circuitry will be ready. All the protection latches (OVP, OCP, UVP) will be cleared only by VCC. The condition of $V_{EN}$ = low will not clear these latches. Figure 17 and Figure 18 show the POR detection and the timing chart for POR process, respectively.

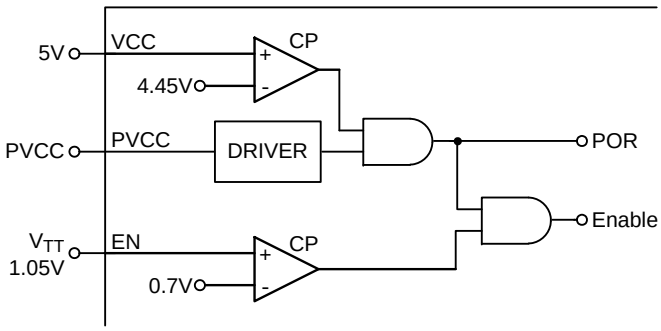



Figure 17. POR Detection

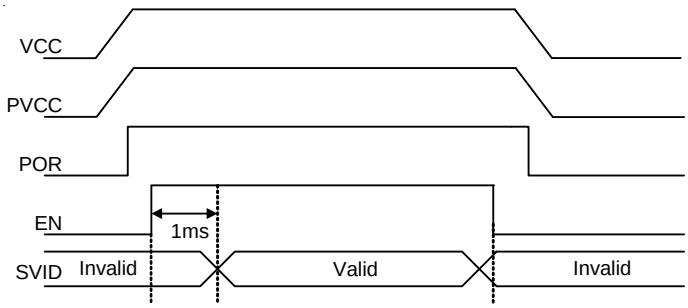



Figure 18. Timing Chart for POR Process

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

### Precise Reference Current Generation, IBIAS

Analog circuits need very precise reference voltage/current to drive/set these analog devices. The RT8889C provides a 2V voltage source at the IBIAS pin, and a 100kΩ resistor is required to be connected between IBIAS pin and analog ground to generate a very precise reference current. Through this connection, the RT8889C will generate a 20μA current from the IBIAS pin to analog ground, and this 20μA current will be mirrored inside the RT8889C for internal use. The IBIAS pin can only be connected with a 100kΩ resistor to GND for internal analog circuit use. The resistance accuracy of this resistor is recommended to be 1% or higher. Figure 19 shows the IBIAS setting circuit.

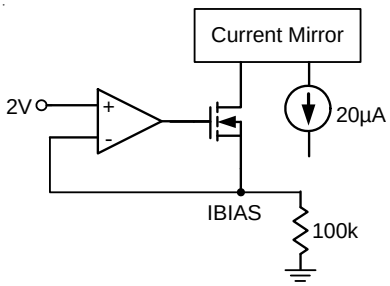



Figure 19. IBIAS Setting Circuit

### TSEN and $\overline{\text{VR_HOT}}$

The $\overline{\text{VR_HOT}}$ signal is an open-drain signal which is used for VR thermal protection. When the sensed voltage in TSEN pin is over 1.887V, the $\overline{\text{VR_HOT}}$ signal will be pulled-low to notify CPU that the thermal protection needs to work. According to Intel VR definition, $\overline{\text{VR_HOT}}$ signal needs acting if VR power chain temperature exceeds 100°C. Placing an NTC thermistor at the hottest area in the VR power chain and its connection is shown in Figure 20, to design the voltage divider elements (R1, R2 and NTC) so that VTSEN = 1.887V at 100°C. The resistance accuracy of TSEN network is recommended to be 1% or higher.

$$V_{TSEN} = V_{CC} \times \frac{R2}{R2 + \left[R1 // R_{NTC(100°C)}\right]} = 1.887V$$

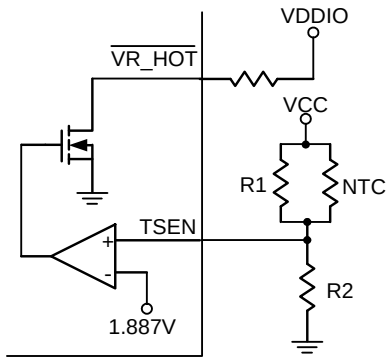



Figure 20. $\overline{\text{VR_HOT}}$ Circuit

### Differential Remote Sense Setting

The VR provides differential remote sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, $V_{CC_SENSE}$ and $V_{SS_SENSE}$. Connecting RGND to $V_{SS_SENSE}$ and FB to $V_{CC_SENSE}$ with a resistor to build the negative input path of the error amplifier. The $V_{DAC}$ and the precision voltage reference are referred to RGND for accurate remote sensing.

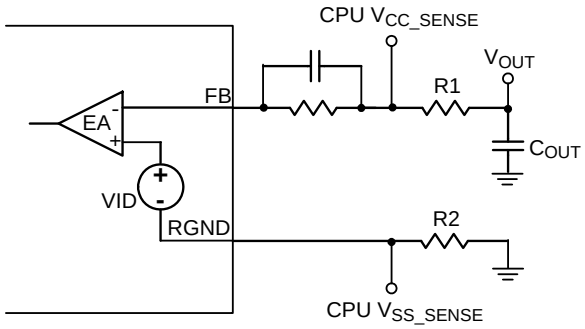



Figure 21. Remote Sensing Circuit

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

### NO Load Offset (Platform)

The RT8889C provides no load offset for platform users. Users can disable this function by pulling the SET3 pin to ground. Figure 22 shows a voltage divider used to set no load offset voltage. No load offset voltage setting is :

$$V_{OFS} = \frac{1}{2} \times (V_{SET3} - 1.2)$$

The range of $V_{OFS}$ is –250mV < $V_{OFS}$ < 600mV.

For example, a 100mV no load offset requirement, $V_{SET3}$ needs to be set as 1.4V.

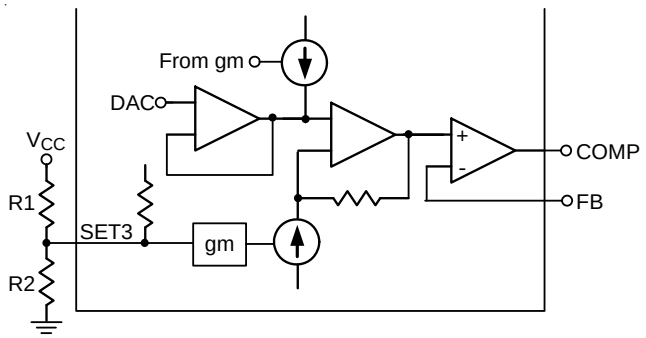



Figure 22. No Load Offset Circuit

### Phase Disable (Before POR)

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during start-up. Normally, the VR operates as a 3-phase PWM controller. Pulling ISEN3N to VCC programs a 2-phase operation, and pulling ISEN2N and ISEN3N to VCC programs a 1-phase operation. Before POR, VR detects whether the voltages of ISEN2N and ISEN3N are higher than "VCC – 1V" respectively to decide how many phases should be active. Phase selection is only active during POR. When POR = high, the number of active phases is determined and latched. The unused ISENxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

### Current Loop Design in Details

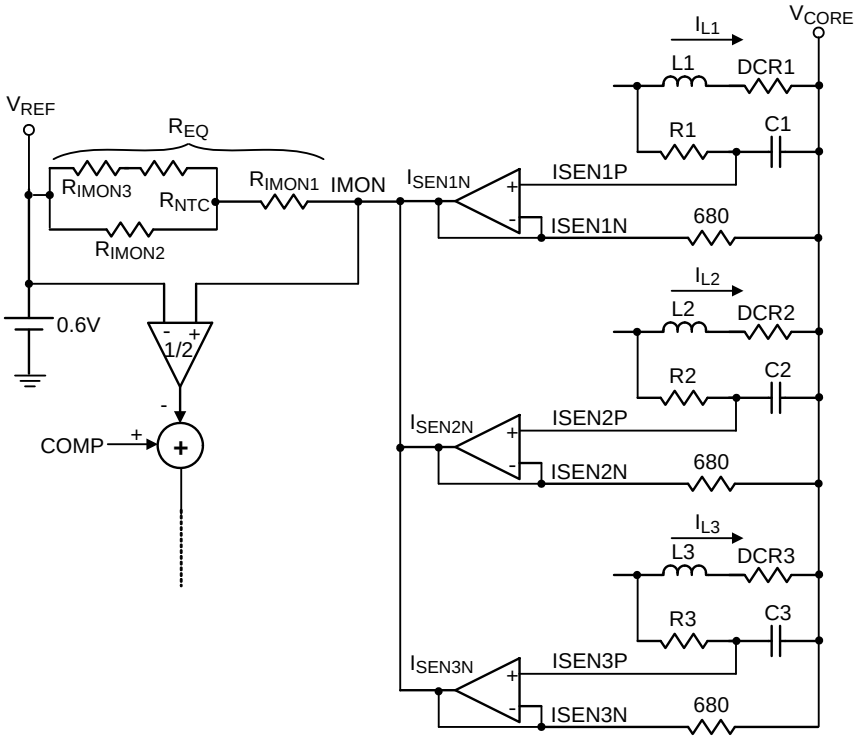



Figure 23. Current Loop Structure

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Figure 23 shows the whole current loop structure. The current loop plays an important role in the RT8889C that can decide ACLL performance, DCLL accuracy and ICCMAX accuracy. For ACLL performance, the correct compensator design is assumed, if RC network time constant matches inductor time constant $L_X/DCR_X$, an expected load transient waveform can be designed. If $R_XC_X$ network time constant is larger than inductor time constant $L_X/DCR_X$, $V_{CORE}$ waveform has a sluggish droop during load transient. If $R_XC_X$ network is smaller than inductor time constant $L_X/DCR_X$, a worst $V_{CORE}$ waveform will sag to create an undershoot to fail the specification. Figure 24 shows the variety of $R_XC_X$ constant corresponding to the output waveforms.

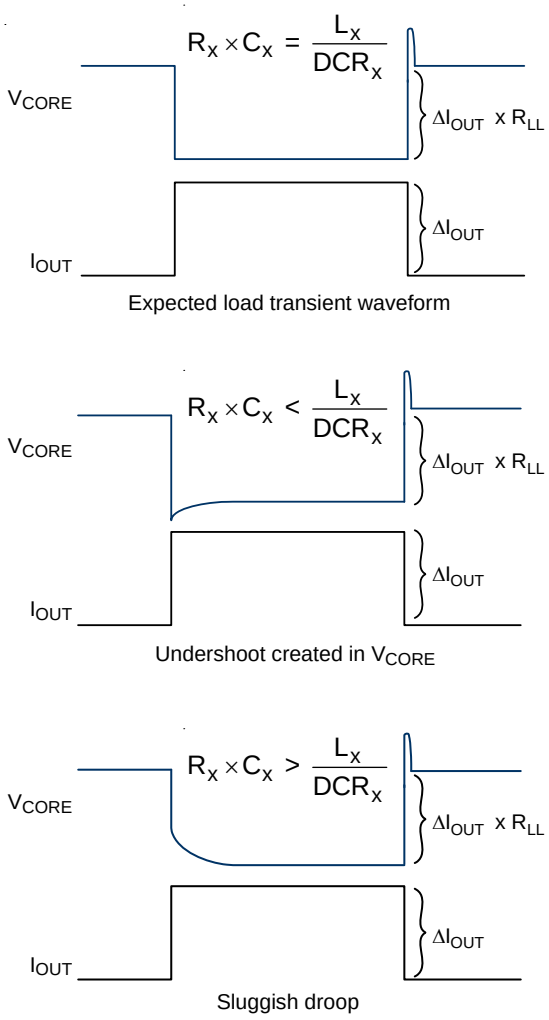



Figure 24. All Kind of $R_XC_X$ Constants

For DCLL performance and ICCMAX accuracy, since the copper wire of inductor has a positive temperature coefficient, when temperature goes high in the heavy load condition then DCR value goes large simultaneously. A resistor network with NTC thermistor compensation connecting between IMON pin and REF pin is necessary, to compensate the positive temperature coefficient of inductor DCR. The design flow is as follows :

Step1 : Given the three system temperature $T_L$, $T_R$ and $T_H$, at which are compensated.

Step2 : Three equations can be listed as

$$\frac{DCR(T_L)}{680} \times \sum_{i=1}^{4} i_{Li} \times R_{EQ}(T_L) = 1.6$$

$$\frac{DCR(T_R)}{680} \times \sum_{i=1}^{4} i_{Li} \times R_{EQ}(T_R) = 1.6$$

$$\frac{DCR(T_H)}{680} \times \sum_{i=1}^{4} i_{Li} \times R_{EQ}(T_H) = 1.6$$

Where :

(1) The relationship between DCR and temperature is as follows :

$$DCR(T) = DCR(25°C) \times [1 + 0.00393(T - 25)]$$

(2) $R_{EQ}(T)$ is the equivalent resistor of the resistor network with a NTC thermistor

$$R_{EQ}(T) = R_{IMON1} + \{R_{IMON2} // [R_{IMON3} + R_{NTC}(T)]\}$$

And the relationship between NTC and temperature is as follows :

$$R_{NTC}(T) = R_{NTC}(25°C) \times e^{\beta(\frac{1}{T+273} - \frac{1}{298})}$$

$\beta$ is in the NTC thermistor datasheet.

Step3 : Three equations and three unknowns, $R_{IMON1}$, $R_{IMON2}$ and $R_{IMON3}$ can be found out unique solution.

$$R_{IMON1} = K_{TR} - \frac{R_{IMON2} \times (R_{NTCTR} + R_{IMON3})}{R_{IMON2} + R_{NTCTR} + R_{IMON3}}$$

$$R_{IMON2} = \sqrt{[K_{R3}^2 + K_{R3}(R_{NTCTL} + R_{NTCTR}) + R_{NTCTL}R_{NTCTR}]\alpha_{TL}}$$

$$R_{IMON3} = -R_{IMON2} + K_{R3}$$

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Where :

$$\alpha_{TH} = \frac{K_{TH} - K_{TR}}{R_{NTCTH} - R_{NTCTR}}$$

$$\alpha_{TL} = \frac{K_{TL} - K_{TR}}{R_{NTCTL} - R_{NTCTR}}$$

$$K_{R3} = \frac{(\alpha_{TH} / \alpha_{TL})R_{NTCTH} - R_{NTCTL}}{1 - (\alpha_{TH} / \alpha_{TL})}$$

$$K_{TL} = \frac{1.6}{G_{CS(TL)} \times I_{CC\text{-}MAX}}$$

$$K_{TR} = \frac{1.6}{G_{CS(TR)} \times I_{CC\text{-}MAX}}$$

$$K_{TH} = \frac{1.6}{G_{CS(TH)} \times I_{CC\text{-}MAX}}$$

**Design Step :**

The RT8889C Excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. Three main design procedures for the RT8889C design, first step is initial settings, second step is loop design and the last step is protection settings. The following design example is to explain RT8889C design procedure :

| | **$V_{CORE}$ Specification** |
|---|---|
| Input Voltage | 12V |
| No. of Phases | 3 |
| Vboot | 1.7V |
| $V_{DAC(MAX)}$ | 1.85V |
| ICCMAX | 90A |
| ICC-DY | 60A |
| ICC-TDC | 55A |
| Load-Line | 1.5mΩ |
| Fast Slew Rate | 12.5mV/μs |
| Max Switching Frequency | 300kHz |

In Shark Bay VRTB Guideline, the output filter requirements of VRTB specification for desktop platform are as follows :

Output Inductor : 360nH/0.72mΩ

Output Bulk Capacitor : 560μF/2.5V/5mΩ (max) 4 to 5pcs

Output Ceramic Capacitor : 22μF/0805 (18pcs max sites on top side)

(1) Initial Settings :

- RT8889C initial voltage is 1.7V
- IBIASE needs to connect a 100kΩ resistor to ground.

(2) Loop Design :

- On time setting : Using the specification, $T_{ON}$ is

$$t_{ON} = \frac{1}{f_{SW(MAX)}} \times \frac{V_{DAC(MAX)}}{V_{IN}} = 514n(s)$$

The on time setting resistor $R_{TON}$ = 130kΩ

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expected load transient waveform, $R_xC_x$ time constant needs to match $L_X/DCR_X$ per phase. $C_x$ = 1μF is set, then

$$R_X = \frac{L_X}{1\mu F \times DCR_X} = 500\Omega$$

- IMON resistor network design : $T_L$ = 25°C, $T_R$ = 50°C and $T_H$ = 100°C are decided, NTC thermistor = 100kΩ @25°C, β = 4485 and ICCMAX = 90A. According to the sub-section "Current Loop Design in Details", $R_{IMON1}$ = 5.43kΩ, $R_{IMON2}$ = 12.6kΩ and $R_{IMON3}$ = 13.9kΩ can be decided. The $R_{EQ}$ (25°C) = 16.8kΩ.

- Load-line design : 1.5mΩ droop is required, because $R_{EQ}$ (25°C) is decided, the voltage loop Av gain is also decided by the following equation :

$$R_{LL} = \frac{A_V}{A_I} = \frac{\frac{1}{2} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} \ (m\Omega)$$

Where DCR (25°C) = 0.72mΩ, $R_{CS}$ = 680Ω and $R_{EQ}$ (25°C) = 16.8kΩ. Hence the $A_V = R_2 / R_1$ = 5.92 can be obtained. $R_1$ = 10kΩ usually is decided, so $R_2$ = 59.2kΩ.

- Typical compensator design can use the following equations to design the $C_1$ and $C_2$ values

$$C_1 = \frac{1}{R_1 \times \pi \times f_{SW}} \approx 106pF$$

$$C_2 = \frac{C_{OUT} \times ESR}{R_2} \approx 79pF$$

For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the compensator of zero can be designed close to 1/10 of switching frequency.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

- SET1 resistor network design : First the DVID compensation parameters need to be decided. The DVID_TH can be calculated as the following equation :

$$V_{DVID_TH} = LL \times C_{OUT} \times \frac{DVID}{dt}$$

Where LL is load-line, $C_{OUT}$ is total output capacitance and dVID/dt is DVID fast slew rate. Thus $V_{DVID_TH}$ = 45mV is needed in this case. And DVID_Width is chosen as 72μs typically. Next, OCP threshold is designed as 1.4 x ICCMAX. Last, RAMP = $R_{TON}$ / 130kΩ = 100%, 100% is set. By using above information, the two equations can be listed by using multi-function pin setting mechanism

$$0.286 = \frac{R2}{R1 + R2} \times 5$$

$$0.737 = 80\mu A \times \left(\frac{R1 \times R2}{R1 + R2}\right)$$

R1 = 160kΩ, R2 = 9.77kΩ.

- SET2 resistor network design : the QR mechanism parameters need to be designed first. Initial QR_TH is designed as 0.4 x LL x ICC-DY = 36mV and QR_Width is designed as 1.11 x $T_{ON}$. The ICCMAX is designed as 90A. By using the information, the two equations can be listed by using multi-function pin setting mechanism

$$0.566 = \frac{R2}{R1 + R2} \times 5$$

$$0.486 = 80\mu A \times \left(\frac{R1 \times R2}{R1 + R2}\right)$$

R1 = 53.7kΩ, R2 = 6.86kΩ.

- No load offset function disabled. Just connect a 0Ω resistor from SET3 pin to ground.

(3) Protection Settings :

- OVP/UVP protections : When the VSEN pin voltage is 350mV more than VID, the OVP will be latched. When the VSEN pin voltage is 350mV less than VID, the UVP will be latched.
- TSEN and $\overline{VR_HOT}$ design : Using the following equation to calculate related resistances for $\overline{VR_HOT}$ setting.

$$V_{TSEN} = V_{CC} \times \frac{R2}{R2 + \left[R_{NTC(100°C)} \,//\, R1\right]} = 1.887V$$

Choosing R1 = 100kΩ and an NTC thermistor $R_{NTC}$ (25°C) = 100kΩ which β =4485. When temperature is 100°C, the $R_{NTC}$(100°C) = 4.85kΩ.Then $R_2$ = 2.8kΩ can be calculated.

**Thermal Considerations**

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a WQFN-40L 5x5, the thermal resistance, $\theta_{JA}$, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.64W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 25 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

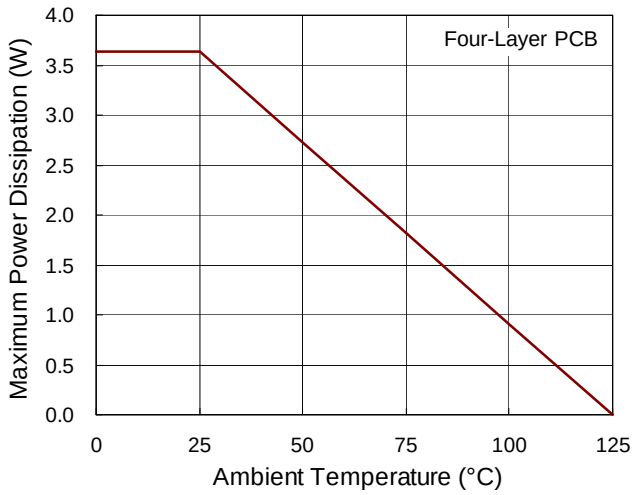



Figure 25. Derating Curve of Maximum Power Dissipation

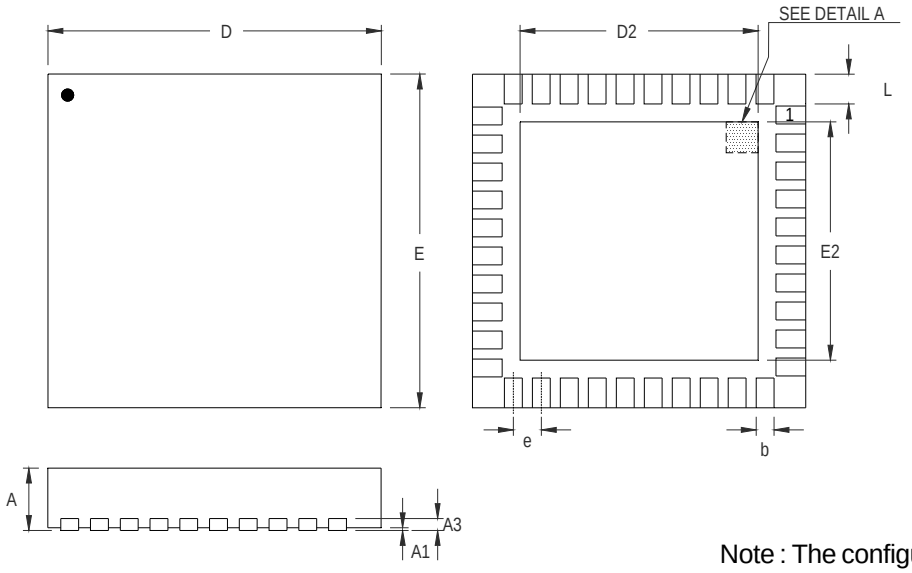
## Layout Considerations

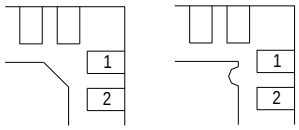
Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for optimum PC board layout :

- Keep the high current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- When trade-offs in trace lengths must be made, it's preferable to let the inductor charging path be longer than the discharging path.
- Place the current sense component close to the controller. ISENxP and ISENxN connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee current sense accuracy. The PCB trace from the sense nodes should be paralleled back to the controller.
- Route high speed switching nodes away from sensitive analog areas (COMP, FB, ISENxP, ISENxN, etc...)
- Connect the exposed pad to a strong ground plane through low impedance path. Recommend use of at least 5 vias to connect to ground planes in PCB internal layers.

Copyright ©2017 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 4.950 | 5.050 | 0.195 | 0.199 |
| D2 | 3.250 | 3.500 | 0.128 | 0.138 |
| E | 4.950 | 5.050 | 0.195 | 0.199 |
| E2 | 3.250 | 3.500 | 0.128 | 0.138 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

**W-Type 40L QFN 5x5 Package**

**Richtek Technology Corporation**

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

Richtek products are sold by description only. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.