Low-Power, Integrated ECG/PPG AFE for Heart-Rate Monitoring and Measurements

General Description

The RT1025 is an integrated AFE solution for Heart-Rate monitoring and measurements. The RT1025 integrates low noise voltage and current sensing channels and is capable of sensing ECG (Electrocardiography) and PPG (Photoplethysmography) simultaneously. The RT1025 have > 100dB dynamic range and can sense pulses accurately by detecting the heart's electric signals. The sampling rates of the high-precision voltage and current sensing channels in the RT1025 are configurable between 64 to 4kHz. The RT1025 solution need only few discrete components and is easy to use for low-power medical ECG/PPG, sports, and fitness applications. With high levels of integration and high-precision voltage and current sensing channels, the RT1025 solution is suitable for scalable medical instrumentation systems.

The RT1025 is available in a 3.1mm x 3.4mm, 41-Ball, 0.4mm pitch, WL-CSP package.

Ordering Information

RT1025 □

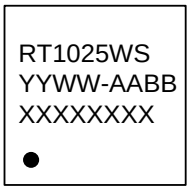
Package Type
WS : WL-CSP-41B 3.10x3.48 (BS)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT1025WS : Product Number
YYWW : Date code
AABB : Version, fad, OSAT & Pb free code
XXXXXXXX : Lot ID number

Features

- **ECG Channel Feature**
  - **Supports Two-Electrode (2E) Mode and Right Leg Drive (RLD) Mode**
  - **Low Noise PGA and High Resolution ADC**
  - **Input Impedance : 125M to 500MΩ at Two-Electrode Mode and > 1GΩ at Right Leg Drive Mode**
  - **Low Input-Referred Noise : 0.67μVrms (64Hz ODR, Gain = 12)**
  - **Dynamic Range : 110dB at Gain = 6**
  - **CMRR > 85dB at 60Hz**
  - **Data rate : 64SPS to 4k SPS**
- **PPG Channel Feature**
  - **Flexible Timing Control and Support Dynamic Power Down**
  - **TX Supports H-bridge and Push/Pull Mode**
  - **TX LED Current Range : 10 / 25 / 35 / 50 / 65 / 75 / 90 / 105mA, Each with 8-bit Current Resolution**
  - **Input Maximum Current Range : 0.5 to 50μA**
  - **Input Maximum Capacitance : 1nF**
  - **Input-Referred Noise : 50pA$_{rms}$ at 5μA Input Current**
  - **CMRR > 80dB at 60Hz**
  - **PGA Gain : 1 to 6V/V**
  - **Ambient DAC1/DAC2 Range : 1 to 6μA**
- **Others**
  - **2-in-1 Bio-Sensing AFE (Voltage/Current)**
  - **Built-In Heartbeat Interval Estimation**
  - **Integrates an Oscillator to offer High-Precision Clock with External Crystal**
  - **Support I^{2}C and SPI I/F for MCU**
  - **On-Chip SRAM for Data Buffering**
  - **Ultra-Low Power Consumption**
  - **Operating Temperature Range : –20°C to 65°C**
  - **Small 3.1mm x 3.4mm, 41-Ball, 0.4mm Pitch, and WL-CSP Package**
  - **RoHS Compliant and Halogen Free**

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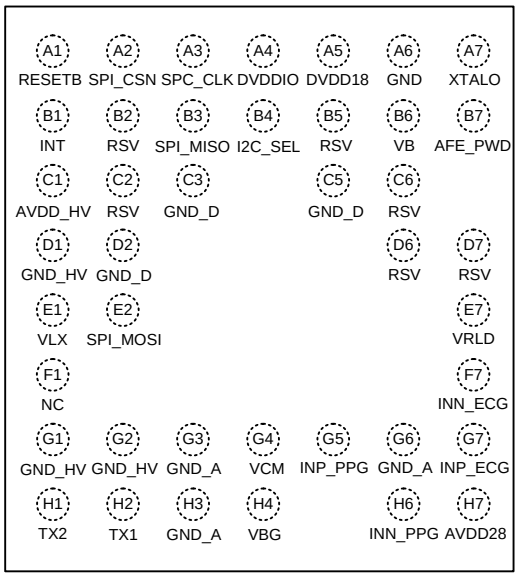
Applications

- Medical Instrumentation (ECG) including :
  - Heart Rate, Respiration, and Single-Lead ECG
- Medical Instrumentation (PPG) including :
  - Optical Heart-Rate Monitoring (HRM)
  - Heart-Rate Variability (HRV)
  - Pulse Oximetry (SpO2 Measurement)
  - VO2 Max
- Sports and Fitness Wearable Devices
- High-Precision, Simultaneous, Multichannel Signal Acquisition

Pin Configuration

(TOP VIEW)



WL-CSP-41B 3.10x3.48 (BS)

Part Status

Part No	Status	Package Type
RT1025WS	Lifebuy	WL-CSP-41B 3.10x3.48 (BS)

The part status values are defined as follows :

Active : Device is in production and is recommended for new designs.

Lifebuy : The device will be discontinued, and a lifetime-buy period is in effect.

NRND : Not recommended for new designs.

Preview : Device has been announced but is not in production.

EOL : Richtek has discontinued the production of the device.

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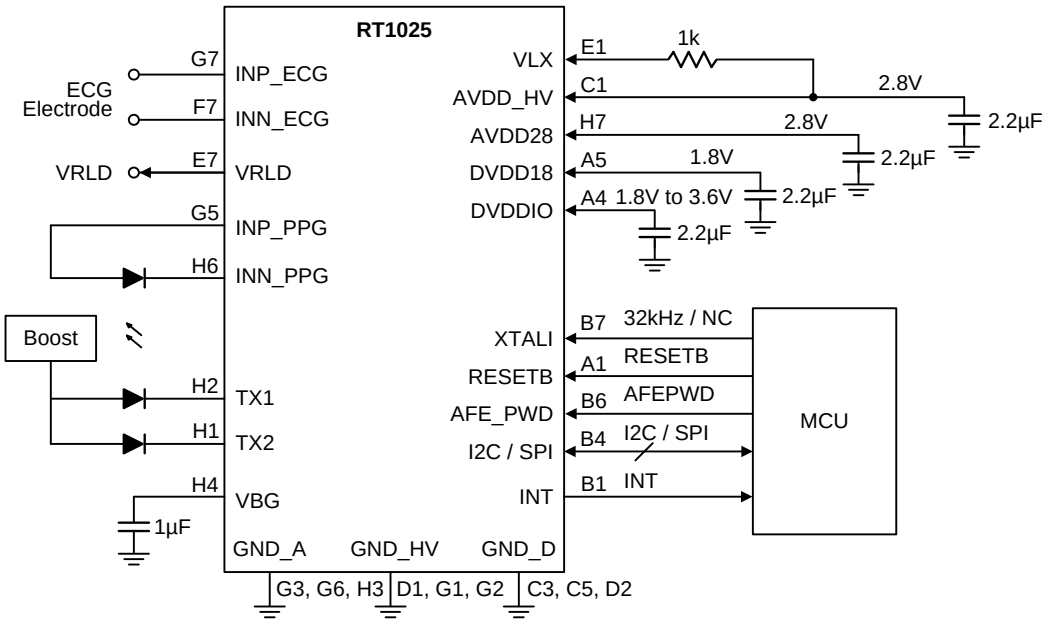
Typical Application Circuit

Using RT1025 for ECG/PPG Sensing



Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
A1	RESETB	DIO	Reset pin. Can be connected to an external MCU.
A2	SPI_CSN = SDA	DIO	(1) SPI mode : SPI data pin. (SPI_CSN) (2) I^2C mode : I^2C data pin. (I2C_SDA)
A3	SPI_CLK = SCL	DIO	(1) SPI mode : SPI clock pin. (SPI_CLK) (2) I^2C mode : I^2C clock pin. (I2C_SCL)
A4	DVDDIO	P	Digital IO supply. 2.2µF decoupling capacitor to ground.
A5	DVDD18	P	Digital supply. 2.2µF decoupling capacitor to ground.
A6	GND	DIO	Tied to ground.
A7	XTALO	AIO	Crystal oscillator pins. Connect an external 32kHz crystal with 22pF decoupling capacitor. If with external clock source, leave floating.
B1	INT	DO	Interrupt pin. Can be connected to an external MCU.
B2, B5, C2, C6, D6, D7	RSV	DIO	Reserve for testing. (leave floating)
B3	SPI_MISO	DIO	SPI serial out master in.
B4	I2C_SEL	DIO	(1) SPI mode : please keep I2C_SEL low. (2) I^2C mode : please keep I2C_SEL high.
B6	AFE_PWD	DIO	Power down pin. Can be connected to an external MCU
B7	XTALI	AIO	Crystal oscillator pins. Connect an external 32kHz crystal with 22pF decoupling capacitor. It can be connected to an external 32kHz clock source.
C1	AVDD_HV	P	PPG LED driver power. 2.2µF decoupling capacitor to ground.

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Pin No.	Pin Name	Type	Pin Function
C3, C5, D2	GND_D	G	Digital ground. Connected to common board ground.
D1, G1, G2	GND_HV	G	High voltage driver ground. Connected to common board ground.
E1	VLX	AI	PPG circuit bias
E2	SPI_MOSI	DIO	(1) SPI mode : SPI serial in master out. (2) I^2C mode : I^2C slave address (7-bit mode) a. H = 7-bit slave address (hex)) = 37 and 27 b. L = 7-bit slave address (hex)) = 33 and 23
E7	VRLD	AO	RLD output. (leave floating at 2E mode)
F1	NC		Leave floating.
F7	INN_ECG	AI	ECG IA negative input.
G3, G6, H3	GND_A	G	Analog ground. Connected to common board ground.
G4	VCM	AI	PPG input common mode voltage. (leave floating)
G5	INP_PPG	AI	PPG receiver input pin. Connected to photodiode anode.
G7	INP_ECG	AI	ECG IA positive input.
H1	TX2	AO	LED driver output. Connected to LED.
H2	TX1	AO	LED driver output. Connected to LED.
H4	VBG	AIO	Bandgap output voltage. 1μF decoupling capacitor to ground.
H6	INN_PPG	AI	PPG receiver input pin. Connected to photodiode cathode.
H7	AVDD28	P	Analog supply. 2.2μF decoupling capacitor to ground.

Pin type :

AI : Analog Input, AO : Analog Input, AIO : Analog I/O, DI : Digital Input, DO : Digital Output, DIO : Digital I/O,

P : Power, G : GND

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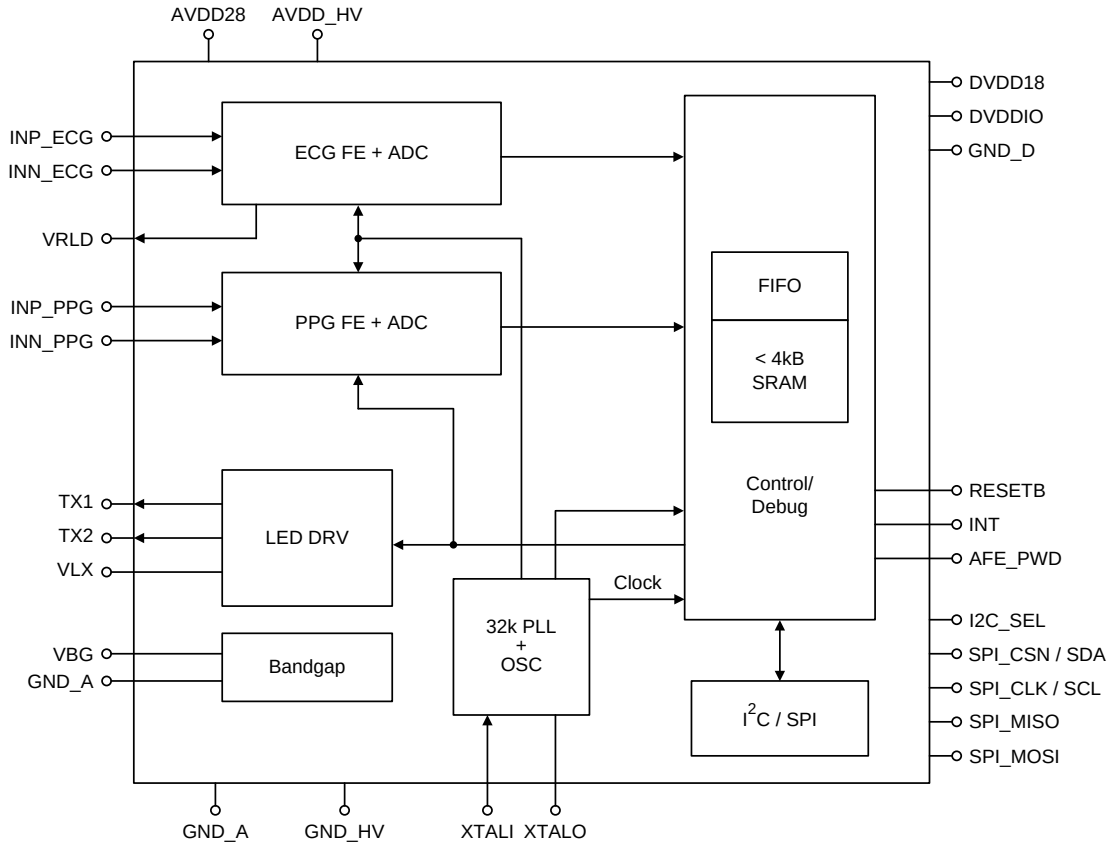
Functional Block Diagram



Operation

ECG FE + ADC

The ECG channel supports two-electrode (2E) mode and right leg drive (RLD) mode. It integrates a programmable gain amplifier (PGA), a right leg drive amplifier, and a 24-bit sigma-delta analog-to-digital converter (ADC) to sense and digitize the ECG signal.

PPG FE +ADC

The PPG channel is separated into two parts : Receiver (RX) and Transmitter (TX). The RX consists of a trans-impedance amplifier (TIA), a programmable gain amplifier (PGA), an ambient digital-to-analog converter (DAC), and a 24-bit incremental ADC.

LED DRV

The TX part of the PPG channel consist of LED driver to light up external LED.

Bandgap

The Bandgap block provides the internal reference voltage.

32kHz PLL

The PLL block offers high-precision clock with external crystal.

Control/Debug

The RT1025 supports on-chip SRAM for data buffering. There are 1kB SRAM for ECG channel, 2kB SRAM for 2PPG channels, and 1kB SRAM for heartbeat internal detection channel. The SRAM buffering allows the MCU to stay in idle mode for power saving.

I^2C/SPI

The RT1025 provides I^2C/SPI dual interface. The maximum SPI Clock operates at a frequency of 2MHz. The maximum I^2C Clock operates at a frequency of 200kHz.

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Absolute Maximum Ratings (Note 1)

- Supply Voltage, DVDDIO ---------- –0.3V to 4V
- Supply Voltage, DVDD18 ---------- –0.3V to 4V
- Supply Voltage, AVDD28 ---------- –0.3V to 4V
- Supply Voltage, AVDD_HV ---------- –0.3V to 4.5V
- DC Input Current at VIN < 0V or VIN > VDD, IIN ---------- –20mA to 20mA
- DC Output Current at VOUT < 0V or VOUT > VDD, IOUT ---------- –20mA to 20mA
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-41B 3.10x3.48 (BS) ---------- 3.75W
- Package Thermal Resistance (Note 2)

  WL-CSP-41B 3.10x3.48 (BS), θ_{JA} ---------- 26.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –40°C to 125°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Ambient Temperature Range ---------- –20°C to 65°C
- Junction Temperature Range ---------- –40°C to 125°C
- Supply Voltage, DVDDIO ---------- 1.62V to 3.3V
- Supply Voltage, DVDD18 ---------- 1.62V to 1.98V
- Supply Voltage, AVDD28 ---------- 2.66V to 2.94V
- Supply Voltage, AVDD_HV (Note 5, 6) ---------- 3.4V to 4.5V

Electrical Characteristics

(T_A = 25°C, 200kHz I^2C interface)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Digital IO Voltage Input	DVDDIO		1.62	2.8	3.3	V
Digital Core Circuit Voltage Input	DVDD18		1.62	1.8	1.98	V
Analog Main Voltage Input	AVDD28		2.66	2.8	2.94	V
Analog Secondary Voltage Input	AVDD_HV		3.4	4	4.5	V
Idle mode current	I_{Idle}	AVDD28 = 2.8V, AVDD_HV = 4V DVDD18 = 1.8V, DVDDIO = 2.8V	--	< 7	--	μA
ECG mode current	I_{ECG}	AVDD28 = 2.8V, AVDD_HV = 4V DVDD18 = 1.8V, DVDDIO = 2.8V	--	570	--	μA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PPG Mode Current @125Hz ODR	I_{PPG}	AVDD28 = 2.8V, AVDD_HV = 4V DVDD18 = 1.8V, DVDDIO = 2.8V	--	430	--	μA
PPG1 + HBI Mode Current @ 125Hz ODR	$I_{PPG1+BI}$	AVDD28 = 2.8V, AVDD_HV=4V DVDD18 = 1.8V, DVDDIO=2.8V	--	470	--	μA
PPG1 + PPG2 Mode Current @ 125Hz ODR	$I_{PPG1+PPG2}$	AVDD28=2.8V, AVDD_HV = 4V DVDD18 = 1.8V, DVDDIO = 2.8V	--	460	--	μA
ECG + PPG1 Mode Current ECG @ 512Hz ODR and PPG1 @ 512Hz ODR	$I_{ECG+PPG1}$	AVDD28=2.8V, AVDD_HV=4V DVDD18=1.8V, DVDDIO=2.8V	--	780	--	μA
Operating Temperature Range	T_C		–20	--	65	°C
ECG						
ECG Analog Inputs						
Full-Scale Differential Input Voltage			--	±1.9/ GAIN	--	mV
Input Capacitance		RLD mode	--	30	--	pF
		Two-electrode mode	--	190	--	
DC Input Impedance		RLD mode	1000	--	--	mΩ
		Two-electrode mode	--	500	--	
ECG IA Performance						
Gain Settings			--	1, 2, 3, 4, 6, 8, 12	--	V/V
Bandwidth			--	650, 250, 135, 100, 65, 50, 35	--	kHz
ECG Low-Pass Filter						
Low-Pass Corner Frequency		3-dB attenuation	--	28, 112	--	kHz
ECG ADC Performance						
Resolution			--	--	23	Bits
Data Rate			64	--	4096	SPS
ECG Channel Performance						
Input-referred noise		Gain = 1, 4096Hz ODR	--	15.2	--	μVrms
		Gain = 12, 4096Hz ODR	--	1.69	--	
		Gain = 6, 64Hz ODR	--	0.8	--	
		Gain = 12, 64Hz ODR	--	0.67	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Common-Mode Rejection		f_{CM} = 50Hz, 60Hz	--	85	--	dB
Power-Supply Rejection		f_{PS} = 50Hz, 60Hz	100	--	--	dB
Total Harmonic Distortion	THD	100Hz, –0.5dBFs	--	78	--	dB
		100Hz, –20dBFs	--	105	--	dB
PPG						
PPG Full-Signal Chain						
Full-Scale Input Current	IN_{FS}	R_F = 10kΩ	--	50	--	μA
		R_F = 25kΩ	--	20	--	
		R_F = 50kΩ	--	10	--	
		R_F = 100kΩ	--	5	--	
		R_F = 250kΩ	--	2	--	
		R_F = 50kΩ	--	1	--	
		R_F = 1MΩ	--	0.5	--	
Pulse Repetition Frequency	PRF		64	--	4096	SPS
PRF Duty Cycle	$Duty_{PRF}$		1	--	25	%
Common-Mode Rejection Ratio	CMRR	f_{CM} = 50Hz and 60Hz, R_{SERIES} = 100kΩ, R_F = 100KΩ	--	80	--	dB
Power-Supply Rejection Ratio	PSRR	f_{CM} = 50Hz and 60Hz, PRF = 125Hz	80	--	--	dB
Power-Supply Rejection Ratio		R_F = 100kΩ with stage2 gain = 1.5, PRF = 1300Hz, duty cycle = 5%	--	52	--	dB
Total Integrated Noise Current, Input Referred (Receiver with Transmitter Loop Back, 0.1Hz to 20Hz Bandwidth)		R_F = 500kΩ with ambient cancellation enabled and stage2 gain = 6, PRF = 1300Hz, duty cycle = 25%	--	7.2	--	pArms
PPG Receiver Functional Block Level Specification						
Total Integrated Noise Current, Input Referred (Receiver Alone) Over 0.1Hz to 5Hz Bandwidth		R_F = 500kΩ with ambient cancellation enabled and stage2 gain = 6, PRF = 1300Hz, duty cycle = 25%	--	1.25	--	pArms
		R_F = 500kΩ with ambient cancellation enabled and stage2 gain = 6, PRF = 1300Hz, duty cycle = 5%	--	3.85	--	
PPG I-V Transimpedance Amplifier						
Feedback Resistance	R_F		--	10k, 25k, 50k, 100k, 250k, 500k, 1M	--	Ω

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Capacitance	C_F		--	5, 10, 25, 50, 100, 250	--	pF
Common-Mode Voltage on Input Pins		Set internally	--	1.25	--	V
External Differential Input Capacitance		Include equivalent capacitance of photodiode, cables, EMI filter, and so forth	--	--	1000	pF
PPG Ambient Cancellation Stage						
Gain	G		--	1, 1.5, 2, 3, 4, 6	--	V/V
Current Range			1	--	6	μA
Current DAC Step Size			--	1	--	μA
PPG Low-Pass Filter						
Low-Pass Corner Frequency		3-dB attenuation	--	0.5, 1, 2, 4	--	kHz
PPG Analog-To-Digital Converter						
Resolution			16	--	--	Bits
Sample Rate			--	4 x PRF	--	SPS
ADC Full-Scale Voltage			--	±1.6	--	V
ADC Conversion Time			60	--	--	μs
ADC Reset Time			0.95	--	--	μs
PPG Transmitter						
Output Current Range			--	10/ 25/ 35/ 50/ 65/ 75/ 90/ 105	--	mA
Output Current Accuracy			--	±10	--	%
Output Current Resolution			--	8	--	Bits
Minimum Sample Time of LED1 and LED2 Pulses			--	50	--	μs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CLOCK						
External Clock DC Range	DC_XTAL		0	--	2.8	V
External Clock Voltage	V_XTAL		400	--	--	mVpp
External Clock Tolerance	TOLXTAL		–100	--	100	ppm
Others						
DIO						
Input Logic-High	V_{IH}		0.65 x VDD	--	VDD+ 0.3	V
Input Logic-Low	V_{IL}		–0.3	--	0.35x VDD	V
Output Logic-High, Push-Pull	V_{OH}	I_{OH} = -1mA	0.75 x VDD	--	--	V
Output Logic-Low, Push-Pull	V_{OL}	I_{OL} = 1mA	--	--	0.25x VDD	V
SPI / I^2C						
Input Logic-High	V_{IH}		0.65 x VDD	--	VDD + 0.3	V
Input Logic-Low	V_{IL}		–0.3	--	0.35 x VDD	V
Output Logic-High, Push-Pull	V_{OH}	I_{OH} = –1mA	0.75 x VDD	--	--	V
Output Logic-Low, Push-Pull	V_{OL}	I_{OL} = 1mA	--	--	0.25 x VDD	V
I^2C SCL Clock Rate	f_{SCL}		--	--	400	kHz
SPI CLK Clock Rate	f_{SPI_CLK}		--	--	2	MHz

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. LED external boost voltage – VLED (off state = no leakage current) ≤ AVDD_HV node voltage (3.4V to 4.2V).

Note 6. TXP/TXN node voltage ≤ AVDD_HV node voltage ≤ 4.5V.

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Application Information

The RT1025 supports the reading of samples and device status upon interrupt or via polling. It contains 4kB SRAM for data buffering. The device is internally clocked to offer high-precision clock with external crystal. The flexible timing control enable the users to control the PPG device timing for different application and to power down the device for power saving. The device can connect as a slave to either a SPI or I^2C master.

Operational Modes

The device has various modes of operation as described below :

Mode	Description and Comments
IDLE	The internal regulators are enabled, and much of the chip is disabled. The IDLE mode is the default POR mode
ECG	ECG channel enable for two-electrode input and right leg drive output
PPG PPG1 / PPG2 PPG + HBI PPG1 + PPG2	PPG channel enable for external LED drivers and receiver for PPG acquisition PPG1 : PPG channel1 enable for single external LED driver and receiver for PPG acquisition PPG2 : PPG channel2 enable for single external LED driver and receiver for PPG acquisition HBI : Enable digital built-in heartbeat interval (HBI) detector to enhance heart rate monitoring application for approximate wavelength of major tone. PPG1 + PPG2 : PPG channel can sense up to four channels (two for signal and two for ambient) by time multiplexing. In this mode, the device enable for dual external LED drivers and receiver for PPG acquisition
ECG + PPG	The device can enable PPG channel and ECG channel at the same time

Reset

The device can be completely reset via pin RESETB, which can be connected to an external MCU. Pull the RESTB to logic low will cause a power-on reset operation to execute. No attempt should be made to access registers within 5mSec after issuing this operation.

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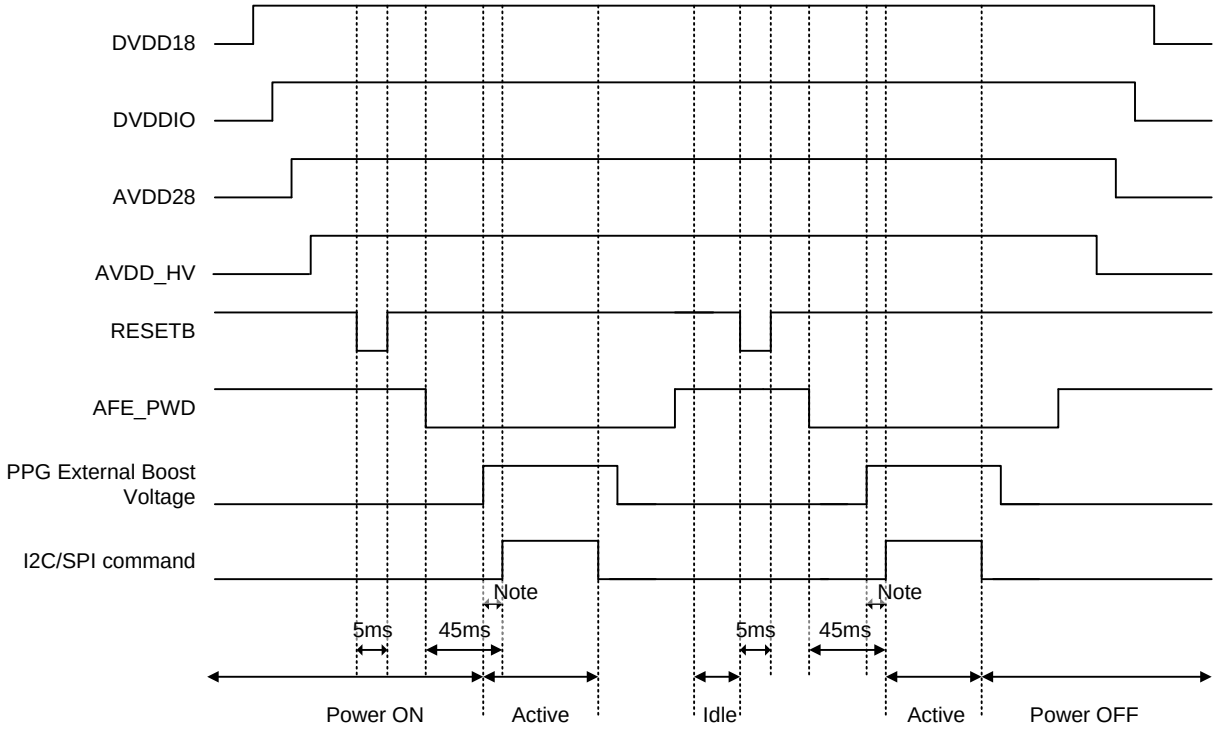
Power on Sequence

Below figure shows the power on sequence for the device supply voltage and control signals.



Note : Settling time of the PPG external boost voltage source

SPI / I²C Interface

The RT1025 device contains both I²C slave and SPI slave interfaces which share some pins. Only one of the interface can be operated after the device completes POR or a hard reset. I²C interface supports fast mode (bit rate up to 400kB/s). SPI interface operate at 2MHz. I²C or SPI interface was selected by pin I2C_SEL (B4). The I²C device address depends upon the state of pin SPI_MOSI (E2) during power-up as shown in the table below.

I/O Pin	I2C_SEL (B4)	SPI_MOSI (E2)	Reg 7-bit Address	Reg 7-bit Address
			Reg_0	Reg_1
I2C	Logic High	Logic High	0x37	0x27
		Logic Low	0x33	0x23
SPI	Logic Low	SPI slave input	0x33	0x23

I²C Interface

The I²C slave interface operates at a maximum speed of 400KHz in I²C “Fast Mode”. The SDA (data) is an Active drive/wired-and, bi-directional pin and the SCL (clock) is an input pin. The device always operates as an I²C slave and only uses 7-bit addressing.

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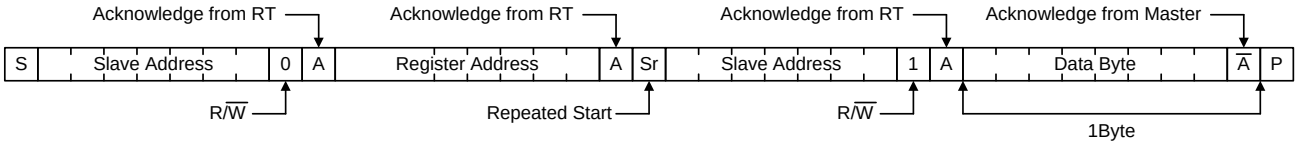
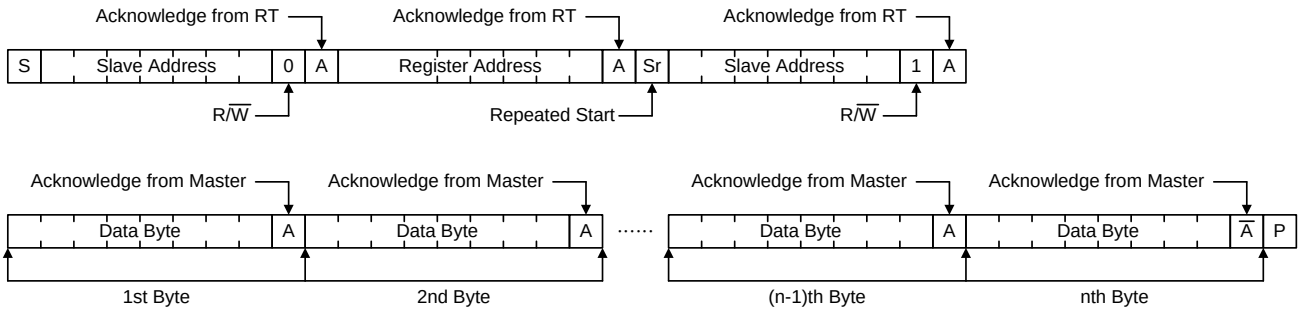
Read Function

■ Reading One Indexed Byte of Data from RT (With 1-Byte)

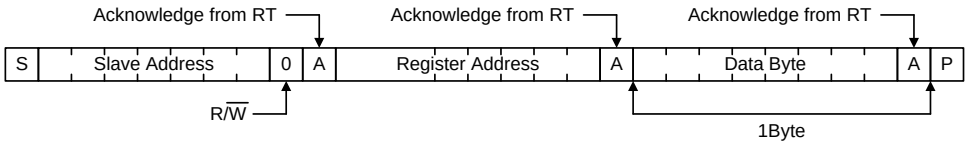


■ Reading n Indexed Words of Data from RT (With N-Byte)

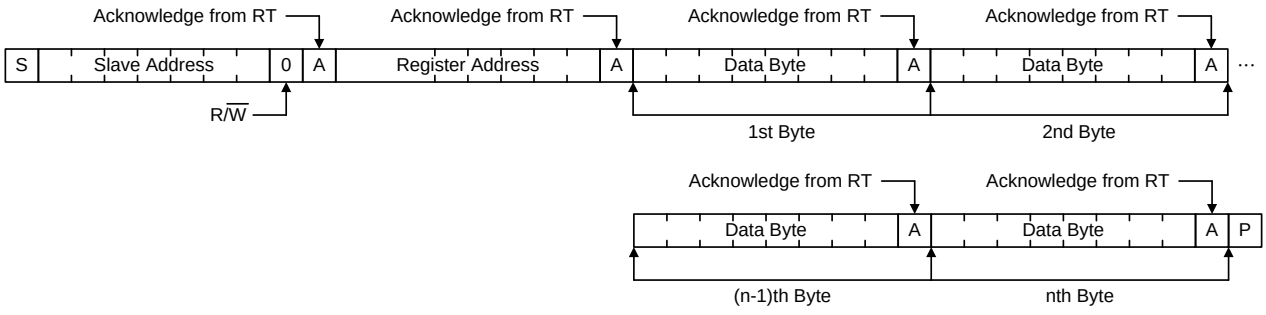


Write Function

■ Writing One Indexed Byte of Data to RT (With 1-Byte)



■ Writing n Indexed Words of Data to RT (With N-Byte)



SPI Interface

The general protocol for the SPI interface is shown in the figures below. The falling edge of CSN initiates the start of the SPI bus cycle. The first byte of the transaction is the command/address byte. When the SPI master is writing data, data may change when the clock is low, and must be stable on the clock rising edge. Similarly, output data written to the SPI master is shifted out on the falling edge of clock and can be latched by the master on the rising edge of the clock. The SPI slave controller data format is LSBF (least significant bit first). The setup/hold/idle time should be

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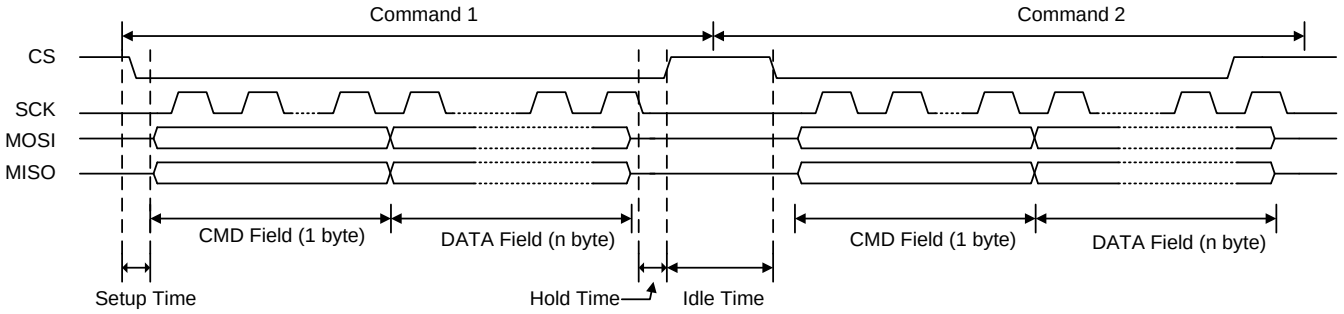
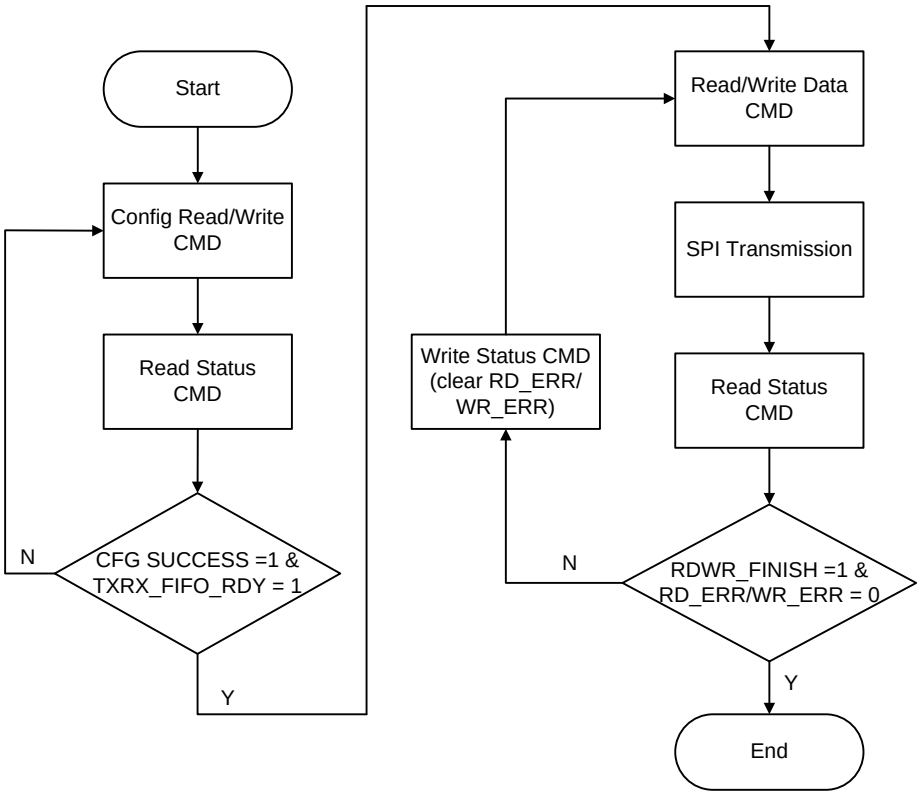
greater than 1μs.



The SPI slave control flow is shown in below.



First, SPI slave controller transmits “config-read/write” command to configure the transfer data length and read/write address of the memory. After the SPI slave is configured, it can send/receive data package with SPI master by “read/write-data” command. In each state, SPI master transmits “read-status” command to poll SPI slave situation. If SPI master detects error flag bit of state, it should send “write-status” command to clear the bit and poll this bit until it turns low.

CMD Field [7:0]	Default Code	Data Field	Usage
Read Data (RD)	0x81	N Bytes. Burst data payload	Master read data
Write Data (WD)	0x06	N Bytes. Burst data payload	Master write data
Read Status (RS)	0x0A	1 Byte	Master read slave status register

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CMD Field [7:0]	Default Code	Data Field	Usage
Write Status (WS)	0x08	1 Byte	Master write slave status register to clear error bit
Config Status (CR)	0x02	2 Bytes address 2 Bytes data length	Master configure slave to start read data
Config Status (CW)	0x04	2 Bytes address 2 Bytes data length	Master configure slave to start write data

SPI slave status description, use “Read Status (RS)” command to poll SPI slave status.

Function	Bit	Usage
SR_CFG_SUCCESS	1	Master checks this bit to know if CW/CR command is successful.
SR_TXRX_FIFO_RDY	2	If master configures read/write, when slave is ready to send/receive data, the master can send RD/WD command. Clean : After SPI slave receives CR/CW command.
SR_RD_ERR	3	After a RD command, master can read this bit to know if there is error in the read transfer. If there is error, master should send WS command to clear this bit and poll this bit until this bit turns 0.
SR_WR_ERR	4	After a WD command, master can read this bit to know if there is error in the write transfer. If there is error, master should send WS command to clear this bit and poll this bit until this bit turns 0.
SR_RDWR_FINISH	5	After RD/WD transaction, master can poll this bit to know if the read/write transfer is finished. Clean: After SPI slave receives CR/CW command.
SR_TIMOUT_ERR	6	SPI slave does not receive or send data over 31.75μs, the flag of timeout will rise. If there is error, master should send WS command to clear this bit and poll this bit until this bit turns 0.
SR_CMD_ERR	7	If master sends an error CMD at the first byte, master can know the error status through the received data. Clean : after SPI slave receivers correct command.

Register Interface

The device has a simple register interface which allows an SPI or I^2C master to configure and monitor all aspects of the device. Below table lists an overview of user programmable registers. By convention, bit 0 is the least significant bit (LSB) of a byte register.

Interrupt Register Interface

Register Module : Reg_0		I^2C address : 0x33 or 0x37 SPI address : 0x33	
Address	**Name**	**Width**	**Register Function**
0000004C	INT_CON	32	Interrupt control register
00000054	INT_STATUS	32	Interrupt status register

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PPG Channel Register Interface

Register Module : Reg_0		I²C address : 0x33 or 0x37 SPI address : 0x33	
Address	**Name**	**Width**	**Register Function**
00000060	AFE_DIG_ENABLE	32	AFE Digital Part Enable
00000018	PPGFE_CON0	32	PPGFE Control 0
0000001C	PPGFE_CON1	32	PPGFE Control 1
00000020	PPGADC_CON0	32	PPGADC Control 0
00000028	LEDDRV_CON0	32	LED Driving Control 0
0000002C	LEDDRV_CON1	32	LED Driving Control 1
00000068	AFE_PPG_CON	32	PPG Digital Part Control
000000D0	PPG1_SRAM_CON4	32	PPG1 SRAM Control 0
000000D4	PPG1_SRAM_CON5	32	PPG1 SRAM Control 1
000000D8	PPG1_SRAM_CON6	32	PPG1 SRAM Control 2
000000DC	PPG1_SRAM_CON7	32	PPG1 SRAM Control 3
000000E0	PPG2_SRAM_CON8	32	PPG2 SRAM Control 0
000000E4	PPG2_SRAM_CON9	32	PPG2 SRAM Control 1
000000E8	PPG2_SRAM_CON10	32	PPG2 SRAM Control 2
000000EC	PPG2_SRAM_CON11	32	PPG2 SRAM Control 3

PPG Channel Timing Control Register Interface

Register Module : Reg_1		I²C address : 0x23 or 0x27 SPI address : 0x23	
Address	**Name**	**Width**	**Register Function**
00000028	AFE_TCTRL_CON0	32	Timing Control Module Control 0
0000002C	AFE_TCTRL_CON1	32	Timing Control Module Control 1
00000030	AFE_TCTRL_CON2	32	Timing Control Module Control 2
00000034	AFE_TCTRL_CON3	32	Timing Control Module Control 3
00000038	AFE_TCTRL_CON4	32	Timing Control Module Control 4
0000003C	AFE_TCTRL_CON5	32	Timing Control Module Control 5
00000040	AFE_TCTRL_CON6	32	Timing Control Module Control 6
00000044	AFE_TCTRL_CON7	32	Timing Control Module Control 7
00000048	AFE_TCTRL_CON8	32	Timing Control Module Control 8
0000004C	AFE_TCTRL_CON9	32	Timing Control Module Control 9

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Address	Name	Width	Register Function
00000050	AFE_TCTRL_CON10	32	Timing Control Module Control 10
00000054	AFE_TCTRL_CON11	32	Timing Control Module Control 11
00000058	AFE_TCTRL_CON12	32	Timing Control Module Control 12
0000005C	AFE_TCTRL_CON13	32	Timing Control Module Control 13
00000060	AFE_TCTRL_CON14	32	Timing Control Module Control 14
00000064	AFE_TCTRL_CON15	32	Timing Control Module Control 15
00000068	AFE_TCTRL_CON16	32	Timing Control Module Control 16
0000006C	AFE_TCTRL_CON17	32	Timing Control Module Control 17
00000070	AFE_TCTRL_CON18	32	Timing Control Module Control 18

ECG Channel Register Interface

Register Module : Reg_0		I^2C address : 0x33 or 0x37 SPI address : 0x33	
Address	**Name**	**Width**	**Register Function**
00000008	ECGFE_CON0	32	ECGFE Control
00000010	ECGADC_CON0	32	ECGADC Control
00000064	AFE_ECG_CON	32	ECG Digital Part Control
000000C0	ECG_SRAM_CON0	32	ECG SRAM Control 0
000000C4	ECG_SRAM_CON1	32	ECG SRAM Control 1
000000C8	ECG_SRAM_CON2	32	ECG SRAM Control 2
000000CC	ECG_SRAM_CON3	32	ECG SRAM Control 3

HBI Estimation Register Interface

Register Module : Reg_0		I^2C address : 0x33 or 0x37 SPI address : 0x33	
Address	**Name**	**Width**	**Register Function**
000000F0	HBI_SRAM_CON12	32	HBI SRAM Control 0
000000F4	HBI_SRAM_CON13	32	HBI SRAM Control 1
000000F8	HBI_SRAM_CON14	32	HBI SRAM Control 2
000000FC	HBI_SRAM_CON15	32	HBI SRAM Control 3

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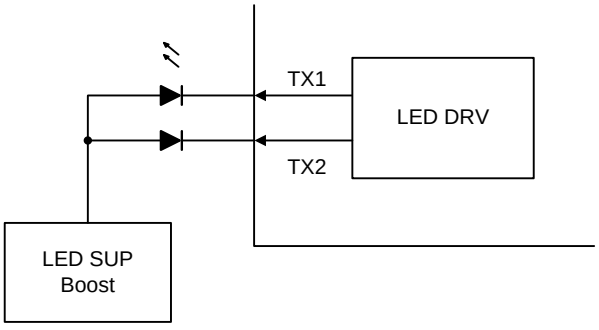
Interrupts

To facilitate MCU programming and sensor data flow control, the RT1025 supports various interrupts for each function. The INT_CON register enables or disables interrupts on various events. Host MCU can identify the exact cause of interrupt by reading the INT_STATUS register. Below table lists supported interrupts and their usage.

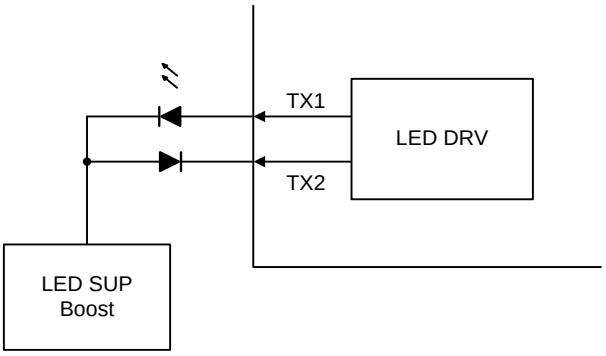
Interrupt	Description
SRAM_ECG	ECG SRAM threshold level is reached
SRAM_ECG_WFULL	ECG SRAM is full.
SRAM_ECG_REMPTY	ECG SRAM is empty
SRAM_PPG1	PPG1 SRAM threshold level is reached
SRAM_PPG1_WFULL	PPG1 SRAM is full
SRAM_PPG1_REMPTY	PPG1 SRAM is empty
SRAM_PPG2	PPG2 SRAM threshold level is reached
SRAM_PPG2_WFULL	PPG2 SRAM is full
SRAM_PPG2_REMPTY	PPG2 SRAM is empty
SRAM_HBI	HBI SRAM threshold level is reached
SRAM_HBI_WFULL	HBI SRAM is full
SRAM_HBI_REMPTY	HBI SRAM is empty

PPG Channel

The LED driver and the external voltage boost are used to light up the external LED. The LED full scale current range is from 10mA to 105mA with a 3-bit current step of 15mA via DAC register setting. Push-Pull mode and H-Bridge mode of the LED driver schemes are supported. Suggest to use Push-Pull LED driving configuration as shown in below figure. The minimum external supply voltage (LED_SUP) = 0.7V + (maximum voltage drop across the LED).



Push-Pull Mode



H-Bridge Mode

PPG Channel - Receiver Front-End

As shown in the block diagram for PPG acquisition, the photo detector transfers the reflected light into current and then amplifies by TIA that converts the input photodiode current into an appropriate voltage. TIA_Filter was controlled by the register for the input current low pass filter tuning. PGA_Gain was used to set the PGA Gain. AMB_DAC control the current source to cancel the ambient light leakage from photo detector. The AMB_DAC has a cancellation current range of 6μA with six steps (1μA each) for two phases (LED1/LED2 phase and AMB1/AMB2 phase). The

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PGA amplifier gains up the photo detector input and has five programmable gain settings : 1, 1.5, 2, 3, 4, and 6 (V/V). Then, the signals are sampled by the corresponding LPFs and digitized by a 16-bit incremental ADC.

The PPG acquisition outputs 24 bits of data per channel in binary twos complement format, MSB first. Bit [22] is sign bit. A positive full-scale input produces an output code of 3FFFFFh and the negative full-scale input produces an output code of 400000h. The output clips at these codes for signals exceeding full-scale. All 23 bits toggle when the analog input is at positive or negative full-scale.

$$PPG\ (mV) = 2 \times \left[(I_{PD} + I_{AMB}) \times \frac{R_F}{100k} - I_{AMB\_DAC}\right] \times 100k \times PGA\ gain$$

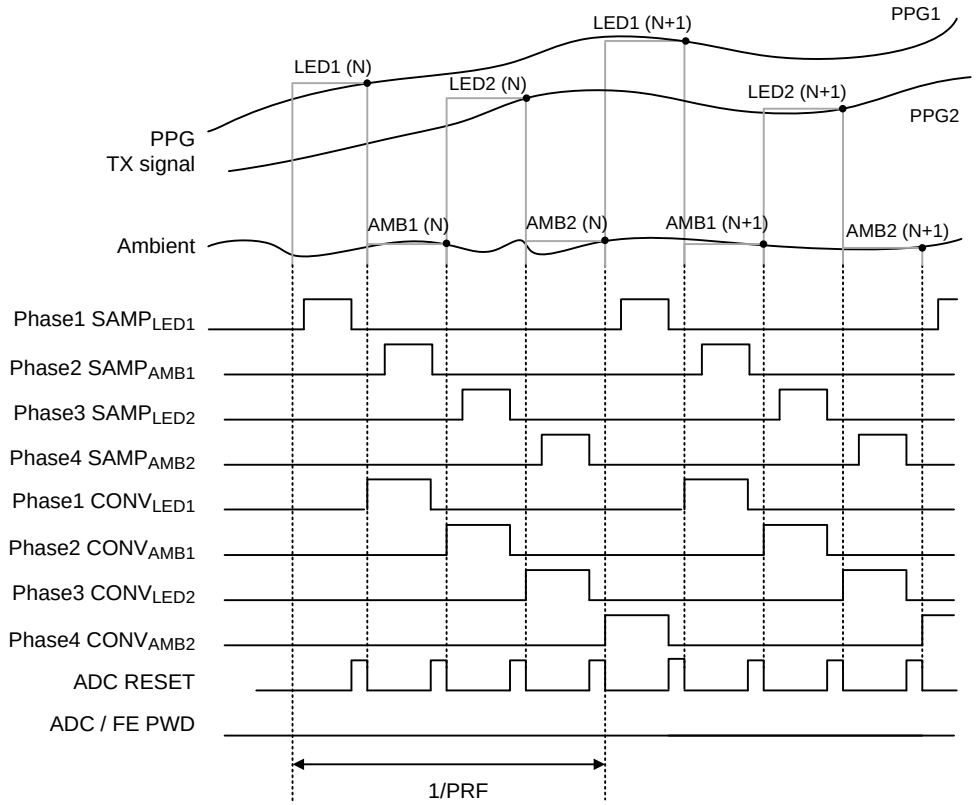
$$PPG\ (mV) = PPGADC\ Outputcode \times LSB \times 1000 = PPGADC\ Outputcode \times \frac{3.2V}{2^{16}} \times 1000$$

The PPG control logic (timing module) can adjust the sampling rate (Equation 5) and duty cycle (Equation 6) of the LED currents and also power down the AFE when the LEDs are off. The output of the ambient cancellation amplifier is separated into LED1, AMB1, LED2, AMB2 channels. When LED2 is on, the amplifier output is filtered and sampled on capacitor CLED2. Similarly, the LED1 signal is sampled on the CLED1 capacitor when LED1 is ON. In between the LED2 and LED1 pulses, the idle amplifier output is sampled to estimate the ambient signal on capacitors CLED2_amb and CLED1_amb. The minimum supported RX sampling time is 50μs.

$$PRF\ (Sampling\ Rate, Hz) = \frac{1MHz}{(PRF + 1)} \times 64Hz\ to\ 4096Hz$$

$$Duty\ (\%) = \frac{LED\ On\ Time}{PRF \times 100} \times 1.5\%\ to\ 25\%$$

PPG Channel - General Operation : PRF = 64 to 4096 SPS and duty = 25%



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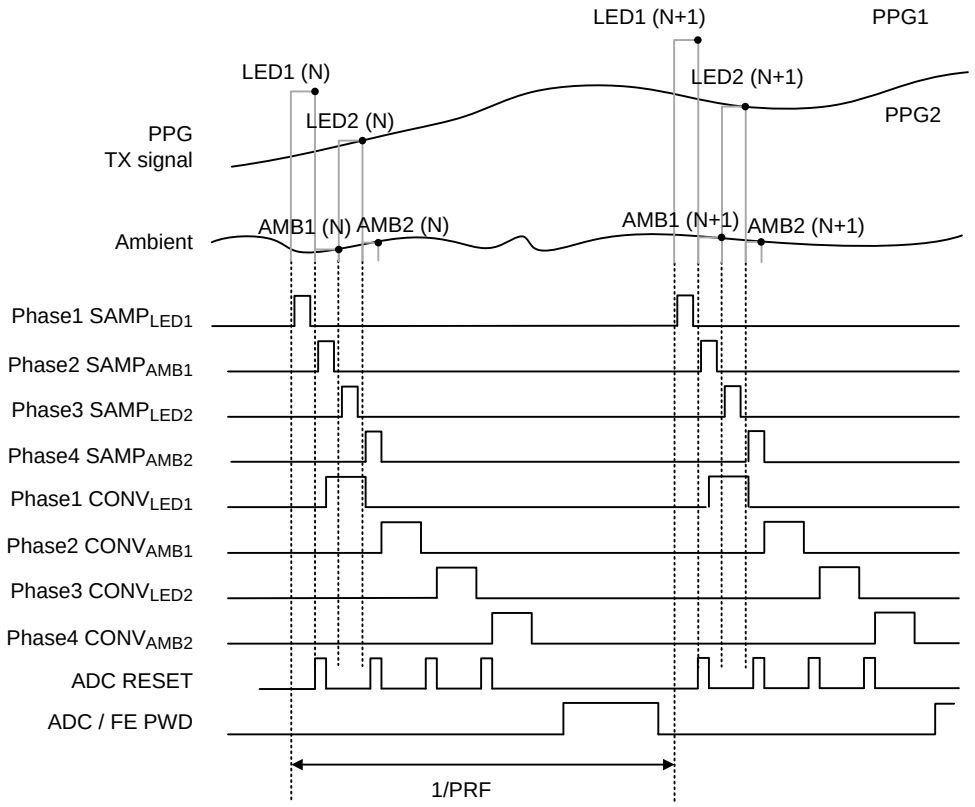
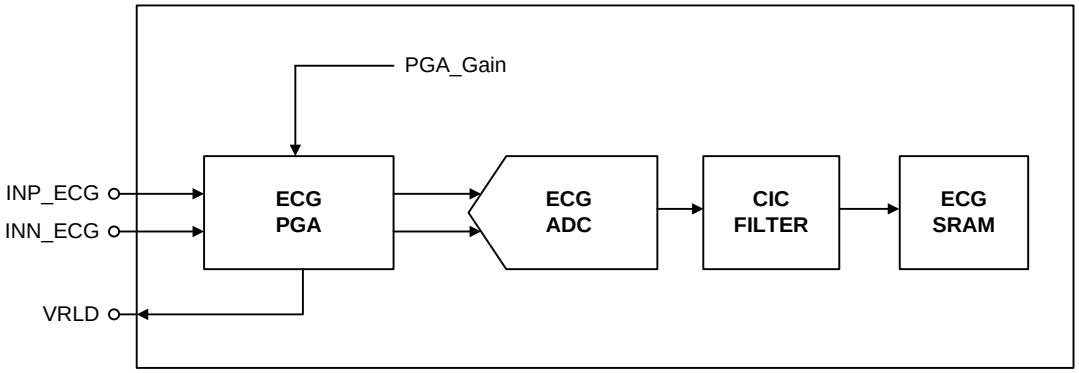
PPG Channel - Dynamic Power Down Mode : PRF = 64 to 4096 SPS and duty = 1.5 to 25%



ECG Channel

Below figure shows show the analog/digital parts of ECG system. The ECG channel supports two-electrode (2E) mode and right leg drive (RLD) mode, and acts as a buffer between human and circuit. It integrates a programmable gain amplifier (PGA), a right leg drive amplifier, and a 24-bit sigma-delta analog-to-digital converter (ADC) to sense and digitize the ECG signal. The PGA is a differential input/differential output, and has seven gain settings (1, 2, 3, 4, 6, 8, and 12). The sampling frequency of ECG ADC is adjustable from 64Hz to 4096Hz. There are two extra samples (data = 0) when doing first time sample ECG.



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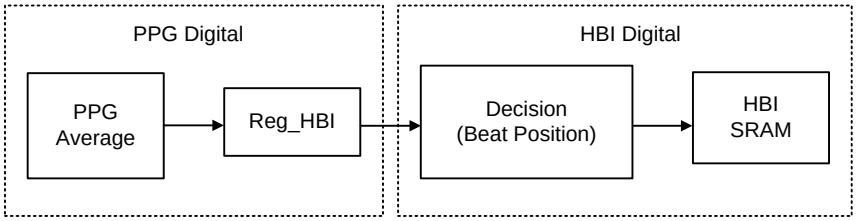
The ECG channel outputs 24 bits of data per channel in binary twos complement format, MSB first. Bit [23] is sign bit. A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. All 24 bits toggle when the analog input is at positive or negative full-scale.

$$\text{ECG (mV)} = \frac{\text{ECGACD Outputcode} \times \text{LSB} \times 1000}{\text{ECG Gain}} = \frac{\text{ECGACD Outputcode} \times \frac{4V}{2^{23}} \times 1000}{\text{ECG Gain}}$$

Heartbeat Interval (HBI) Estimation

The RT1025 has a built-in heartbeat interval (HBI) detector to reduce power consumption of hear-beat detection. When the signal quality of PPG is good enough, the BI detector is able to approximate wavelength of major tone. Instead of complete PPG signals, only beat time intervals are recorded in SRAM. The MCU is freed from estimating heart rate; as a result the amount of data read from the RT1025 SRAM via I^2C/SPI is reduced significantly.



Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-41B 3.10x3.48 (BS) package, the thermal resistance, θ_{JA}, is 3.75°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (3.75°C/W) = 26.6W for a WL-CSP-41B 3.10x3.48 (BS) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

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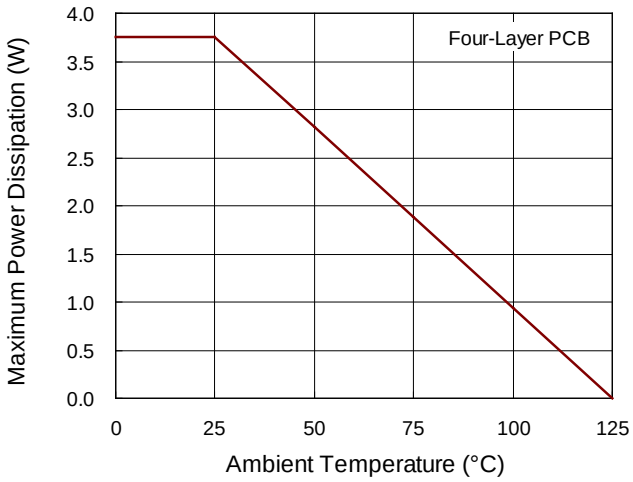

Figure 1. Derating Curve of Maximum Power Dissipation

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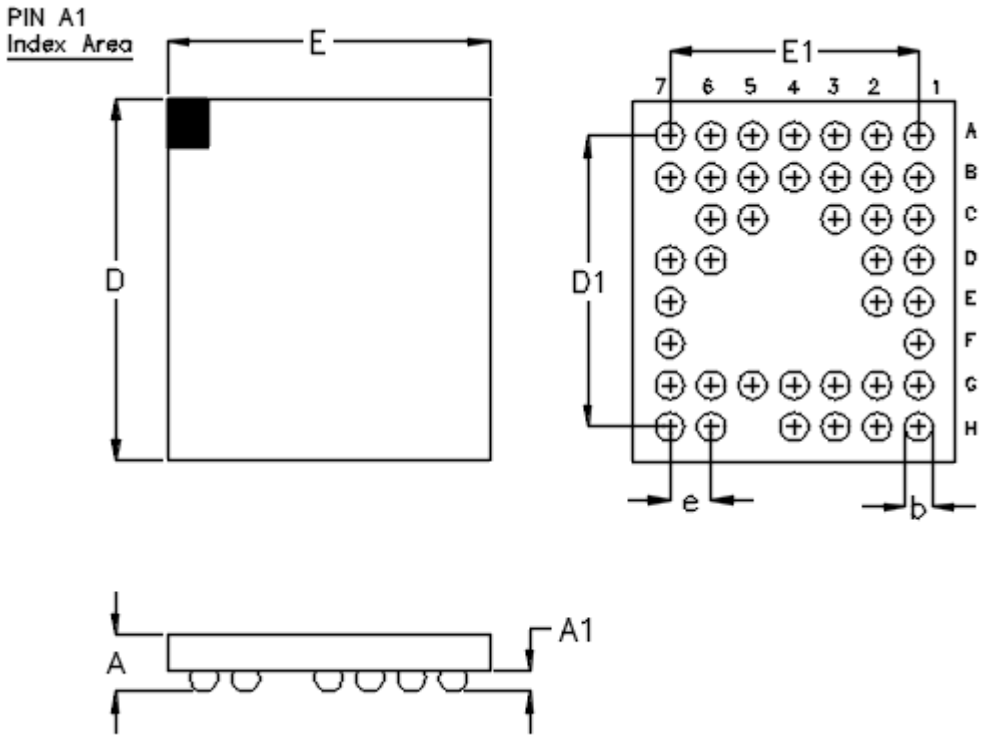
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.490	0.570	0.019	0.022
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	3.431	3.511	0.135	0.138
D1	2.800		0.110	
E	3.048	3.128	0.120	0.123
E1	2.400		0.094	
e	0.400		0.016	

41B WL-CSP 3.10x3.48 Package

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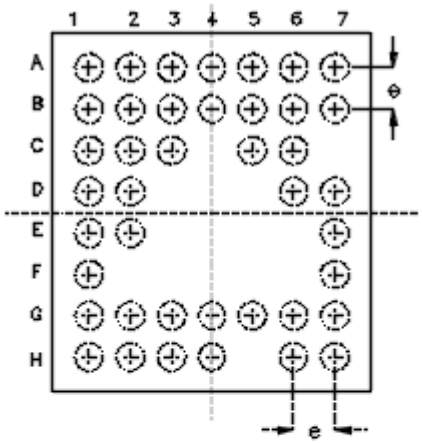
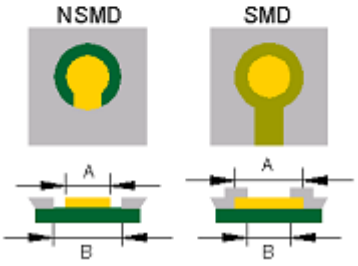
Footprint Information





Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP3.10x3.48-24	41	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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