36V, 4-Switch Bidirectional Buck-Boost Controller with I²C Interface

General Description

The RT6190 is a 4-switch bidirectional Buck-Boost controller designed for USB power delivery (USB PD). It operates with wide input voltage range from 4.5V to 36V, and the output voltage can be programmable between 3V and 36V. The RT6190 implements peak current mode control mechanism with the programmable constant voltage (CV) and constant current (CC) output to support USB-PD 3.0 SPR mode and 3.1 EPR mode. It also has built-in charge pumps for driving external low-cost N-MOSFETs to control the power path. With an I²C compatible interface, the RT6190 supports many programmable functions including CV/CC output, switching frequency, and cable voltage drop compensation. Moreover, the RT6190 integrates fully protection such as input UVLO, over/under voltage protection, cycle-by-cycle current limit, short protection, and over-temperature protection. The RT6190 is available in a WQFN-40L 5x5 package.

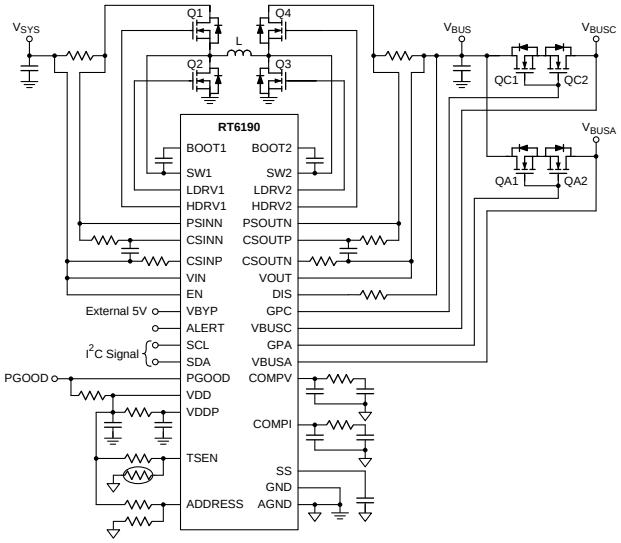
Applications

- Monitor
- USB Power Delivery
- Power Bank
-

Features

- **Support USB-PD 3.0 SPR Mode and 3.1 EPR Mode**
- **Integrated Buck-Boost Controller :**
  - **Wide Input Voltage Range : 4.5V to 36V**
  - **Wide Output Voltage Range : 3V to 36V**
  - **Peak Current Mode Control**
  - **Programmable Switching Frequency (250kHz to 1MHz)**
  - **Power Saving Mode Enables Higher Light Load Efficiency**
- **AnyPower™ for Constant Voltage (12.5mV/step, Typ.) and Constant Current (in 9-Bit Resolution) Output Settings**
- **Bi-directional Power Delivery for Forward Operation and Reverse Operation**
- **Embedded 2nd OCP Function**
- **I²C Compatible Interface**
- **Adjustable Soft-Start Time**
- **Programmable Cable Voltage Drop Compensation**
- **Built-in Bleeders for Quick VBUS Discharge**
- **Power Good Indicator**
- **Fully Protection with UVLO, OVP, UVP, OCP, Cycle-by-Cycle Current Limit and OTP**
- **WQFN-40L 5x5 Package**

Simplified Application Circuit



Ordering Information

RT6190 (□) □□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Protection Type
  None : Latch Mode
  H : Hiccup Mode

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT6190GQW

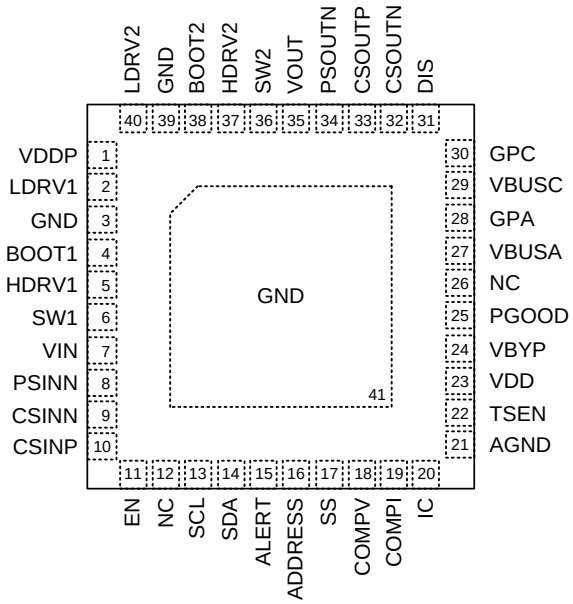
RT6190GQW : Product Number
YMDNN : Date Code

RT6190HGQW

RT6190HGQW : Product Number
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



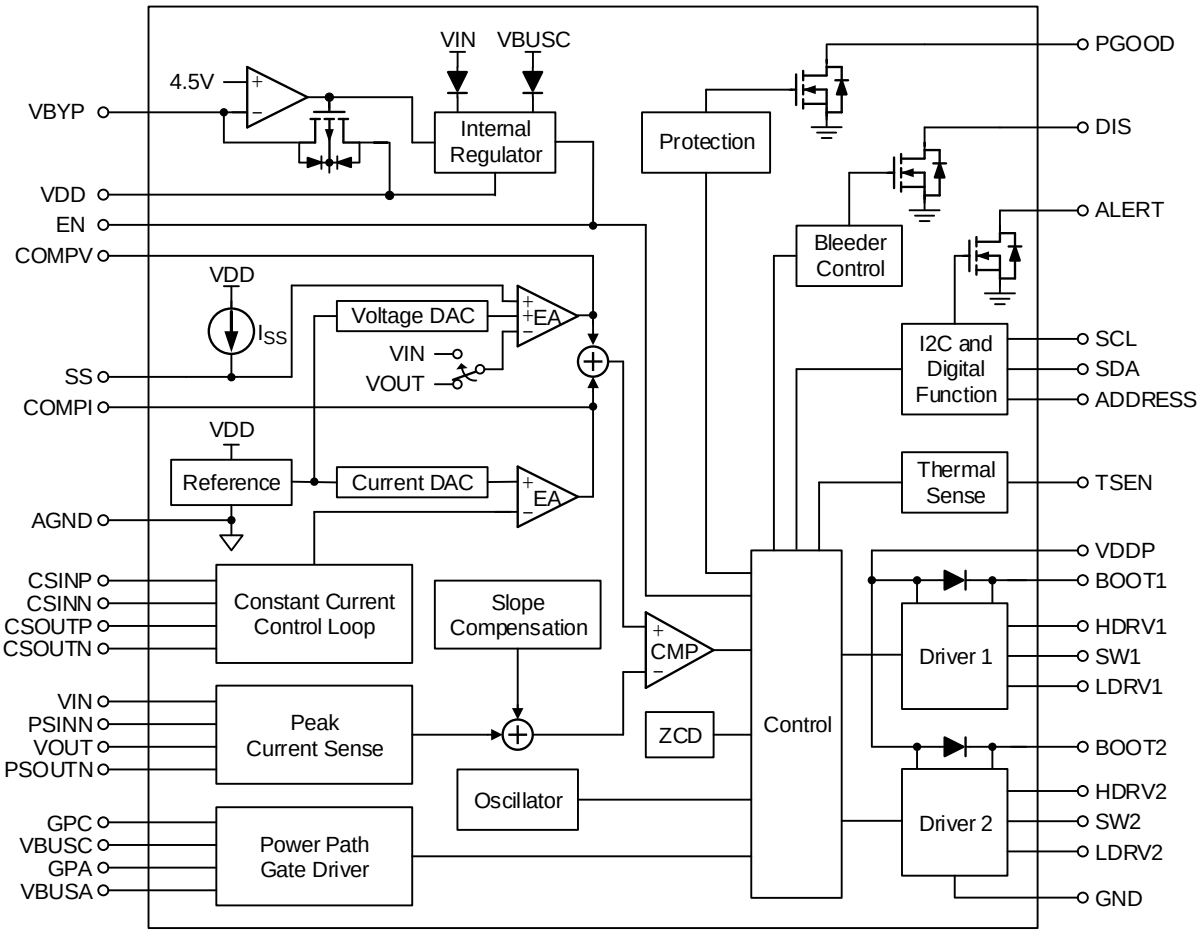
WQFN-40L 5x5

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDDP	Bias voltage input pin for internal gate drivers. It is recommended to connect an external 4.7μF capacitor from this pin to GND.
2	LDRV1	Buck mode low-side gate driver output for Q2. Connect to gate of low-side N-MOSFET Q2.
3, 39, 41 (Exposed Pad)	GND	Ground. Exposed pad. The exposed pad must be soldered to a large PCB copper area for maximum power dissipation.
4	BOOT1	Buck mode bootstrap supply for high-side N-MOSFET Q1. It is recommended to connect a 0.1μF capacitor from this pin to SW1 pin. The bootstrap diode is integrated internally between VDDP pin and this pin.
5	HDRV1	Buck mode high-side gate driver output for Q1. Connect to gate of high-side N-MOSFET Q1.
6	SW1	Buck mode switch node. Connect to power inductor.
7	VIN	Supply voltage input. Input peak current sense positive input. Connect to the current sense resistor R29 for input peak current sense in Forward operation.
8	PSINN	Input peak current sense negative input. Connect to the current sense resistor R29 for input peak current sense in Forward operation.
9	CSINN	Current sense negative input for input constant current control in Forward operation. Current sense positive input for output constant current control in Reverse operation. Connect to the current sense resistor R29 directly. It is recommended to use 10mΩ for the current sense resistor R29.
10	CSINP	Current sense positive input for input constant current control in Forward operation. Current sense negative input for output constant current control in Reverse operation. Connect to the current sense resistor R29 directly. It is recommended to use 10mΩ for the current sense resistor R29.
11	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode. "Do Not" leave this pin floating.
12, 26	NC	No internal connection. Please keep these pins floating.
13	SCL	Clock input for I^2C interface. Connect this pin to AGND if I^2C interface is not used. "Do Not" leave this pin floating.
14	SDA	Data line for I^2C interface. Connect this pin to AGND if I^2C interface is not used. "Do Not" leave this pin floating.
15	ALERT	Active low open-drain output. Connect this pin to 1.8V or 3.3V for normal operation. It will be pulled low if this chip is under the conditions of protection, EN shutdown, or after soft-start end.
16	ADDRESS	I^2C slave address selection pin. Connect this pin to VDD selects 0x2D, and connect this pin to AGND selects 0x2C.
17	SS	Soft-start time control pin. Connect a capacitor between this pin and AGND to set the soft-start time.
18	COMPV	Constant voltage (CV) loop compensation. Connect an external RC network from this pin to AGND for CV loop compensation. "Do Not" leave this pin floating.
19	COMPI	Constant current (CC) loop compensation. Connect an external RC network from this pin to AGND for CC loop compensation. "Do Not" leave this pin floating.

Pin No.	Pin Name	Pin Function
20	IC	Internal connection. Connect this pin to AGND.
21	AGND	Analog ground.
22	TSEN	Thermal sense input. This pin is used for external over-temperature protection via an external NTC network circuit. Connect this pin to VDD if thermal sense function is not used. “Do Not” leave this pin floating.
23	VDD	Internal LDO output. It is recommended to connect an external 4.7μF capacitor from this pin to GND. This pin is also used for internal analog circuit.
24	VBYP	Optional supply input from external 5V. Connect to external 5V voltage for VDD to increase converter efficiency.
25	PGOOD	Power good indicator open-drain output. This pin is pulled high when the output voltage is within the target range. It will be pulled to ground if this chip is under the conditions of protection, EN shutdown, or during soft-start.
27	VBUSA	Voltage sense input for monitoring VBUSA OVP and UVP.
28	GPA	Charge-pump gate driver output for VBUSA. This pin drives external power N-MOSFETs to turn on or off the power path between V_{OUT} and V_{VBUSA}.
29	VBUSC	Voltage sense input for monitoring VBUSC OVP and UVP.
30	GPC	Charge-pump gate driver output for VBUSC. This pin drives external power N-MOSFETs to turn on or off the power path between V_{OUT} and V_{VBUSC}.
31	DIS	Input pin for output discharge. Connect an external resistor between this pin and converter output to discharge energy of output capacitors through internal pull-low N-MOSFET.
32	CSOUTN	Current sense negative input for output constant current control in Forward operation. Current sense positive input for input constant current control in Reverse operation. Connect to the current sense resistor R30 directly. It is recommended to use 10mΩ for the current sense resistor R30.
33	CSOUTP	Current sense positive input for output constant current control in Forward operation. Current sense negative input for input constant current control in Reverse operation. Connect to the current sense resistor R30 directly. It is recommended to use 10mΩ for the current sense resistor R30.
34	PSOUTN	Input peak current sense negative input. Connect to the current sense resistor R30 for input peak current sense in Reverse operation.
35	VOUT	Voltage sense input for monitoring VOUT OVP and UVP. Input peak current sense positive input. Connect to the current sense resistor R30 for input peak current sense in Reverse operation.
36	SW2	Boost mode switch node. Connect to power inductor.
37	HDRV2	Boost mode high-side gate driver output for Q4. Connect to gate of high-side N-MOSFET Q4.
38	BOOT2	Boost mode bootstrap supply for high-side N-MOSFET Q4. It is recommended to connect a 0.1μF capacitor from this pin to SW1 pin. The bootstrap diode is integrated internally between VDDP pin and this pin.
40	LDRV2	Boost mode low-side gate driver output for Q3. Connect to gate of low-side N-MOSFET Q3.

Functional Block Diagram



Operation

The RT6190 is a 4-switch Buck-Boost controller to support USB-PD 3.0 SPR mode and 3.1 EPR mode. The input voltage range is from 4.5V to 36V, and the output range is from 3V to 36V. The RT6190 utilizes peak current mode control to obtain fixed switching frequency from 250kHz to 1MHz. This control topology is also used for constant voltage (AnyVolt^{TM}) regulation and constant current (AnyCurrent^{TM}) regulation. The RT6190 also provides DVS function to set the output voltage dynamically with different rising and falling slew rate. By status change detected function, the host can quickly and easily understand what a warning or fault events have occurred from external ALERT pin of RT6190.

The RT6190 integrates an internal gate driver to control external power path MOSFETs for USB-C and USB-A (1C1A) VBUS terminals in Forward operation when V_{BUS} = 5V. The RT6190 also provides the flexibility for using N-MOSFETs or P-MOSFETs as external power path MOSFETs. With the cable voltage drop compensated function, the output voltage can be adjusted in heavy load condition for different equivalent series resistance (ESR) of USB cables.

The RT6190 implements fully protection including input under-voltage lockout (UVLO), input and output over/under-voltage protection (OVP/UVP), output over current protection (OCP), input cycle-by-cycle peak/average current limit and OTP. It is recommended to use 10mΩ/1206 with 1W power dissipation as current sense resister for over current condition.

UVLO, Enable Control and Soft-Start

The RT6190 implements under-voltage lockout (UVLO) protection to prevent insufficient input voltage by monitoring VIN, VOUT, VDD and VDDP pins (VIN for Forward operation and VOUT for Reverse operation). When the input voltage of these pins are lower than UVLO threshold, IC stops switching and resets all digital functions.

The RT6190 provides an EN pin to enable or disable the device externally. When EN pin voltage falls below a logic-low threshold voltage (V_{ENL}), the RT6190 will enter to shutdown mode and reset all digital functions even if the input voltage of relative pins are above each UVLO threshold (V_{UVLO}). In shutdown mode, the supply current can be reduced to I_{SHDN} (typically 15μA). Once the EN pin voltage rises above a logic-high threshold voltage (V_{ENH}) and VIN/VOUT (VIN for Forward operation and VOUT for Reverse operation) is higher than its UVLO threshold, the VDD pin voltage will be regulated at 5V for internal digital circuits and VDDP for internal MOSFET gate drivers. After VDD and VDDP are higher than UVLO threshold voltage, the VOUT/VIN (VOUT for Forward operation and VIN for Reverse operation) starts to ramp up with 50μs (typ.) delay time. In addition, EN pin can be connected to VIN or VOUT pins directly to save power rail of system for Forward or Reverse operation.

The RT6190 provides adjustable soft-start function by connecting a capacitor from SS pin to AGND to prevent large inrush current during start-up. The soft-start time can be calculated as below equation :

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.9V}{I_{SS}(\mu A)}$$

Figure 1 shows the start-up sequence with enable control by software in Forward operation. When VIN is above UVLO threshold voltage and EN is higher than a logic-high threshold voltage, internal digital circuit will be enabled after VDD and VDDP rise above each UVLO threshold. If software EN (0x0E[7]) changes to “1”, the VOUT starts to ramp up when SS voltage is higher than 0.7V. After SS voltage reaches to 2.3V, PGOOD will change to high level with 512μs (typ.) delay time.

For power-off condition, RT6190 can be disabled by internal software EN (0x0E[7]) and external EN pin. When RT6190 is disabled by software, the discharge resistor can be controlled to on or off by register 0x0E[4]. Once the RT6190 is disabled by external EN pin, the output voltage will ramp down with default discharge resistor on. In both software and hardware disabled operation, PGOOD will go low after 16us (typ.) delay time after SS pin voltage is pulled low by internal discharging current. The power-off sequence of Forward operation is shown in Figure 2 and Figure 3.

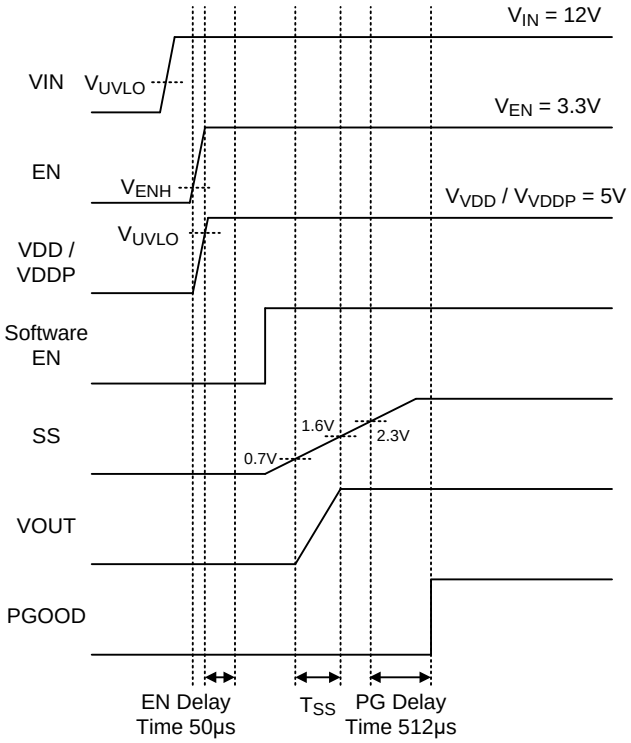


Figure 1. Start-up Sequence by Software in Forward Operation

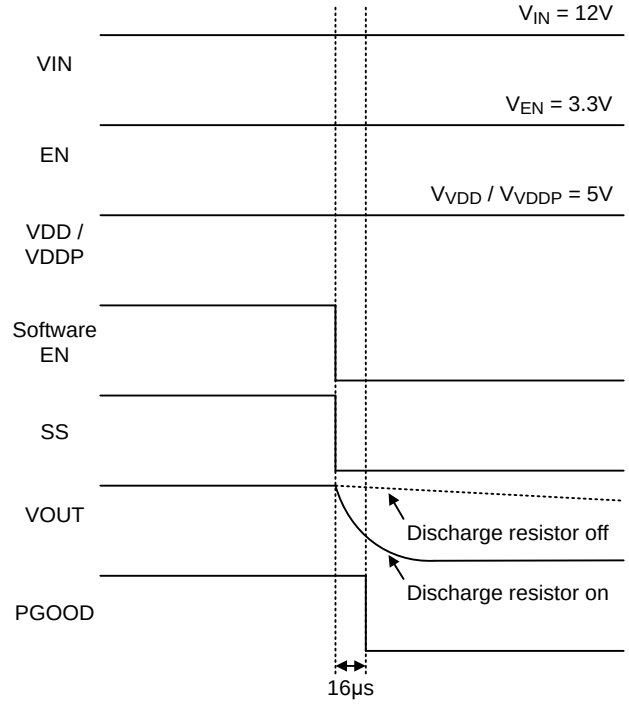


Figure 2. Power-off Sequence by Software in Forward Operation

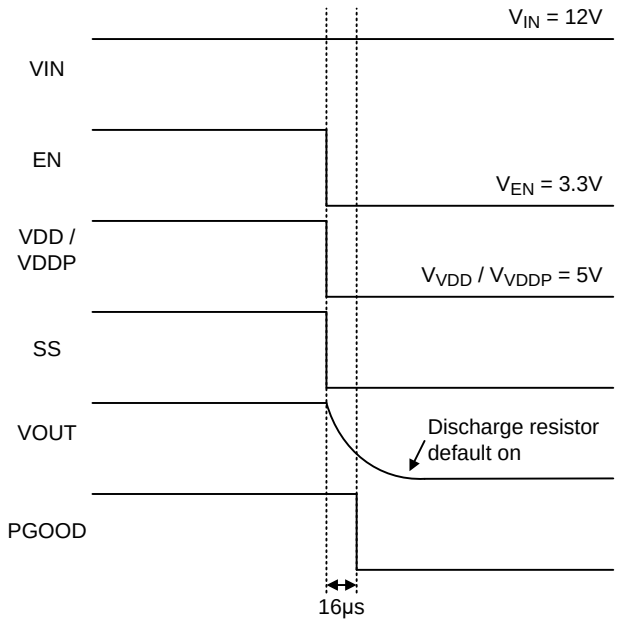


Figure 3. Power-off Sequence by external EN Pin in Forward Operation

Dynamic Voltage Scaling (DVS)

The RT6190 provides DVS function with wild voltage range for setting output voltage dynamically. Based on voltage ratio setting of register 0x11[5], output voltage can be set with different resolution by using register 0x01 and 0x02. The RT6190 also support DVS rising and falling slew rate selection by using register 0x0D[6:3], the default factory setting of 0x0D[6:3] is "1111" for DVS rising and falling slew rate = ΔVOUT / 32µs.

The ALERT_PG bit, 0x1F[6], will change to "1" when the output voltage reaches to target voltage, and then external ALERT pin will go low immediately. The RT6190 also support Mask function by register 0x21[6] to make external ALERT pin not go low after DVS operation end. In addition, register 0x37[2] and 0x38[2] shows 275ms timeout indication if output voltage do not reach to target level within 275ms, and this mechanism also has Mask function by register 0x39[2].

AnyVolt™ Constant Voltage (CV) Regulation

The RT6190 utilizes peak current mode control topology as main control loop for output constant voltage (CV) regulation. The output voltage is used to compare with the internal reference voltage to obtain an error signal by sensing VOUT pin voltage. This error signal is

externally compensated on COMPV pin to compare with the inductor current sensed on the output current sense resistor. As the signal relative inductor current falls below the compensated error signal in Forward operation, the HDRV1 or LDRV2 will be turned on with a time interval to make inductor current ramp up. As the inductor current reaches to peak current threshold (0x09[5:0]), the HDRV1 or LDRV2 turned off and LDRV1/HDRV2 will be turned on until an internal oscillator initializing next switching cycle.

AnyCurrent™ Constant Current (CC) Regulation

The RT6190 also implements average current control loop by sensing the voltage across output current sense resistor R30 and R29 (R30 for Forward operation and R29 for Reverse operation) for output constant current (CC) regulation. The voltage across output current sense resistor is used to compare with the output CC level as register 0x03/0x04 to obtain an error signal, and then this error signal is externally compensated on COMPI pin. When the voltage across output current sense resistor is higher than output CC level, the COMPI pin voltage will fall below COMPV pin voltage to limit and keep the output current as output CC level. As the output current becomes higher than output CC level, RT6190 will limit the output current and then output voltage will lower than regulation point until UVP happened. In addition, it is recommended to use 10mΩ/1206 with 1W power dissipation as current sense resister for correct operation.

Mode Selection

The RT6190 provides operation mode selection for light load Power Saving Mode (PSM) and Forced-CCM Mode (FCCM) by using register 0x0D[7]. The default factory setting of operation mode is light load PSM.

Power Saving Mode

When 0x0D[7] = 0, RT6190 operates in PSM and automatically reduces switching frequency at light-load conditions to maintain high efficiency. The internal zero current detection (ZCD) circuitry will be enabled to sense the inductor current by utilizing $R_{DS(ON)}$ of the Q4 N-MOSFET in typical application circuit. As the inductor current drops to zero and becomes negative, both HDRVx and LDRVx are turned off with the output capacitor supplying the load current until the output voltage falls below the internal reference voltage. In reverse, when the output current increases from light load to heavy load, the switching frequency will increase to 250kHz (default factory setting) as the inductor current reaches the continuous conduction condition.

FCCM Mode

When 0x0D[7] = 1, the internal ZCD circuitry is disabled and the RT6190 operates in FCCM with typically 250kHz (default factory setting) at any load condition. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

ADC Reporting

The RT6190 provides ADC function to report input/output voltage and current, VBUSC voltage and TSEN pin voltage by utilizing register 0x12 to 0x1B and 0x33 to 0x34 with 11-bit resolution. Register 0x10[1] and 0x32[1] are the enable control bit for ADC function, and 0x10[7:6] is the average times of ADC function. The default factory setting of 0x10 is 82h and 0x32 is 00h for ADC function default enable with average 8 times except VBUSC voltage reporting. Please see the I^2C register map for detail description of register 0x12 to 0x1B.

Power Path Control

The RT6190 integrates an internal gate driver to control external power path MOSFETs for USB-C and USB-A (1C1A) VBUS terminals in Forward operation when V_{BUS} = 5V. The GPC/VBUSC pins are used for USB-C terminal, and GPA/VBUSA pins are used for USB-A terminal. Register 0x29[3:2] selects the external MOSFETs type of N-MOSFETs and P-MOSFETs for USB-C and USB-A terminals, and register 0x29[1:0] are the enable control bit for each power path MOSFETs. All power path MOSFETs will be turned off when protection happened with the default factory setting of register 0x29[7:4], and it can be set after internal digital circuit enabled for different application. For Reverse operation, OVP/UVP of VBUSC/A need to be disabled

for correct operation. In addition, the default factory setting of register 0x29[1:0] is 00 for power path function not used.

Cable Voltage Drop Compensation

The RT6190 implements cable voltage drop compensation to adjust the output voltage in heavy load condition for different equivalent series resistance (ESR) of USB cables. Register 0x0E[2:0] can set different compensation, and the default factory setting of 0x0E[2:0] is 000 for cable voltage drop compensation function default disabled.

Power Good Indication

The RT6190 provides a power good indication with open-drain output capability to show the output voltage status. When output voltage is between 90% and 120% (typically OVP trip threshold of default factory setting) of reference voltage, the external PGOOD pin keeps as high level and internal PGOOD bit changes to “1” in register 0x1D[6] and 0x1F[6]. Register 0x1F[6] also shows the output voltage status for DVS operation, 0x1F[6] will change to “1” if the output voltage reaches to the target voltage whether in DVS up or down operation.

External Thermal Sense

The RT6190 provides an external thermal sense function to sense the temperature of external components such as inductor or MOSFETs by connecting a negative temperature coefficient (NTC) thermistor from TSEN pin to AGND and a resistor from VDD to TSEN pin. Register 0x1A/0x1B can report the TSEN pin voltage from 0V to 2V with 1mV resolution while ADC function is enabled (0x10[1] = 1).

Spread-Spectrum Operation

Due to periodicity of the switching signals, the energy concentrates in one particular frequency and in its harmonics. These levels of energy will be radiated to induce potential EMI issues. The RT6190 provides spread-spectrum function by register 0x11[7] for simplifying in compliance with the CISPR and EMI requirements.

After the soft-start end, the spread-spectrum can be enabled with a pseudo random sequence and used +8% spread of the switching frequency.

Timer1 and Watchdog Function

The RT6190 implements a Timer1 function to detect Host status if system hang occurred without any protection be detected. Register 0x30[6:4] selects different Timer1 timeout, and the default factory setting value of 0x30[6:4] is 000 for Timer1 disabled. Timer1 will begin to count if 0x30[6:4] ≠ 000, and ALERT pin keeps high level if Timer1 is still counting. After Timer1 timeout completed, external ALERT pin will go to low level.

The RT6190 also implements a watchdog function to reset IC to factory default setting after watchdog timeout completed if ALERT pin keeps as low level. Register 0x30[2:0] selects different watchdog timeout, and the default factory setting value of 0x30[2:0] is 000 for watchdog disabled.

Status Change Detection and ALERT Pin

The RT6190 implements a status change detection to alert the host when a warning or fault events have occurred by using external ALERT pin with push-pull output capability for active low behavior. The warning events are input UVLO, Timer1 and PGOOD, and the fault events are the conditions of over-voltage, under-voltage, over-current and over-temperature. In addition, PGOOD event indicates output voltage status for normal and DVS operation.

Register 0x1C, 0x1D, 0x1E and 0x1F can help host to know what the warning of fault events happened. 0x1C and 0x1D will be cleared to default setting “0” if the event is removed, but 0x1E and 0x1F will be cleared to default setting “0” by writing this bit to "1" after the events removed only. The RT6190 also supports mask function to mask or pass the internal event flag output to external ALERT pin by using 0x20, and 0x21 registers. The overall detection function is shown in Figure 4.

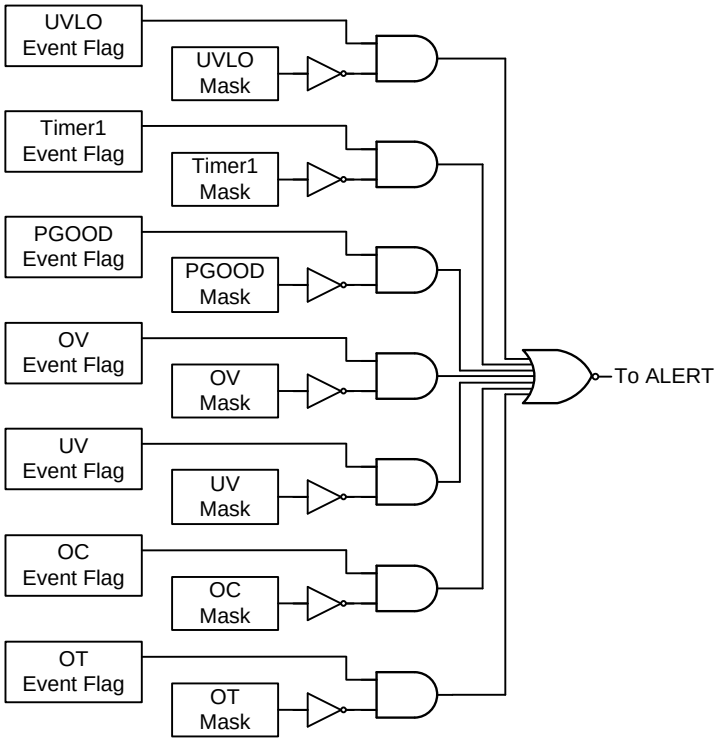


Figure 4. Overall Detection Function Block Diagram

Protection

The RT6190 implements fully protective mechanism including over/under-voltage protection (OVP/UVP) for each VOUT/VBUSC/VBUSA pin, output over-current protection (OCP), input cycle-by-cycle peak/average current limit, over-temperature protection (OTP) and input OVP/UVP. The protection type of RT6190 is latched-off operation, and RT6190H is hiccup operation. Besides, RT6190 also provide pin-short protection to prevent IC damaged in smoke, fire or spark conditions.

Output Over-Voltage Protection (OVP)

The RT6190 provides output over-voltage protection (OVP) by constantly monitoring output voltage (VOUT/VBUSC/VBUSA pins for Forward operation, VIN pin for Reverse operation). If VOUT/VIN is larger than the OVP trip threshold (typically 120%) with relative OVP delay time, HDRVx will stop switching and LDRVx will fully turn on to discharge energy of the inductor immediately until ZCD triggered. When VBUSC/VBUSA OVP triggered in Forward operation, GPC/GPA will turn off but HDRVx/LDRVx will keep original state. In addition, the default factory setting of VBUSC/VBUSA OVP is disabled for correct operation if power path is not used or in Reverse operation. Register 0x0B[5:0] can select different OVP trip threshold and OVP delay time, and OVP trip threshold can also be adjustable by register 0x2B[4] and 0x36.

In latched-off operation, RT6190 will return to normal operating unless resetting IC by 0x0E[7] after OVP happened. For hiccup behavior, RT6190H will return to last state before OVP happened and the output voltage will back to regulation point after OVP released.

Output Under-Voltage Protection (UVP)

The RT6190 provides output under-voltage protection (UVP) against over-load or short-circuit condition by constantly monitoring output voltage (VOUT / VBUSC / VBUSA pins for Forward operation, VIN pin for Reverse operation). If VOUT/VIN drop below the UVP trip threshold (typically 70%) with relative UVP delay time, HDRVx will stop switching and LDRVx will fully turn on to discharge energy of the inductor immediately until ZCD triggered. When VBUSC/VBUSA UVP triggered in Forward operation, GPC/GPA will turn off but HDRVx/LDRVx will keep original state. In addition, the default factory setting of VBUSC/VBUSA UVP is disabled for correct operation if power path is not used or in Reverse operation. Register 0x0C[5:0] can select different UVP trip threshold and UVP delay time, and

UVP trip threshold can also be adjustable by register 0x2B[5] and 0x35.

In latched-off operation, RT6190 will return to normal operating unless resetting IC by 0x0E[7] after UVP happened. For hiccup behavior, both HDRVx and LDRVx of RT6190H will keep low state in 65ms and then IC starts to switch. If the output voltage is not greater than UVP trip threshold after internal soft-start end signal triggered, both HDRVx and LDRVx will still keep low state again for next cycle.

Output Over-Current Protection (OCP) and Input Peak/Average Current Limit

The RT6190 provides over-current protection (OCP) and cycle-by-cycle current limit to prevent IC from the catastrophic damage in output short-circuit, over-current or inductor saturation conditions. For OCP function, RT6190 monitors the voltage across output current sense resistor (R30 for Forward operation, R29 for Reverse operation) for OCP1/OCP2/OCP3 detection, and R30/R29 for OCP4 detection. If OCPx is triggered with relative OCP delay time, HDRVx will stop switching and LDRVx will fully turn on to discharge energy of the inductor immediately until ZCD triggered. Register 0x22 to 0x27 and 0x28[3:0] can select OCP trip threshold and delay time, and 0x28[7:4] are the control bits for OCPx enable. It is recommended to use the same current sense gain of input and output for correct OCP4 function.

In latched-off operation, RT6190 will return to normal operating unless resetting IC by 0x0E[7] after OCPx happened. For hiccup behavior, RT6190H will return to last state before OCPx happened and the output voltage will back to regulation point after OCPx released.

The RT6190 also monitors the voltage across input current sense resistor (R29 for Forward operation, R30 for Reverse operation) for cycle-by-cycle peak and average current limit function. When peak or average current limit is triggered, RT6190 will limit the output current and then output voltage will lower than regulation point until UVP happened. Register 0x0A can set input peak current limit threshold, and register 0x06/0x07 can set input average current limit threshold.

Input Over/Under-Voltage Protection (OVP/UVP)

The RT6190 also provides OVP and UVP by constantly monitoring input voltage (VIN pin for Forward operation, VOUT pin for Reverse operation). Register 0x0C[7] is used to enable or disable input OVP, and the default factory setting of input OVP is disabled. If input voltage is larger than OVP trip threshold (default factory setting is 27V), HDRVx will stop switching and LDRVx will fully turn on to discharge energy of the inductor immediately until ZCD triggered.

In addition, register 0x05 can be used to set minimum input voltage level in FCCM operation. When the input voltage is lower than minimum input voltage level, COMPV will be pulled low to make output voltage be lower than regulation point until output UVP is triggered.

Output Over-Temperature Protection (OTP)

The RT6190 includes an over-temperature protection (OTP) circuitry to prevent overheating condition. When junction temperature exceeds a thermal shutdown threshold T_{SD} with latched-off operation, the RT6190 will stop switching and resume normal operation unless resetting IC by 0x0E[7] after the junction temperature is lower than thermal shutdown hysteresis (ΔT_{SD}). For hiccup operation, the RT6190H resumes normal operation immediately once the junction temperature cools down by ΔT_{SD}.

Pin-Short Protection

The RT1690 provides pin-short protection for neighbor pins. The internal protection circuitry will be enabled to prevent IC in smoke, fire and spark situations.

Absolute Maximum Ratings (Note 1)

- VIN, PSINN, CSINP, CSINN, VOUT, PSOUTN, CSOUTP, CSOUTN to GND ---------- –0.3V to 40V
- VIN to PSINN, CSINP to CSINN, VOUT to PSOUTN, CSOUTP to CSOUTN ---------- –5V to 5V
- EN, DIS, VBUSC, VBUSA to GND ---------- –0.3V to 40V
- GPC, GPA to GND ---------- –0.3V to 50V
- BOOT1 to SW1, BOOT2 to SW2 ---------- –0.3V to 6V
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –5V to 7.5V
- HDRV1 to SW1, HDRV2 to SW2
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –5V to 7.5V
- SW1, SW2 to GND
  - DC ---------- –0.3V to 40V
  - < 100ns ---------- –5V to 45V
- LDRV1, LDRV2 to GND
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –2.5V to 7.5V
- Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings

- ESD Susceptibility (Note 2)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 4.5V to 36V
- Output Voltage ---------- 3V to 36V
- VDDP Supply Voltage ---------- 4.5V to 5.5V
- VBYP Supply Voltage ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4)

- WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W
- WQFN-40L 5x5, $\theta_{JC(Top)}$ ---------- 6°C/W

Electrical Characteristics

(V_{VIN} = 12V, V_{VDD} = V_{VDDP} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input and Output Voltage Range						
Input Voltage Range	V_{INPUT}	V_{VIN} for Forward, V_{VBUSC} for Reverse	4.5	--	36	V
Output Voltage Range	V_{OUTPUT}	V_{VBUSC} for Forward, V_{VIN} for Reverse	3	--	36	V
Input UVLO Threshold	V_{UVLO}	V_{VIN} for Forward, V_{VOUT} for Reverse	2.7	3	3.4	V
Input UVLO Hysteresis	ΔV_{UVLO}	V_{VIN} for Forward, V_{VOUT} for Reverse	--	200	--	mV
VDD Supply Voltage and Enable						
VDD Output Voltage	V_{VDD}	I_{VDD} = 0 to 60mA, V_{VIN} or V_{VBUSC} = 12V	4.8	5	5.2	V
VDD Short-Circuit Current	I_{VDD_SC}		--	120	--	mA
VDD UVLO Threshold	V_{VDD_UVLO}	V_{VDD} rising	2.7	3	3.4	V
VDD UVLO Hysteresis	ΔV_{VDD_UVLO}		--	200	--	mV
VDDP UVLO Threshold	V_{VDDP_UVLO}	V_{VDDP} rising	3.7	4	4.3	V
VDDP UVLO Hysteresis	ΔV_{VDDP_UVLO}		--	200	--	mV
EN Threshold	V_{ENH}	EN rising	1.35	--	36	V
	V_{ENL}	EN falling	--	--	0.85	
VBYP Switchover Threshold		VBYP rising	--	4.5	--	V
		VBYP falling	--	230	--	mV
VBYP Switchover On-Resistance			--	3	--	Ω
VIN (Forward) and VBUSC (Reverse) Operating Current						
Input Current in Normal Mode	I_Q	EN = High. In PSM without switching. Forward operation	--	3	5	mA
	I_{Q_VBUSC}	EN = High. In PSM without switching. Reverse operation	--	3	5	
Input Current in Standby Mode	I_{SHDN}	EN = Low. Forward operation	--	15	30	μA
	I_{SHDN_VBUSC}	EN = Low. Reverse operation	--	35	45	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency						
Switching Frequency	f_{SW}	Programmable by 0x0D[2:0]	200	250	300	kHz
			260	325	390	
			320	400	480	
			400	500	600	
			492	615	738	
			584	730	876	
			676	845	1014	
			768	960	1152	
Soft-Start						
Soft-Start Charge Current	I_{SS}		5	6	7	μA
Constant-Voltage (CV) and Constant-Current (CC) Output Levels						
CSOUTP and CSOUTN Operating Voltage Range			3	--	36	V
CV Regulated Voltage Range at VOUT Pin	V_{REG_VOUT}	11-bit DAC, VOUT Ratio = 0.08V/V, 12.5mV/step	3	--	25.6	V
		11-bit DAC, VOUT Ratio = 0.05V/V, 20mV/step	3	--	36	
CV Regulated Voltage Accuracy at VOUT Pin		V_{REG_VOUT} = 5V/9V/12V/15V/20V	−1.5	--	1.5	%
CSOUTP to CSOUTN Built-in Offset Voltage		Forward for output current sense	--	1.5	--	mV
		Reverse for input current sense	--	4.5	--	
CSINP to CSINN Built-in Offset Voltage		Forward for input current sense	--	4.5	--	mV
		Reverse for output current sense	--	1.5	--	
Output CC Regulated Voltage Range	$V_{REF\_CC\_OUT}$	Forward, V_{CSOUTP} and V_{CSOUTN} > 3V, with GAIN_OCS = 10x, $\Delta V_{REF\_CC\_OUT}$ = 0.24mV/step, and R30 = 10mΩ for $I_{REF\_CC\_OUT}$ = 24mA/step	3	--	58	mV
		Reverse, V_{CSINP} and V_{CSINN} > 3V, with GAIN_OCS = 10x, $\Delta V_{REF\_CC\_OUT}$ = 0.24mV/step, and R29 = 10mΩ for $I_{REF\_CC\_OUT}$ = 24mA/step				

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output CC Regulated Voltage Accuracy		Forward, V_{CSOUTP} and V_{CSOUTN} > 3V, $V_{REF\_CC\_OUT}$ = 10mV/30mV/50mV, GAIN_OCS = 10x, R30 = 10mΩ	–1	--	1	mV
		Reverse, V_{CSINP} and V_{CSINN} > 3V, $V_{REF\_CC\_OUT}$ = 10mV/30mV/50mV, GAIN_OCS = 10x, R29 = 10mΩ	–2	--	2	
Input CC Regulated Voltage Range	$V_{REF\_CC\_IN}$	Forward, V_{CSINP} and V_{CSINN} > 3V, with GAIN_ICS = 10x, $\Delta V_{REF\_CC\_IN}$ = 0.24mV/step, and R29 = 10mΩ for $I_{REF\_CC\_IN}$ = 24mA/step	3	--	58	mV
		Reverse, V_{CSOUTP} and V_{CSOUTN} > 3V with GAIN_ICS = 10x, $\Delta V_{REF\_CC\_IN}$ = 0.24mV/step, and R30 = 10mΩ for $I_{REF\_CC\_IN}$ = 24mA/step				
Input CC Regulated Voltage Accuracy		Forward, V_{CSINP} and V_{CSINN} > 3V, $V_{REF\_CC\_IN}$ = 10mV/30mV/50mV, GAIN_ICS = 10x, R29 = 10mΩ	–3	--	3	mV
		Reverse, V_{CSOUTP} and V_{CSOUTN} > 3V, $V_{REF\_CC\_IN}$ = 10mV/30mV/50mV, GAIN_ICS = 10x, R30 = 10mΩ	–3	--	3	
Minimum Regulated Voltage Range at VIN Pin	V_{REG_VIN}	6-bit DAC, VIN Ratio = 0.08V/V, 350mV/step	4.55	--	22.05	V
		6-bit DAC, VIN Ratio = 0.05V/V, 560mV/step	7.28	--	35.28	
Constant-Voltage (CV) and Constant-Current (CC) Error Amplifiers						
Trans-conductance of COMPV Error Amplifier	Gmv	I_{COMPV} = ±20μA	382	550	718	μA/V
Maximum Sink/Source Current of COMPV Error Amplifier			--	54	--	μA
Trans-conductance of COMPI Error Amplifier	Gmi	I_{COMPI} = ±20μA	382	550	718	μA/V
Maximum Sink/Source Current of COMPI Error Amplifier			--	54	--	μA
On-Time Timer Control and ZCD						
Minimum On-Time	t_{ON_MIN}		--	200	230	ns
Minimum Off-Time	t_{OFF_MIN}		--	200	230	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Q4 ZCD Voltage Threshold	V_{ZCD}		--	4	--	mV
ZC Mask Time	t_{ZCD_Mask}		--	250	--	ns
Gate Drivers						
HDRV1/2 Pull-Up Resistance	R_{HDRVx_SRC}	$V_{BOOT1/2}$ - $V_{SW1/2}$ = 5V, $V_{BOOT1/2}$ - $V_{HDRV1/2}$ = 0.1V	--	1	--	Ω
HDRV1/2 Pull-Down Resistance	R_{HDRVx_SNK}	$V_{HDRV1/2}$ - $V_{SW1/2}$ = 0.1V	--	0.7	--	Ω
LDRV1/2 Pull-Up Resistance	R_{LDRVx_SRC}	V_{VDDP} - $V_{LDRV1/2}$ = 0.1V	--	2	--	Ω
LDRV1/2 Pull-Down Resistance	R_{LDRVx_SNK}	$V_{LDRV1/2}$ = 0.1V	--	0.4	--	Ω
Dead Time	t_{DT}	Programmable by 0x0F[7:6]	--	30	--	ns
			--	50	--	
			--	70	--	
			--	90	--	
SW1/2 Pull-Down Period for Charging Bootstrap Capacitor			--	250	--	ns
Operating Frequency of Internal Charge Pump for BOOT1/2			--	10	--	MHz
Protections : Over-Voltage, Under-Voltage, Over-Current and External Over-Temperature Protections (OVP, UVP, OCP, OTP)						
Input OVP Trip Threshold	V_{OVP_INPUT}	0x0C[7] = 1	--	27	--	V
Output OVP Trip Threshold	V_{OVP}	Programmable by 0x0B[1:0]	--	115	--	%
			--	120	--	
			--	125	--	
Output OVP Recovery Threshold	V_{OVP_R}	Hiccup mode of protection type	--	500	--	mV
Output OVP Delay Time at VBUSC and VBUSA Pins	t_{OVP_EXT}	Programmable by 0x0B[3:2]	--	8	--	µs
			--	16	--	
			--	32	--	
			--	64	--	
Output OVP Delay Time at VOUT Pin	t_{OVP_INT}	Programmable by 0x0B[5:4]	--	96	--	µs
			--	192	--	
			--	288	--	
			--	386	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output UVP Trip Threshold	V_{UVP}	Programmable by 0x0C[1:0]	--	50	--	%
			--	60	--	
			--	70	--	
			--	80	--	
Output UVP Recovery Threshold	V_{UVP_R}	Hiccup mode of protection type	--	500	--	mV
Output UVP Delay Time at VBUSC and VBUSA Pins	t_{UVP_EXT}	Programmable by 0x0C[3:2]	--	32	--	µs
			--	64	--	
			--	128	--	
			--	256	--	
Output UVP Delay Time at VOUT Pin	t_{UVP_INT}	Programmable by 0x0C[5:4]	--	256	--	µs
			--	512	--	
			--	768	--	
			--	1024	--	
Peak Current Protection	I_{POCP}	R29 = R30 = 10mΩ, 0x0A = 24h R29 for Forward, R30 for Reverse	--	13.2	--	A
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	25	--	
Power Good and DIS						
Power Good Threshold	V_{TH_PG}	V_{OUT} rising for % of V_{OUT}, PGOOD from low to high	--	90	--	%
	ΔV_{TH_PG}	V_{OUT} falling for % of V_{OUT}, PGOOD from high to low	--	5	--	
Power Good Output Low Voltage	V_{PG_L}	I_{SINK} = 1mA	--	--	0.4	V
Discharge Resistor at DIS Pin	R_{DIS}	V_{DIS} = 0.5V	--	6	--	Ω
ADC Reporting						
Input Voltage Reporting		V_{VIN} for Forward, V_{VOUT} for Reverse	–2.5	--	2.5	%
Output Voltage Reporting		V_{VOUT} or $V_{VIN} \leq$ 5V, V_{VOUT} for Forward, V_{VIN} for Reverse	–2.5	--	2.5	%
		V_{VOUT} or $V_{VIN} >$ 5V, V_{VOUT} for Forward, V_{VIN} for Reverse	–2	--	2	
VBUSC Voltage Reporting		V_{VBUSC} = 0.8V	–40	--	40	mV
		$V_{VBUSC} \geq$ 5V	–2	--	2	%
TSEN Voltage Reporting			–30	--	30	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input and Output Current Reporting		V_{CSINP} - V_{CSINN} = 40mV, V_{CSOUTP} - V_{CSOUTN} = 40mV	–2.5	--	2.5	%
		V_{CSINP} - V_{CSINN} = 20mV, V_{CSOUTP} - V_{CSOUTN} = 20mV	–4	--	4	
		V_{CSINP} - V_{CSINN} = 10mV, V_{CSOUTP} - V_{CSOUTN} = 10mV	–7	--	7	
		V_{CSINP} - V_{CSINN} = 5mV, V_{CSOUTP} - V_{CSOUTN} = 5mV	–15	--	15	
Charge-Pump Gate Drivers (GPC and GPA)						
Maximum GPC Voltage	V_{GPC}	V_{OUT} = 20V, $R_{GPC\text{-}to\text{-}GND}$ ≥ 2MΩ	V_{VBUSC} + 2 x V_{VDD} - 5V	V_{VBUSC} + 2 x V_{VDD} - 3V	V_{VBUSC} + 2 x V_{VDD} - 1V	V
Maximum GPA Voltage	V_{GPA}	V_{VBUSA} = 12V, $R_{GPA\text{-}to\text{-}GND}$ ≥ 2MΩ	V_{VBUSA} + 2 x V_{VDD} - 5V	V_{VBUSA} + 2 x V_{VDD} - 3V	V_{VBUSA} + 2 x V_{VDD} - 1V	V
On-Resistance of the GPC/A Pull-Low MOSFET			--	250	350	Ω
I^2C Interface (Note 6)						
SCL, SDA Input Voltage	V_{IH}	Rising	1.2	--	--	V
	V_{IL}	Falling	--	--	0.4	
SCL Clock Rate	f_{SCL}	Fast mode	--	400	--	kHz
		Fast plus mode	--	1	--	MHz
		High speed mode, load 100pF max.	--	--	3.4	MHz
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	Fast mode	0.6	--	--	µs
		Fast plus mode	0.26	--	--	
Low Period of the SCL Clock	t_{LOW}	Fast mode	1.3	--	--	µs
		Fast plus mode	0.5	--	--	
High Period of the SCL Clock	t_{HIGH}	Fast mode	0.6	--	--	µs
		Fast plus mode	0.26	--	--	
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	Fast mode	0.6	--	--	µs
		Fast plus mode	0.26	--	--	
Data Hold Time	$t_{HD;DAT}$	Fast mode	0	--	--	µs
		Fast plus mode	0	--	--	
Data Set-Up Time	$t_{SU;DAT}$	Fast mode	100	--	--	ns
		Fast plus mode	50	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Set-Up Time for STOP Condition	$t_{SU;STO}$	Fast mode	0.6	--	--	µs
		Fast plus mode	0.26	--	--	
Bus Free Time between a STOP and START Condition	t_{BUF}	Fast mode	1.3	--	--	µs
		Fast plus mode	0.5	--	--	
Rising Time of both SDA and SCL Signals	t_R	Fast mode	20	--	300	ns
		Fast plus mode	--	--	120	
Falling Time of both SDA and SCL Signals	t_F	Fast mode	20	--	300	ns
		Fast plus mode	--	--	120	
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

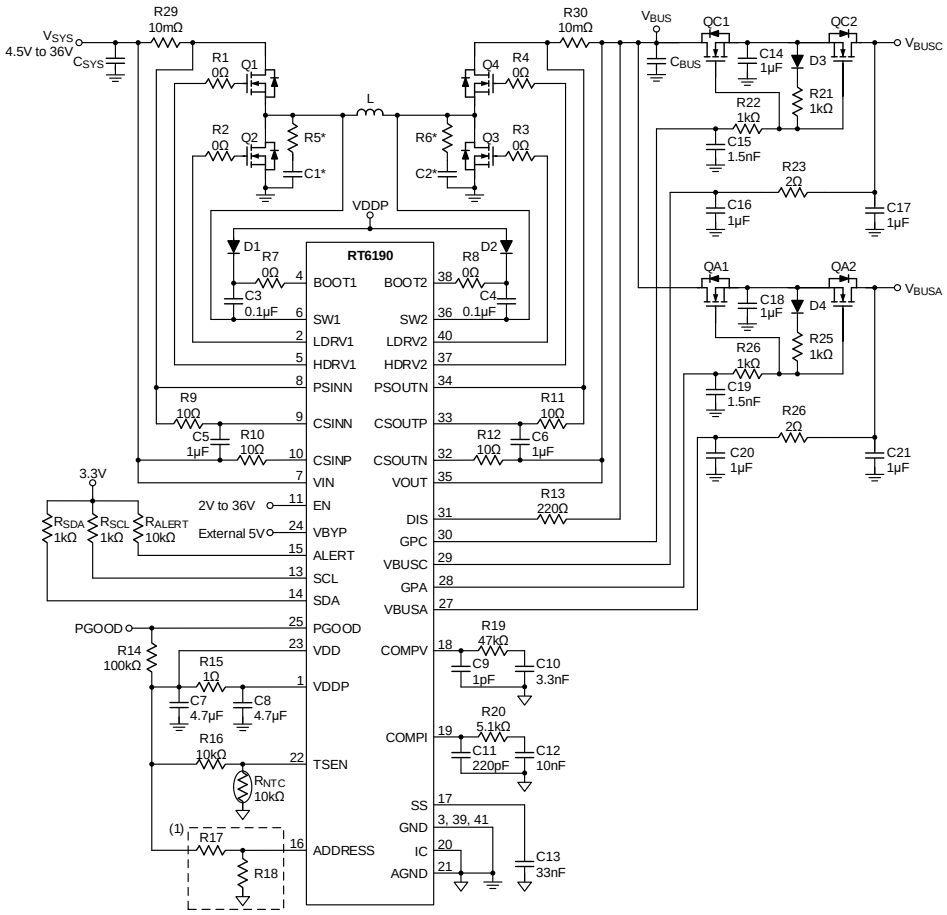
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. Guaranteed by design.

Typical Application Circuit

Normal Application Circuit for Forward and Reverse Operation



Note :

(1) I^2C slave address is 0x2C when R17 = NC, R18 = 100kΩ.
I^2C slave address is 0x2D when R17 = 100kΩ, R18 = NC.

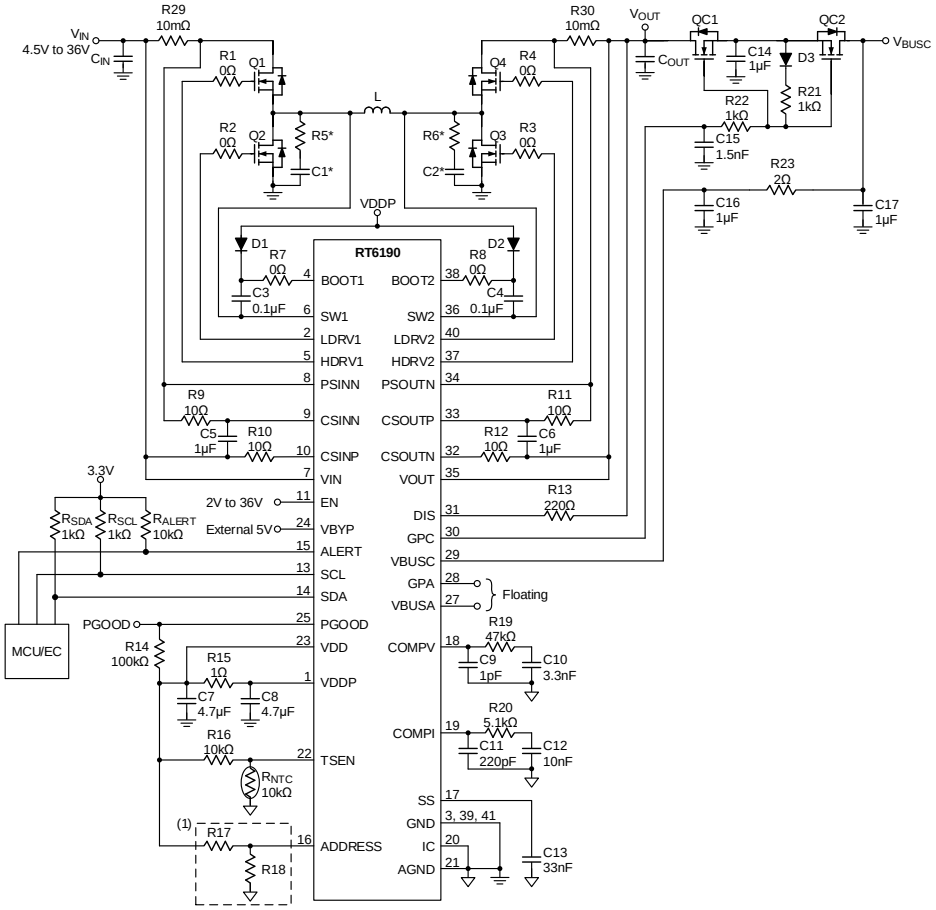
(2) For Forward operation:
- ✓ Connect input power supply to V_{SYS} and EN pin, and connect e-load to V_{BUSC}.
- ✓ Set 0x0E = 90h, 0x29 = 02h, then V_{BUSC} will be 5V.

(3) For Reverse operation:
- ✓ Connect input power supply to V_{BUSC} and EN pin, and connect e-load to V_{SYS}.
- ✓ Set 0x0C = 52h, 0x29 = 02h, 0x0E = 90h, then V_{SYS} will be 5V.

(4) Support 1C1A when V_{BUS} = 5V.

(5) * : Optional components R5, R6, C1 and C2 are used for Snubber.

RT6190 + MCU (with CC Logic) for Monitor



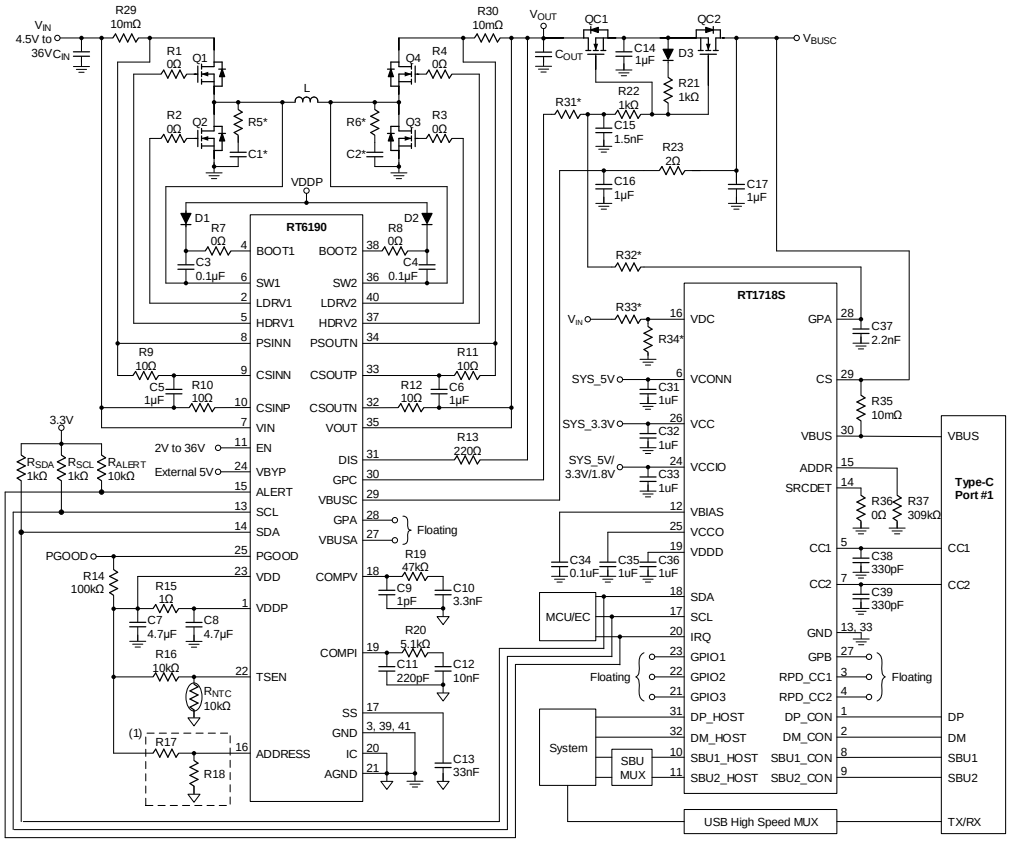
Note :

(1) I^{2}C slave address is 0x2C when R17 = NC, R18 = 100kΩ.
I^{2}C slave address is 0x2D when R17 = 100kΩ, R18 = NC.

(2) VBUSA and GPA can be floating if VBUSC used only.

(3) * : Optional components R5, R6, C1 and C2 are used for Snubber.

RT6190 + TCPC IC (RT1718S) for Monitor



Note :

(1) I^{2}C slave address is 0x2C when R17 = NC, R18 = 100kΩ.
I^{2}C slave address is 0x2D when R17 = 100kΩ, R18 = NC.

(2) VBUSA and GPA can be floating if VBUSC used only.

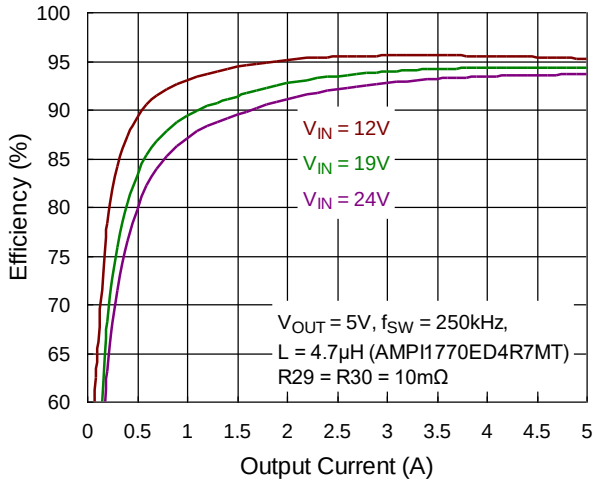
(3) * : Optional components
- ✓ R5, R6, C1 and C2 are used for Snubber.
- ✓ R31 = 0Ω, R32 = NC, QC1 and QC2 controlled by RT6190.
  R31 = NC, R32 = 0Ω, QC1 and QC2 controlled by RT1718S.
- ✓ Refer to RT1718S datasheet to set R33 and R34 for VDC pin.

Table 1. Recommended BOM

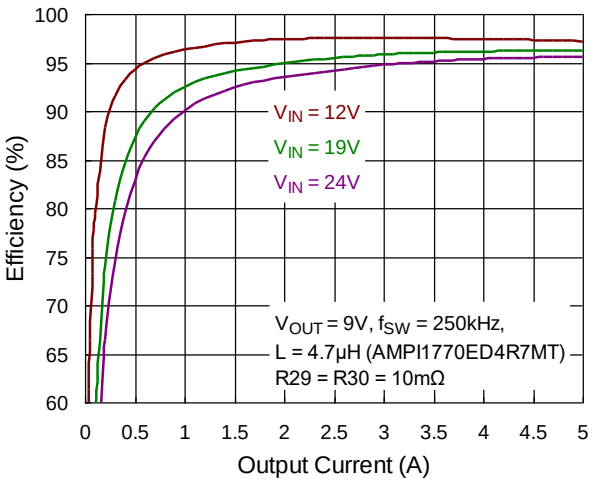
Reference	Qty	Part Number	Description	Package	Manufacture
U1	1	RT6190	DC-DC Controller	WQFN-40L 5x5	RICHTEK
L1	1	AMPI1770ED4R7MT	4.7μH	17.0 x 17.0 x 7.0	ARLITECH
	1	7443551470	4.7μH	12.8 x 12.8 x 6.2	WÜRTH ELEKTRONIK
	1	CMMB135T4R7MS	4.7μH	13.45 x 12.6 x 4.8	CYNTEC
C_{IN}	1	350ARHA101M08X8	100μF/35V/23mΩ	EC-2P_8_3-5MM	APAQ
	4	GRM31CR61H106KA12	10μF/50V	C-1206	MURATA
C_{OUT}	1	350ARHA101M08X8	100μF/35V/23mΩ	EC-2P_8_3-5MM	APAQ
	4	GRM31CR61H106KA12	10μF/50V	C-1206	MURATA
R29, R30	2	RLM-1632-6F-R010-FNH	Current Sense Resistor	R-1206	CYNTEC
Q1, Q4	2	SM4514NHKP	30V High-Side N-MOSFET for USB-PD 3.0 SPR Mode	DFN5x6-8	SINOPOWER
	2	SM4037NHKP	40V High-Side N-MOSFET for USB-PD 3.1 EPR Mode	DFN5x6-8	SINOPOWER
Q2, Q3	2	SM4512NHKP	30V Low-Side N-MOSFET for USB-PD 3.0 SPR Mode	DFN5x6-8	SINOPOWER
	2	SM4035NHKP	40V Low-Side N-MOSFET for USB-PD 3.1 EPR Mode	DFN5x6-8	SINOPOWER
QC1, QC2 QA1, QA2	4	SM3425NHQA	30V Power Path N-MOSFET for USB-PD 3.0 SPR Mode	DFN3.3x3.3-8	SINOPOWER
	4	SM3430NHQA	40V Power Path N-MOSFET for USB-PD 3.1 EPR Mode	DFN3.3x3.3-8	SINOPOWER
D1, D2, D3, D4	4	1N4148WS	Diode	SOD-323	PANJIT

Typical Operating Characteristics

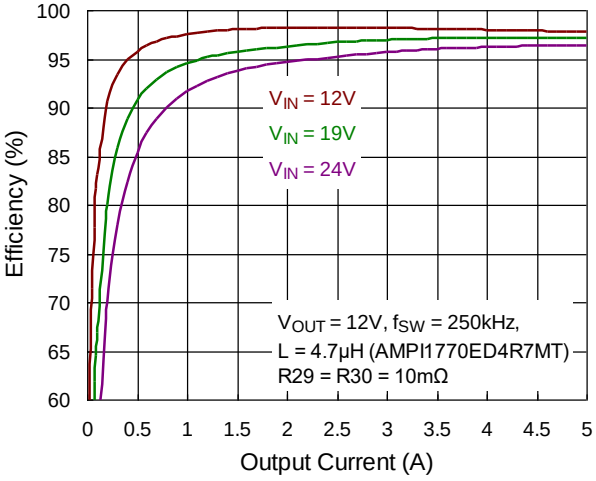
Efficiency vs. Output Current



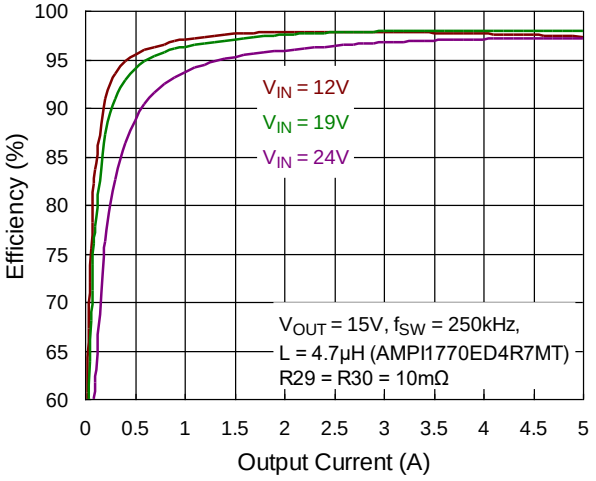
Efficiency vs. Output Current



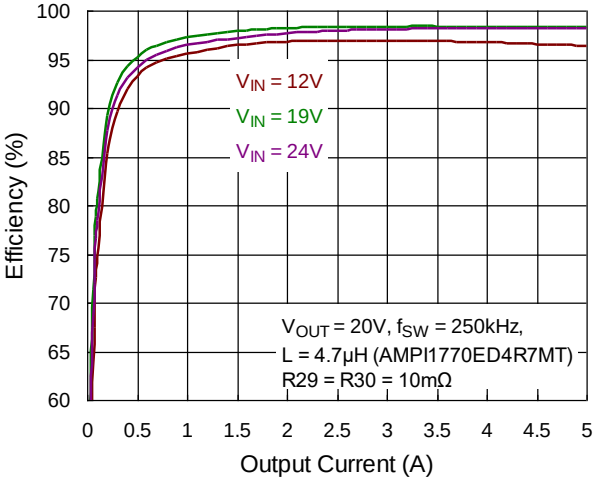
Efficiency vs. Output Current



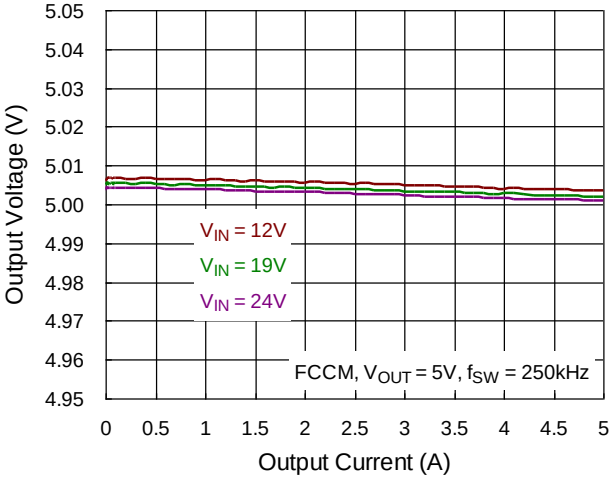
Efficiency vs. Output Current



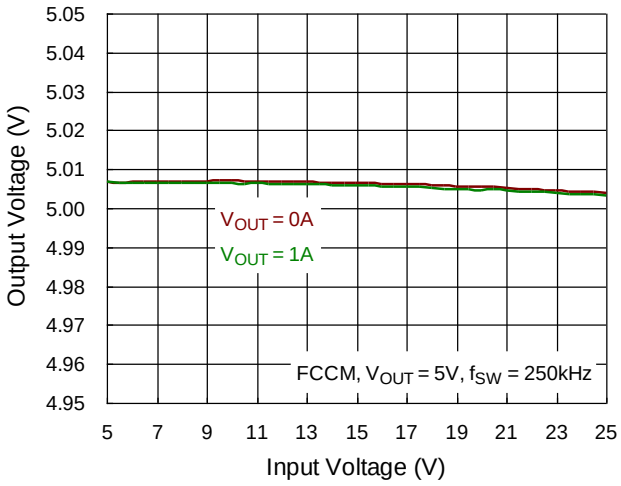
Efficiency vs. Output Current



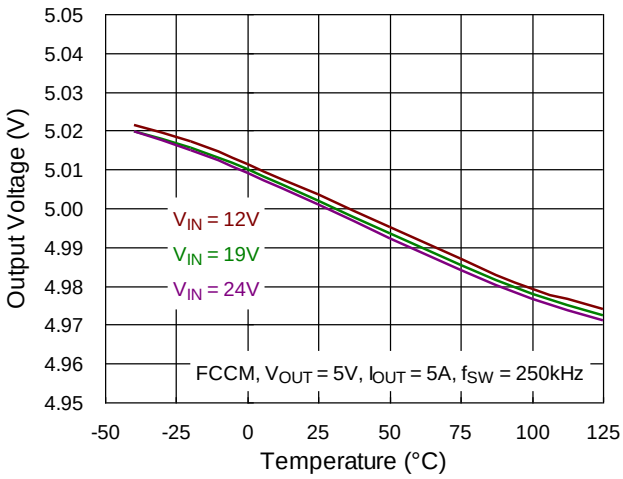
Output Voltage vs. Output Current



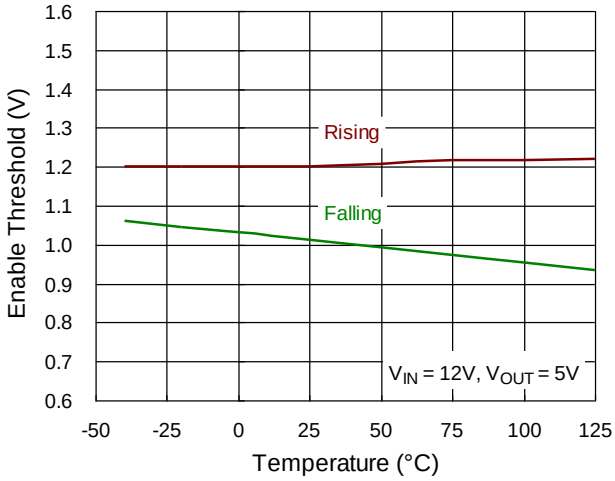
Output Voltage vs. Input Voltage



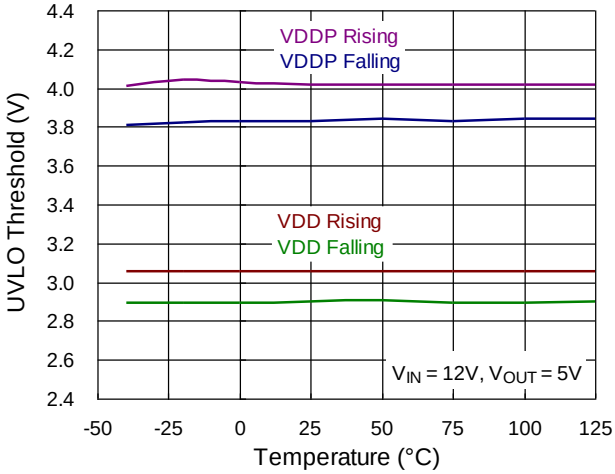
Output Voltage vs. Temperature



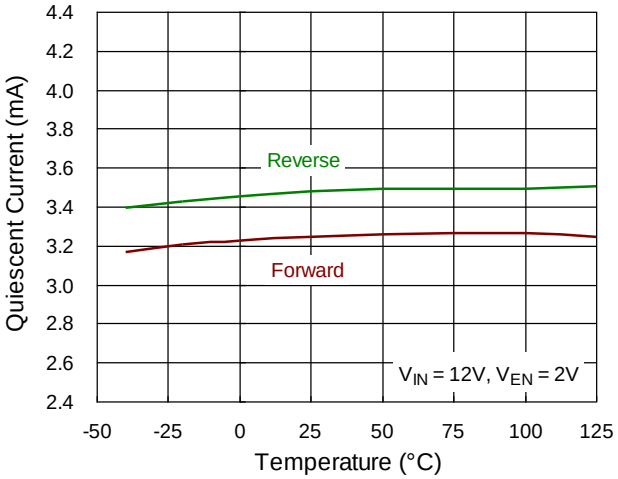
Enable Threshold vs. Temperature



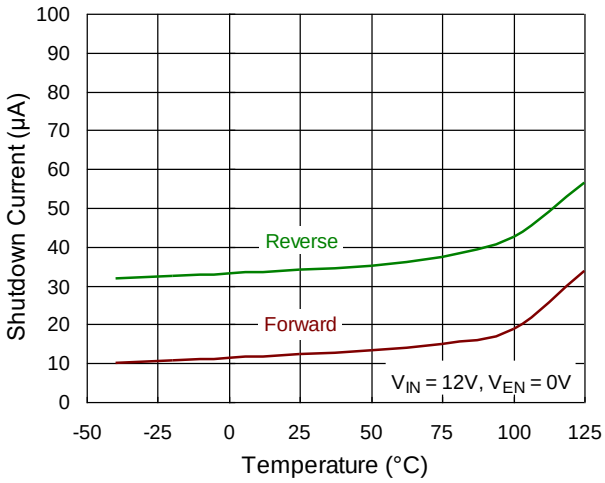
UVLO Threshold vs. Temperature



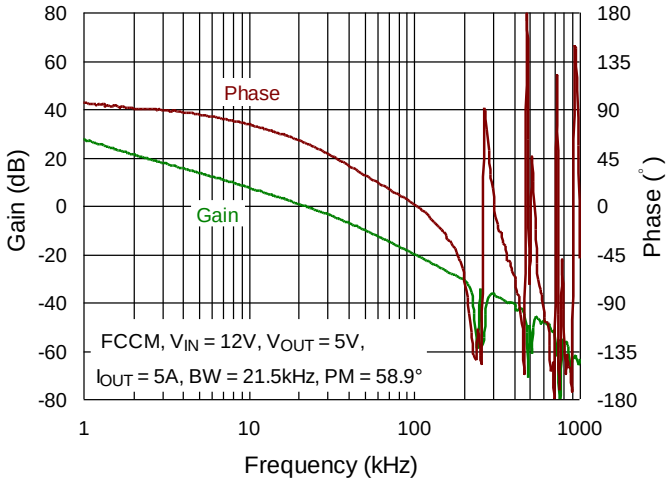
Quiescent Current vs. Temperature



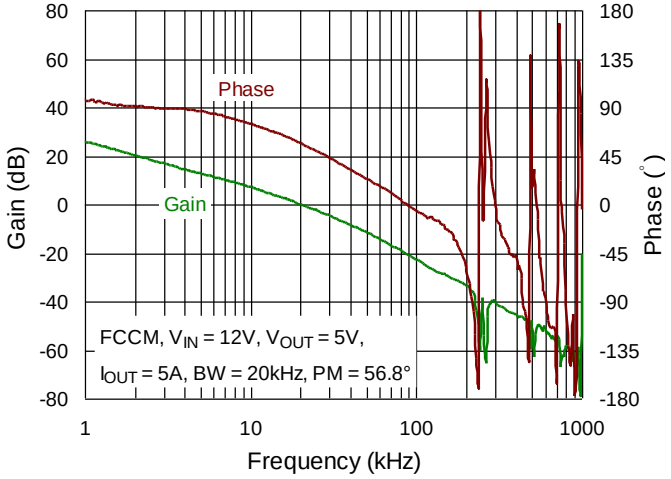
Shutdown Current vs. Temperature



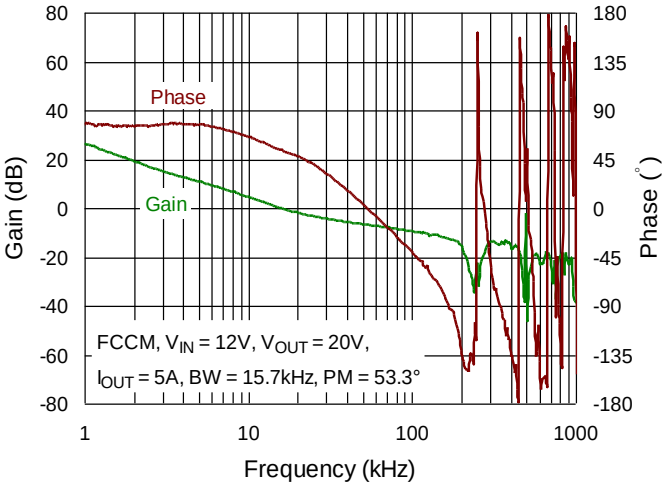
Forward Buck Mode Bode Plot



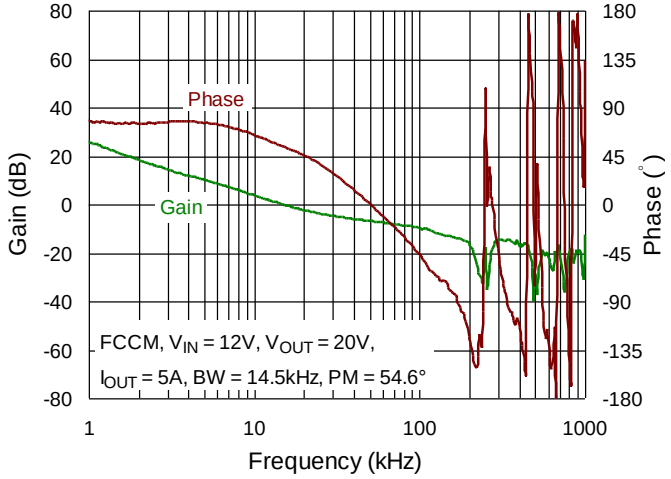
Reverse Buck Mode Bode Plot



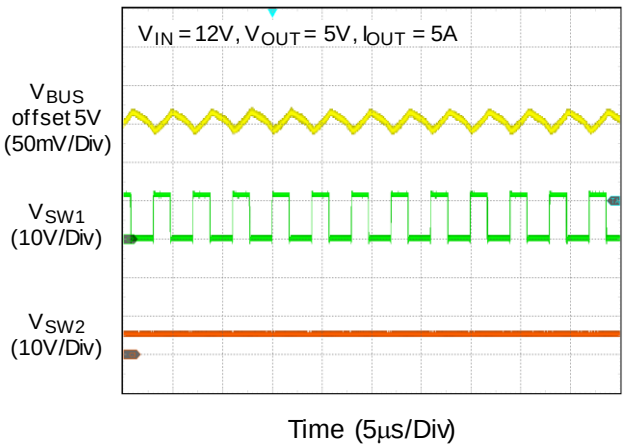
Forward Boost Mode Bode Plot



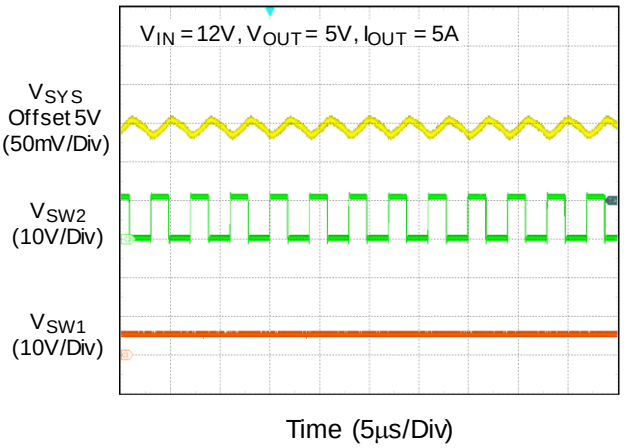
Reverse Boost Mode Bode Plot



Forward Buck Mode Output Ripple Voltage



Reverse Buck Mode Output Ripple Voltage



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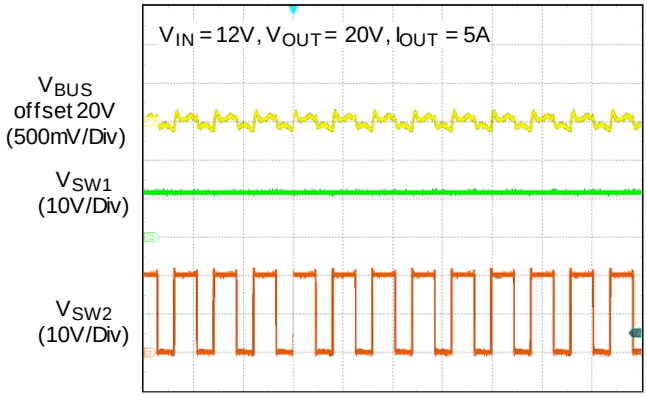

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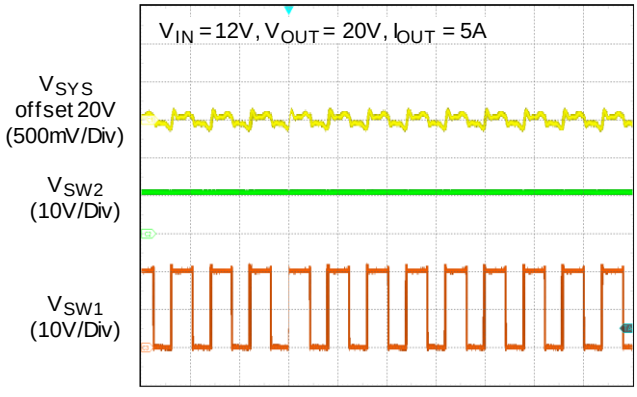
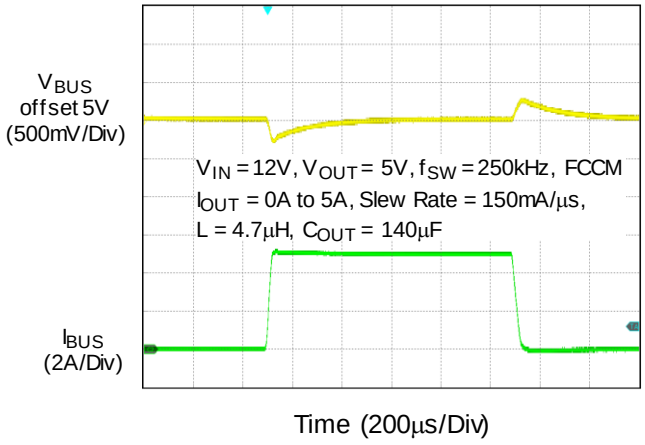


Forward Buck Mode Load Transient Response



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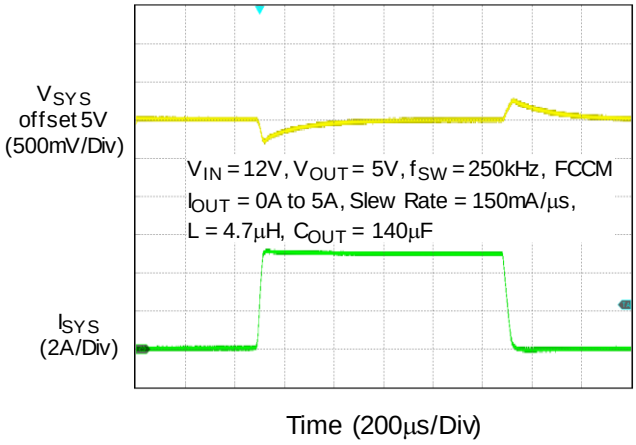

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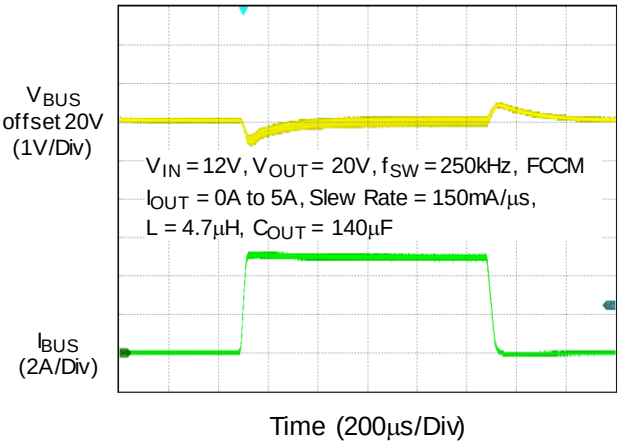

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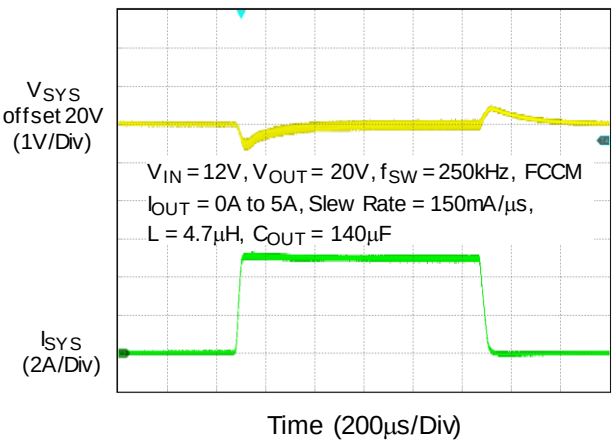
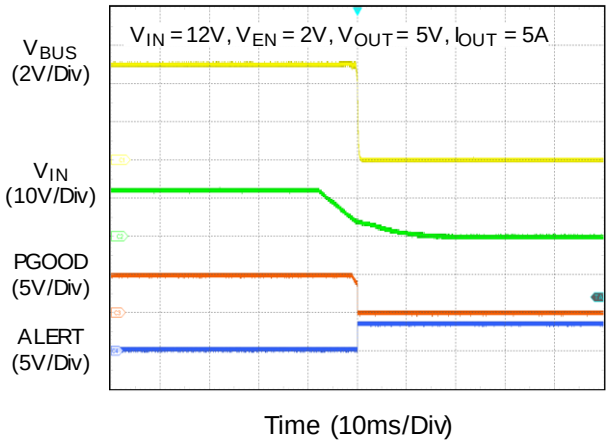
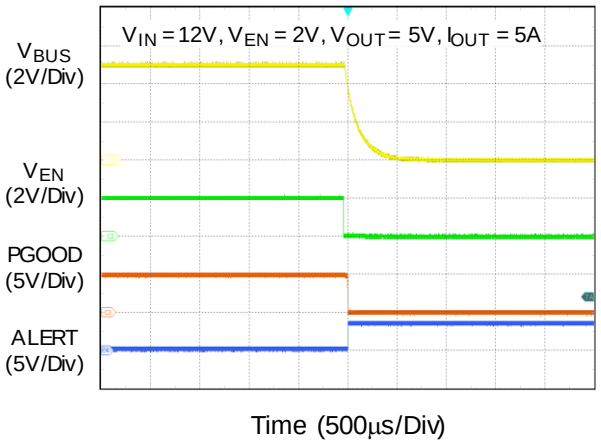


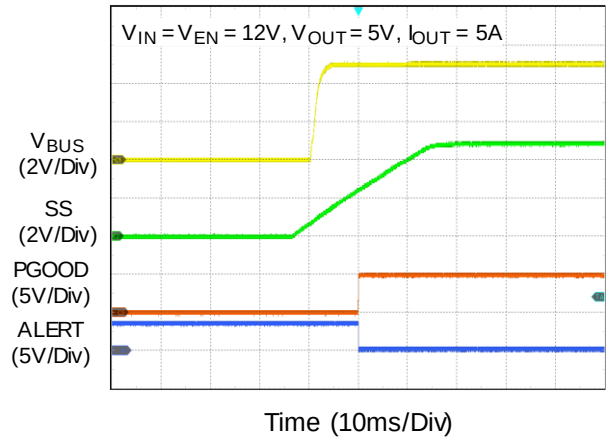
Power Off from VIN



Power Off from EN



Forward Power On from I2C



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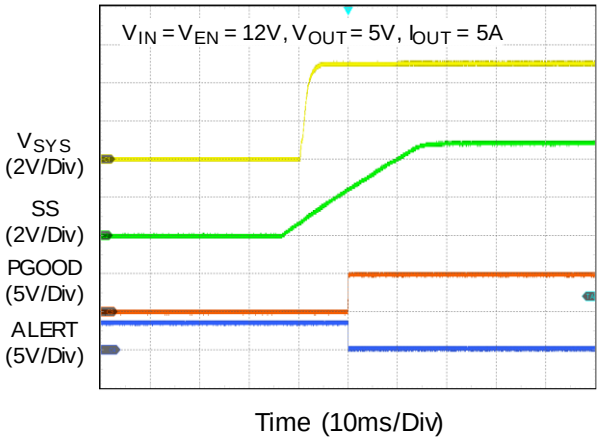

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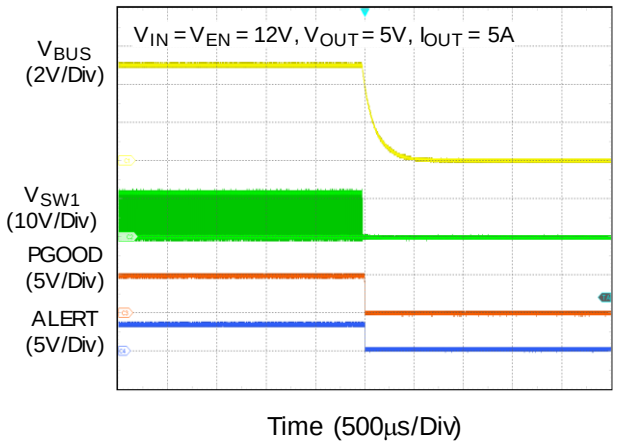
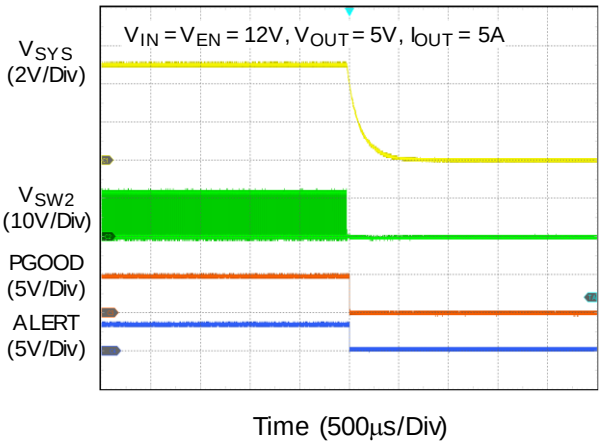
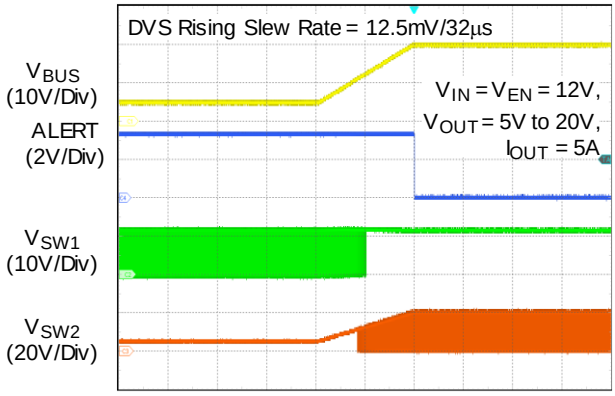


Reverse Power Off from I2C



Forward DVS Up



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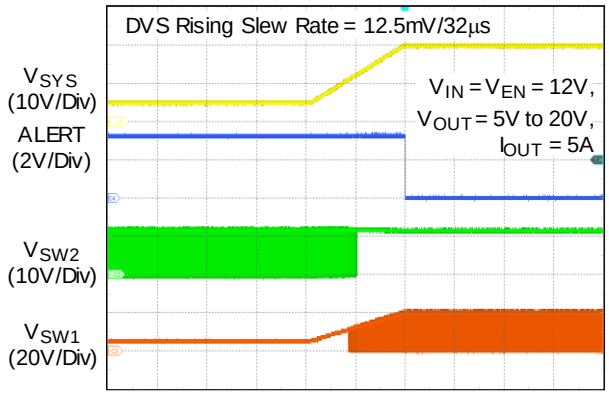
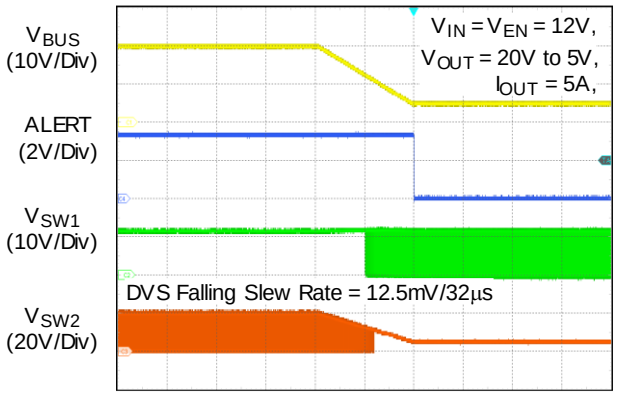


Forward DVS Down



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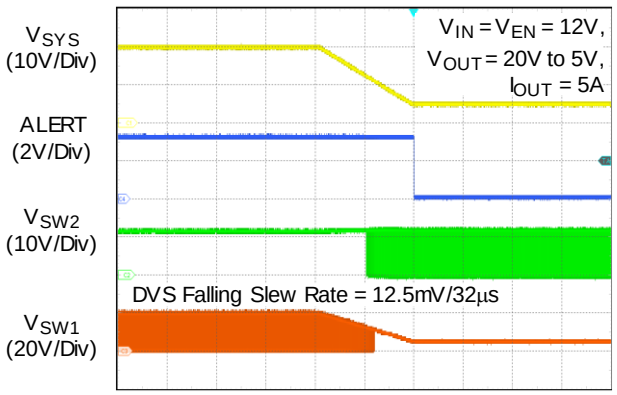
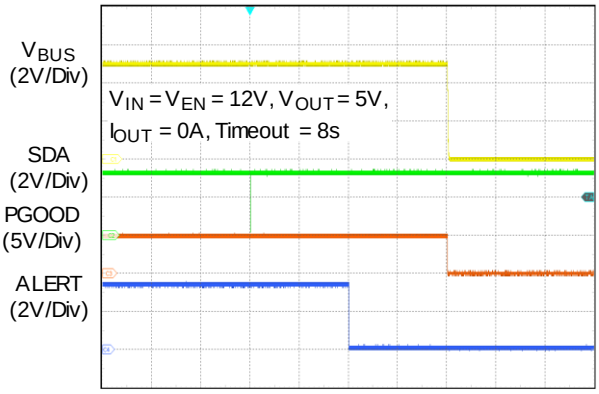
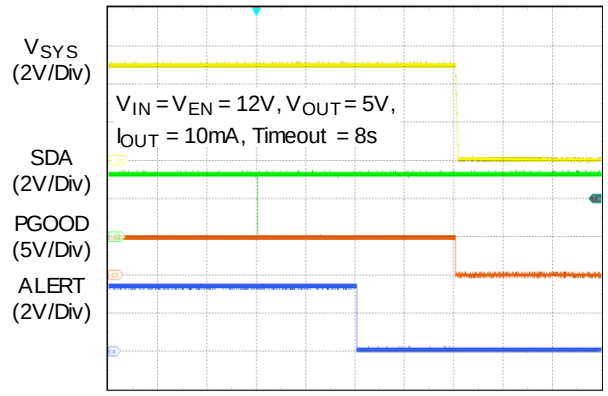


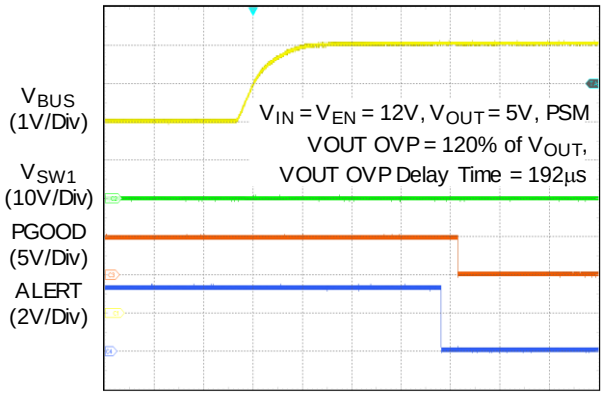
Forward Timer1 and Watchdog



Reverse Timer1 and Watchdog



Forward VOUT OVP



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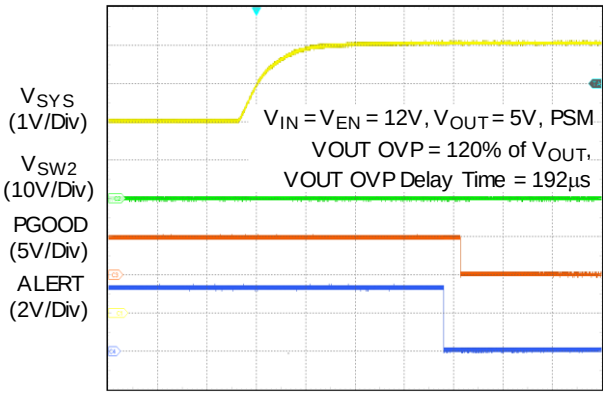
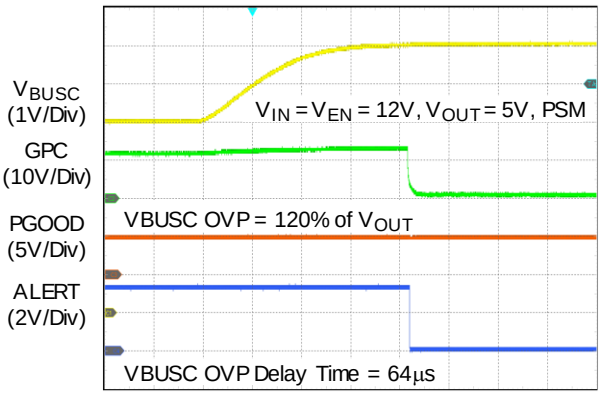
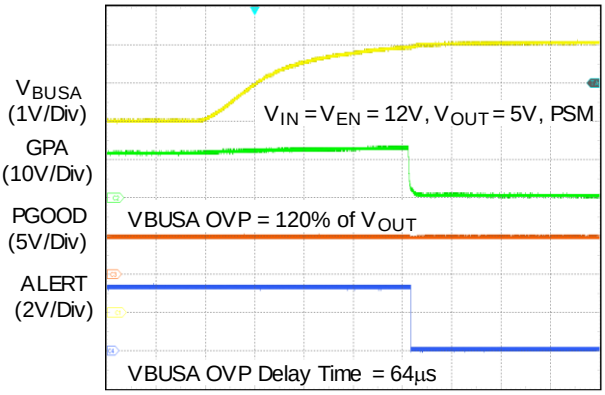


VBUSC OVP



VBUSA OVP



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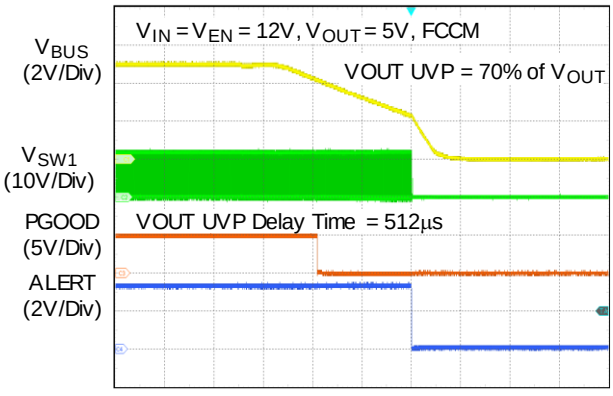

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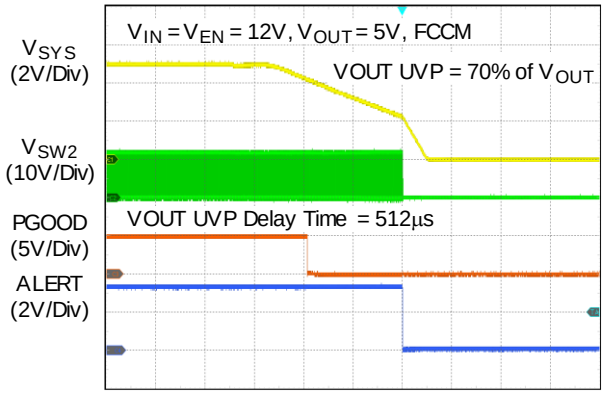

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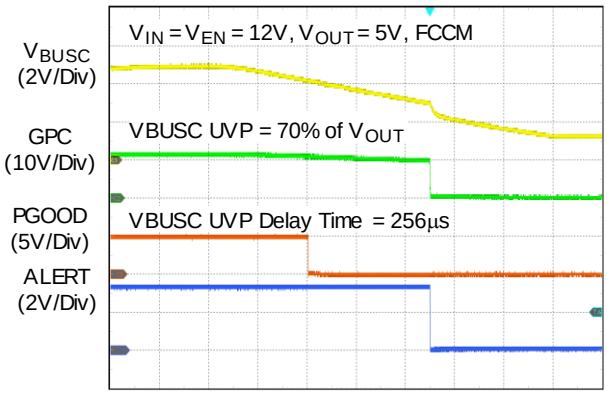
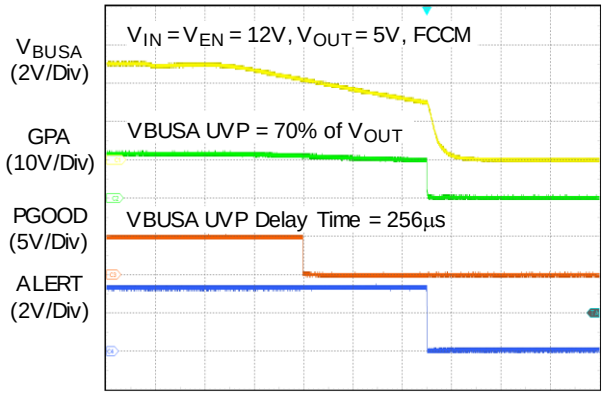


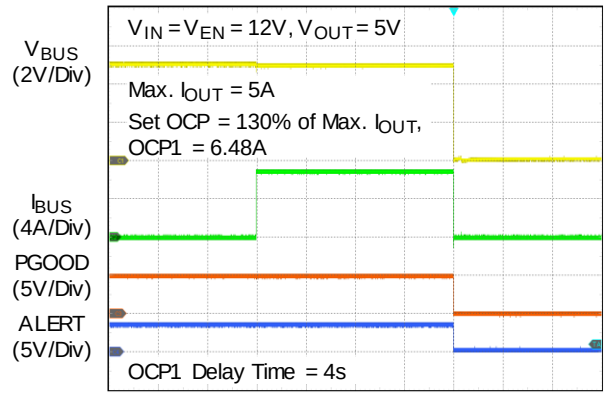
Time (200µs/Div)

VBUSA UVP



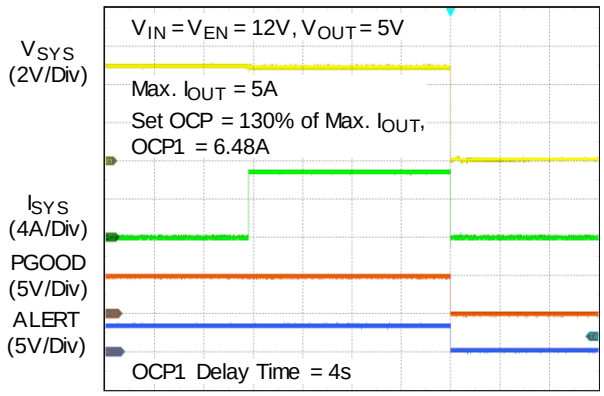
Time (200µs/Div)

Forward OCP



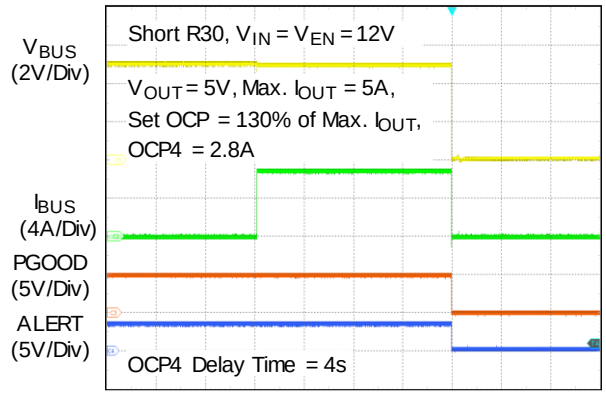
Time (1s/Div)

Reverse OCP



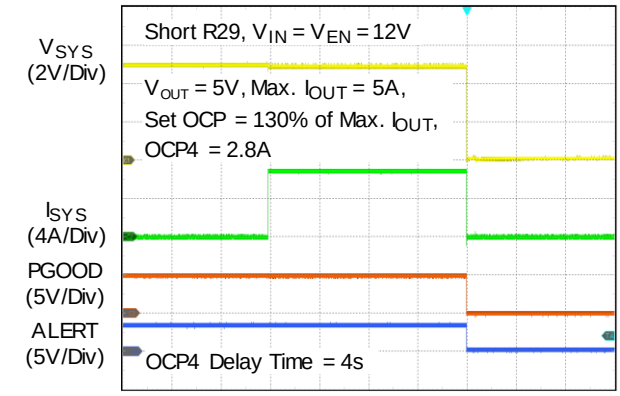
Time (1s/Div)

Forward 2nd OCP



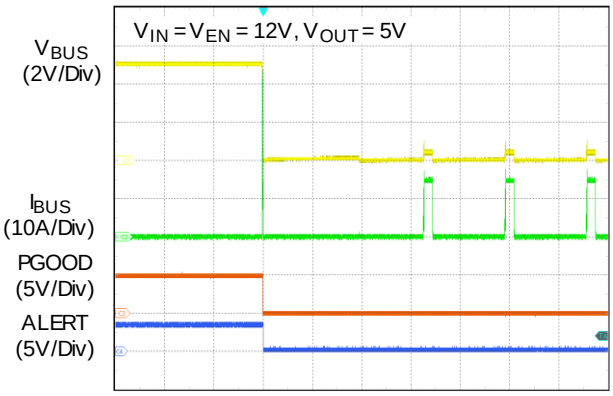
Time (1s/Div)

Reverse 2nd OCP

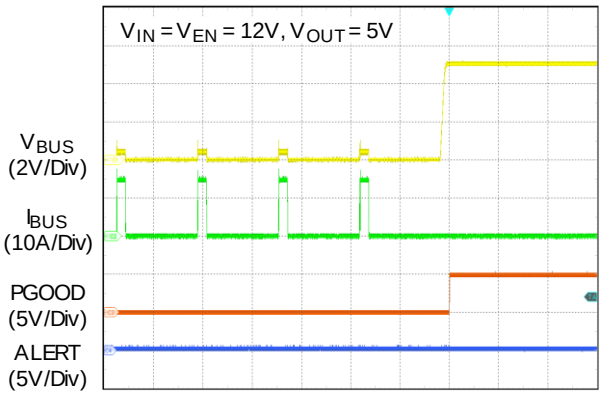


Time (1s/Div)

SCP Entry



SCP Release



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

A general RT6190 application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement and begins with the operating frequency from setting register 0x0D[2:0]. Then the inductor (L), the input capacitor (C_{IN}), and the output capacitor (C_{OUT}) can be determined in this section. In addition, other external components such as the internal regulator capacitor of VDD and VDDP pins, resistor and capacitor of the bootstrap network circuit, and the gate driver resistors for external power N-MOSMET will also be introduced. Finally, the discharge resistor from DIS pin to the output capacitor can be calculated to meet the USB power delivery specification.

Inductor Selection

The inductor selection trade-offs among size, cost, power conversion efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductor value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR). A good compromise between inductor size and power loss is from a 30% to 50% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value for Buck and Boost operations as follows :

$$L_{BUCK} = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

$$L_{BOOST} = \frac{V_{IN}}{\Delta I_L \times f_{SW}} \times \frac{(V_{OUT} - V_{IN})}{V_{OUT}}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded load transient response. This result in additional phase lag in the loop and reduce the crossover frequency. As the ratio of the slope compensation ramp to the sensed current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple current lowers the effective input peak current limit threshold and increases the AC losses in the inductor. To enhance the power conversion efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The selected inductor should have a saturation current rating greater than the peak current limit setting by RT6190, and the core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_{L\_BUCK} = \frac{(V_{IN} - V_{OUT})}{L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta I_{L\_BOOST} = \frac{V_{IN}}{L \times f_{SW}} \times \frac{(V_{OUT} - V_{IN})}{V_{OUT}}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \times (\Delta I_{L\_BUCK} \text{ or } \Delta I_{L\_BOOST})$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In load transient conditions, the inductor current can increase up to the input peak current limit setting by RT6190. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the input peak current limit rather than the peak inductor current.

Input Capacitor Selection

Since the input current is discontinuous conduction in Buck mode, and continuous conduction in Boost mode, the input capacitor (C_{IN}) is needed to filter the pulsating current at the drain terminal of an external power N-MOSFET (Q1 for Forward, and Q4 for Reverse) for Buck mode only. C_{IN} should be sized to do this without causing a large variation in input voltage. By using solid

or electrolytic capacitors as the input bulk capacitor, the peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = I_{OUT} \times \frac{D \times (1-D)}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR_{CIN}$$

where D = V_{OUT} / V_{IN}, and ESR_{CIN} is the equivalent series resistance of the input capacitor.

Then, the minimum value of effective input capacitance can be estimated with ESR as equation below :

$$C_{IN\_MIN} = I_{OUTMAX} \times \frac{D \times (1-D)}{(\Delta V_{CIN\_MAX} - I_{OUT\_MAX} \times ESR_{CIN}) \times f_{SW}}$$

assume ΔV_{CIN_MAX} = 200mV for typical application.

Figure 5 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the input capacitors.

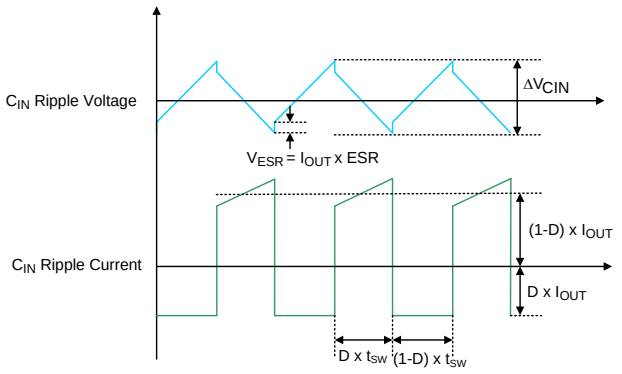


Figure 5. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a low ESR and must be rated to handle the worst-case RMS input current. The RMS input ripple current (I_{CIN_RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and maximum output current (I_{OUT_MAX}) as the following equation :

$$I_{CIN\_RMS} \cong I_{OUT\_MAX} \times \sqrt{D \times (1-D)}$$

The worst condition occurs when duty cycle = 50%, then V_{IN} = 2 x V_{OUT} and maximum RMS input ripple current will be 0.5 x I_{OUT_MAX}. Note that ripple current ratings from capacitor manufacturers are often based on 2000 hours life cycle only, which makes it advisable to further de-rate the capacitor, or choose a capacitor with higher temperature rating than required.

The input capacitor should be placed as close as possible to the input current sense resistor (R29 for Forward, and R30 for Reverse), and with a low inductance connection from negative side of the input capacitor to S terminal of an external power N-MOSFET (Q2 for Forward, and Q4 for Reverse). The larger input capacitance is required for high power application by the combination of larger bulk capacitor and 2 to 4 ceramic capacitors of 10μF with 1206 in size.

In addition, the combination of bulk and ceramic capacitors can provide high ripple current capacity, reduce the output voltage ripple and minimize transient effects during output load change. For filtering high frequency noise, additional small capacitor 1μF with 0603 in size should be placed close to the part. It is recommended to use ceramic capacitors with X7R type and voltage rating up to 50V for best performance across temperature and input voltage variations.

Output Capacitor Selection

The output capacitor (C_{OUT}) is determined to satisfy the requirements for output voltage ripple and the load transient response. Similar the input current conduction mode for different operation, the output current is continuous conduction in Buck mode, and discontinuous conduction in Boost mode. C_{OUT} needs to decrease the output voltage ripple caused by the pulsating output current in Boost mode. By using solid capacitors as the output bulk capacitor, the peak-to-peak voltage ripple on output capacitor can be calculated as equation below :

$$\Delta V_{COUT} = I_{OUT} \times \frac{D}{C_{OUT} \times f_{SW}} + \frac{I_{OUT}}{1-D} \times ESR_{COUT}$$

where D = (V_{OUT} − V_{IN}) / V_{OUT}, and ESR_{COUT} is the equivalent series resistance of the output capacitor.

Then, the minimum value of effective output capacitance can be calculated with ESR as equation below :

$$C_{OUT\_MIN} = I_{OUT\_MAX} \times \frac{D}{\left(\Delta V_{COUT\_MAX} - \frac{I_{OUT\_MAX}}{1-D} \times ESR_{COUT}\right) \times f_{SW}}$$

where ΔV_{COUT_MAX} is the design target to meet system requirement.

In addition, the output capacitor also needs to have a low ESR and must be rated to handle the worst-case RMS output current in real application. The RMS output ripple current (I_{COUT_RMS}) of the regulator can be

determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and maximum output current (I_{OUT_MAX}) as the following equation :

$$I_{COUT\_RMS} \cong I_{OUT\_MAX} \times \sqrt{\frac{D}{1-D}}$$

Assume V_{IN_MIN} is 12V and V_{OUT_MAX} is 20V defined from system, the duty cycle of the regulator is 40%, and the worst case of RMS output ripple current will be 0.8165 x I_{OUT_MAX}. Note that ripple current ratings from capacitor manufacturers are often based on 2000 hours life cycle only, which makes it advisable to further de-rate the capacitor, or choose a capacitor with higher temperature rating than required.

The output capacitor should be placed as close as possible to the output current sense resistor (R30 for Forward, and R29 for Reverse), and with a low inductance connection from negative side of the output capacitor to S terminal of an external power N-MOSFET (Q4 for Forward, and Q2 for Reverse). The larger output capacitance is required for high power application by the combination of larger bulk capacitor and 2 to 4 ceramic capacitors of 10μF with 1206 in size. In addition, the combination of bulk and ceramic capacitors can provide high ripple current capacity, reduce the output voltage ripple and minimize transient effects during output load change. For filtering high frequency noise, additional small capacitor 1μF with 0603 in size should be placed close to the part. It is recommended to use ceramic capacitors with X7R type and voltage rating up to 50V for best performance across temperature and input voltage variations.

Loop Compensation Design

In real condition, the undercompensated system may result in unstable operations such as audible noise from the magnetic components or capacitors, larger jitter rate of the switching waveforms, output voltage oscillation, overheating of external power N-MOSFETs and so on. In order to check loop response of the compensated system, the Bode plot can be ideally measured with a network analyzer such as Bode 100. However, the measurements will be error due to parasitic parameters from PCB layout and components nonlinearity such as the ESR variations of output capacitors, linearity of inductors and capacitors, etc. In addition, the limited measurement accuracy of the instrument will also have an influence on measured results.

The RT6190 provides two control loops by connecting relative network circuit from COMPV or COMPI pins to AGND. The COMPV pin is used for main control loop to ensure loop stability and load transient response requirements, and COMPI pin is used for output constant current function setting by register 0x03/0x04. In addition, the input constant voltage (Register 0x05) function will also have an influence on main control loop. By using peak current mode control topology, the RT6190 will operate in Buck and Boost modes automatically. The used method below can easily calculate the component value for compensation by ignoring the effects of the slope compensation due to its internal to the RT6190.

Since the compensation design is more restrictive when a right half plane zero appeared in boost mode, the COMPV compensation components can be calculated based on Boost mode as the following steps below :

(1) Assume some parameters for normal operation below :

- ✓ Input voltage V_{IN} = 12V
- ✓ Output voltage V_{OUT} = 5V for Buck mode, and V_{OUT} = 20V for Boost mode
- ✓ Maximum output current I_{OUT} = 5A
- ✓ Inductor L = 4.7μH
- ✓ Output capacitor C_{OUT} = 140μF with R_{ESR} = 1mΩ

(2) Power stage pole and zero location :

$$f_{P\_BUCK} = \frac{1}{2\pi} \times \left(\frac{1}{C_{OUT} \times R_{OUT\_BUCK}} \right) = 1.14kHz$$

$$f_{P\_BOOST} = \frac{1}{2\pi} \times \left(\frac{2}{C_{OUT} \times R_{OUT\_BOOST}} \right) = 568Hz$$

$$f_{Z} = \frac{1}{2\pi} \times \left(\frac{1}{C_{OUT} \times R_{ESR}} \right) = 1.14MHz$$

$$f_{Z\_RHP} = \frac{1}{2\pi} \times \left(\frac{R_{OUT\_BOOST} \times (1-D_{BOOST})^2}{L} \right) = 48.8kHz$$

where R_{OUT_BUCK} = 1Ω when V_{OUT} = 5V and max. I_{OUT} = 5A, R_{OUT_BOOST} = 4Ω when V_{OUT} = 20V and max. I_{OUT} = 5A, D_{BOOST} = 0.4 when V_{IN} = 12V

and V_{OUT} = 20V.

(3) Set the crossover frequency f_C to be less than one-fifth of the right half plane zero f_{Z_RHP} in Boost mode.

(4) R19 as the typical application circuit can be calculated as :

$$R19 = \frac{2\pi \times C_{OUT} \times f_C}{1-D_{BOOST}} \times \frac{A_{CS} \times R_{CSI}}{Gmv} \times \frac{1}{VOUT\_RATIO}$$

where A_{CS} = 16, Gmv = 550μA/V, R_{CSI} = R29 = 10mΩ for Forward operation and R_{CSI} = R30 = 10mΩ for Reverse operation, VOUT_RATIO default factory setting is 0.08 and can be adjustable by register 0x11[5] when 0x0E[7] = 0.

(5) C10 as the typical application circuit can be calculated as :

$$C10 = \frac{C_{OUT} \times R_{OUT\_BOOST}}{2 \times R19}$$

(6) C9 as the typical application circuit can be calculated as :

$$C9 = \frac{C_{OUT} \times R_{ESR}}{R19}$$

Based on the equation above, the final compensation components of COMPV can be selected as R19 = 47kΩ, C10 = 3.3nF and C9 = 1pF.

Since the loop response of output constant current function will be slower than main control loop, and a right half plane zero appeared in Boost mode, the crossover frequency f_C can be set to less than one-fifth to one-tenth of the right half plane zero f_{Z_RHP}. The COMPI compensation values can be calculated as below :

$$R20 = \frac{A_{CS}}{GAIN\_OCS \times Gmi} \times \frac{R_{CSI}}{R_{CSO}} \times \frac{(1-D_{BOOST})^2}{VIN} \times 2\pi \times C_{OUT} \times f_C \times R_{OUT\_BOOST}^2$$

$$C12 = \frac{\sqrt{C_{OUT} \times L}}{R20 \times (1\text{-}D_{BOOST})}$$

$$C11 = \frac{1}{2\pi \times f_{Z\_RHP} \times R20}$$

where A_{CS} = 16, Gmi = 550μA/V, R_{CSI} = R29 = 10mΩ for Forward operation and R_{CSI} = R30 = 10mΩ for Reverse operation, R_{CSO} = R30 = 10mΩ for Forward operation and R_{CSO} = R29 = 10mΩ for Reverse operation, GAIN_OCS = 10 and can be adjustable by register 0x0F[1:0] after RT6190 powered on.

Based on the equation above, the final compensation components can be selected as R20 = 5.1kΩ, C12 = 10nF and C11 = 220pF.

Output Discharge Time Setting

The RT6190 provides output discharge function to discharge output capacitor quickly by connecting external discharge resistor from DIS pin to the positive side of output capacitor. Register 0x0E[4] is the enable control bit of output discharge function, and the default factory setting of 0x0E[4] = 1 for default output discharge function enable.

When RT6190 operates in power off conditions or DVS down operation, the internal N-MOSFET of DIS pin will be turned on to discharge output capacitor by internal N-MOSFET $R_{DS(ON)}$ (Typically 6Ω) and external discharge resistor. The power off conditions include external EN pin off where output discharge function is default on, and I2C EN_PWM (0x0E[7]) off where output discharge function is controlled by 0x0E[4]. If RT6190 operates in DVS down operation, the output discharge function is enabled only for DVS falling time plus an additional 100ms for correct operation in PSM condition, and this time interval can be calculated by the equation below :

$$t_{DIS\_EN} = \frac{V_{OUT1}\text{-}V_{OUT2}}{\text{DVS Down Slew Rate}} + 100ms$$

where V_{OUT1} is the initial output voltage before DVS down operation, and V_{OUT2} is the final output voltage after DVS down operation, DVS down slew rate is referred to 0x0D[4:3].

For example, t_{DIS_EN} is equal to 138.4ms when DVS down from 20V to 5V with 0x11[5] = 0 and 0x0D[4:3] = 11.

The output voltage is discharged by the external discharge resistance and output capacitance, and discharge time can be calculated by the equation below :

$$t_{DIS} = (R_{DS(ON)} + R13) \times C_{OUT} \times \ln\left(\frac{V_{OUT\_INI}}{V_{OUT\_FINAL}}\right)$$

where $R_{DS(ON)}$ is the on-resistance of internal N-MOSFET for DIS pin, R13 is the external discharge

resistor which is referred to the application circuit, C_{OUT} is the total capacitance of the PWM output, V_{OUT_INI} is the initial output voltage before discharging, and V_{OUT_FINAL} is the final output voltage after discharging.

Note that VOUT over-voltage protection will be triggered if RT6190 operates in DVS down operation with PSM and t_{DIS} is longer than t_{DIS_EN}.

Internal Regulator

The RT6190 integrates a 5V linear regulator (VDD) that is supplied from VIN or VBUSC to provide power to the internal circuitry. For internal MOSFET gate drivers, it is necessary to connect an R-C filter from VDD pin to VDDP pin. The VDD can be used as PGOOD pull-up supply, but it is "NOT" allowed to power other device or circuitry. It is recommended to use 4.7μF/X5R with 0603 in size and rated voltage higher than 10V as bypass capacitors for VDD and VDDP, and it needs to be placed as close as possible to the VDD and VDDP pins.

Bootstrap Driver Supply

The external bootstrap capacitors (C3/C4) between BOOTx and SWx pins are used to create a voltage rail above the applied input voltage to turn on external power N-MOSFET (Q1/Q4). Once the external power N-MOSFET (Q2/Q3) are turned on, the external bootstrap capacitors can be charged through an internal diode to a voltage equal to approximately VDD each time. It is recommended to use 0.1μF/X5R with 0603 in size and rated voltage higher than 10V as bootstrap capacitors, and it needs to be placed as close as possible to BOOTx and SWx pins.

External Bootstrap Diode

It is recommended to add an external bootstrap Schottky diode between an external 5V voltage supply and BOOTx pins to improve enhancement of the external power N-MOSFET (Q1/Q4) and improve efficiency when high power application. Refer to D1/D2 of application circuit for correct connection. The external bootstrap Schottky diode can be 1N4148 or BAT54 for low-cost consideration and the external 5V can be a fixed 5V voltage supply from the system, or a VDDP pin voltage for saving power rail. Note that the $V_{BOOTx-SWx}$ must be lower than 5.5V for correct operation.

External Bootstrap Resistor (Option)

The external bootstrap resistors (R7/R8) between BOOTx pins and external bootstrap capacitors (C3/C4) are reserved to reduce the voltage spike at switch node (SW1/SW2). The potential EMI issues will also be minimized due to smaller di/dt noise caused by slow rising slew rate of external power N-MOSFET (Q1/Q4). The external bootstrap resistor selection trade-offs voltage spike at switch node, potential EMI issues and power conversion efficiency. Therefore, the usual range of external bootstrap resistor is from 0Ω to 10Ω with 0603 in size, and it is recommended to use 0Ω for initial setting. Refer to application circuit for correct connection of bootstrap network circuit.

Gate Driver Resistor for External Power N-MOSFET (Option)

The gate driver resistors (R1/R2/R3/R4) are placed optional between HDRVx/LDRVx pins and external power N-MOSFET (Q1/Q2/Q3/Q4). Different from the function of external bootstrap resistor, the rising and falling slew rate of an external power N-MOSFET will be both slow. The gate driver resistors (R1/R4) for the external power N-MOSFET (Q1/Q4) are also used to reduce the voltage spike at switch node (SW1/SW2) to minimize potential EMI issues, but the gate driver resistors (R2/R3) for the external power N-MOSFET (Q2/Q3) are only used to add series resistance to avoid LDRVx turned on rapidly. The gate driver resistor selection also trade-offs voltage spike at switch node, potential EMI issues and power conversion efficiency. Therefore, the usual range of gate driver resistor is from 0Ω to 10Ω with 0603 in size, and it is recommended to use 0Ω for initial setting. Refer to application circuit for correct connection.

RC Snubber Components (Option)

The RC snubber (R5/R6/C1/C2) components are placed optional in parallel with an external power N-MOSFET (Q2/Q3) to avoid larger voltage spike appeared between D and S terminals of an external power N-MOSFET (Q2/Q3). These components are also used to minimize the potential EMI issues due to smaller voltage spike at switch node (SW1/SW2). The RC snubber components selection also trade-offs

voltage spike between D and S terminals of an external power N-MOSFET (Q2/Q3), potential EMI issues and power conversion efficiency. Therefore, the usual range of snubber resistor (R5/R6) is from 0Ω to 10Ω, and snubber capacitor (C1/C2) is from 100pF to 1nF. To avoid larger power dissipation on snubber resistor (R5/R6), it is recommended to use 1206 in size when larger snubber capacitor (C1/C2) is selected. Refer to application circuit for correct connection.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid the permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (27.5°C/W) = 3.63W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

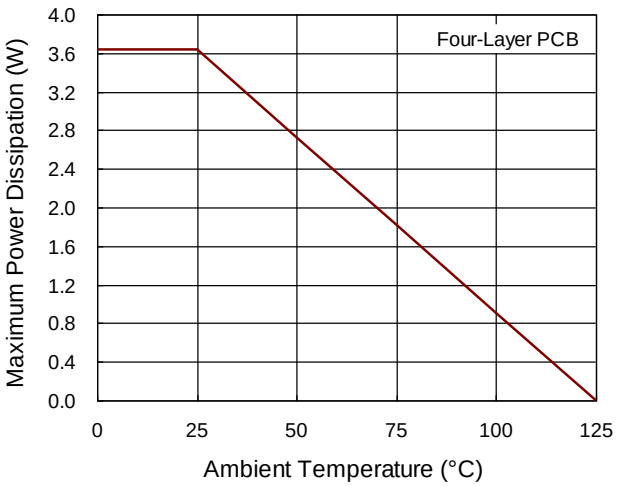


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RT6190 :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place input capacitors, external power N-MOSFETs Q1 and Q2, and input current sense resistor R29 as close together as possible to minimize loop impedance of input switching current.
- Place output capacitors, external power N-MOSFETs Q3 and Q4, and output current sense resistor R30 as close together as possible to minimize loop impedance of output switching current.
- Place multiple vias near the negative side of the input and output capacitor, and the s terminal of external power N-MOSFETs to reduce parasitic inductance and improve thermal performance.
- Place C7 and C8 as close to VDD and VDDP pins as possible.
- Place bootstrap capacitor C3 and C4 as close to IC as possible, and connect directly between BOOTx and SWx pins.

- Route the trace with 30mil width for BOOTx, SWx, HDRVx, LDRVx pins, and 20mil for VDD, VDDP, VBUSC, GPC, VBUSA, GPA pins.
- The high frequency switching nodes, BOOTx and SWx, should be as small as possible, and reduce the area size of SWx exposed copper to minimize the electrically coupling from this voltage. Keep analog components away from the BOOTx and SWx nodes.
- Minimize current sense voltage errors by using Kelvin connection for PCB routing. R29, CSINP/CSINN and VIN/PSINN pins for input current sense, R30, CSOUTP/CSOUTN and VOUT/PSOUTN for output current sense.
- Place the compensation components R19/C9/C10 and R20/C11/C12 near the IC.
- Place the soft-start capacitor C13 near the IC.
- Separate AGND and GND planes to avoid noise couple on SS pins and network circuit of COMPV and COMPI pins.

Figure 7. and Figure 8. are the layout example that uses four-layer PCB in size of 132mm x 90mm with 1oz copper thickness.

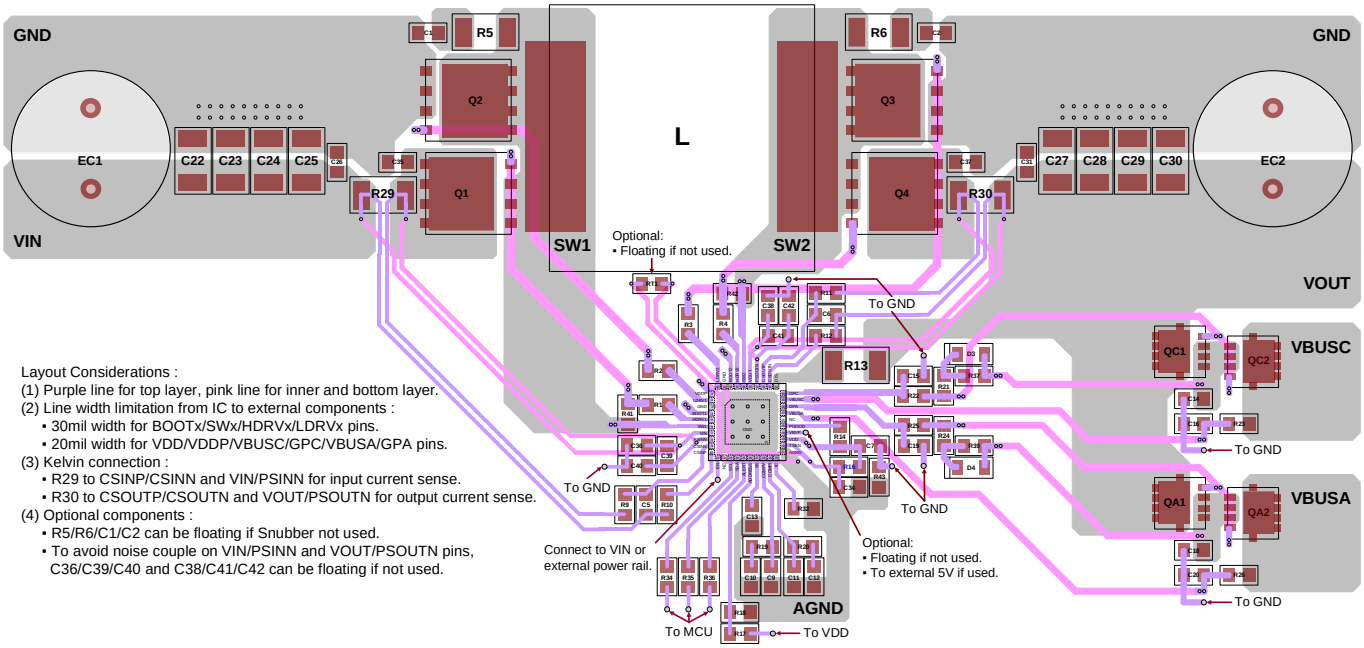


Figure 7. PCB Layout in Top Layer

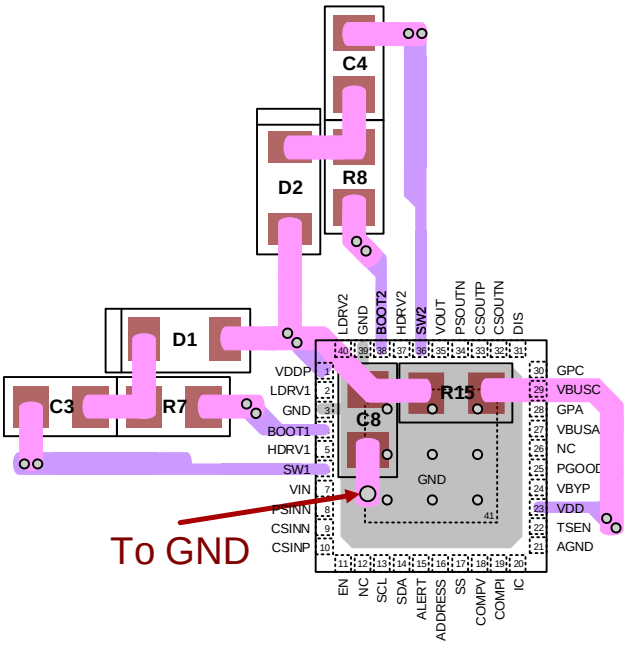
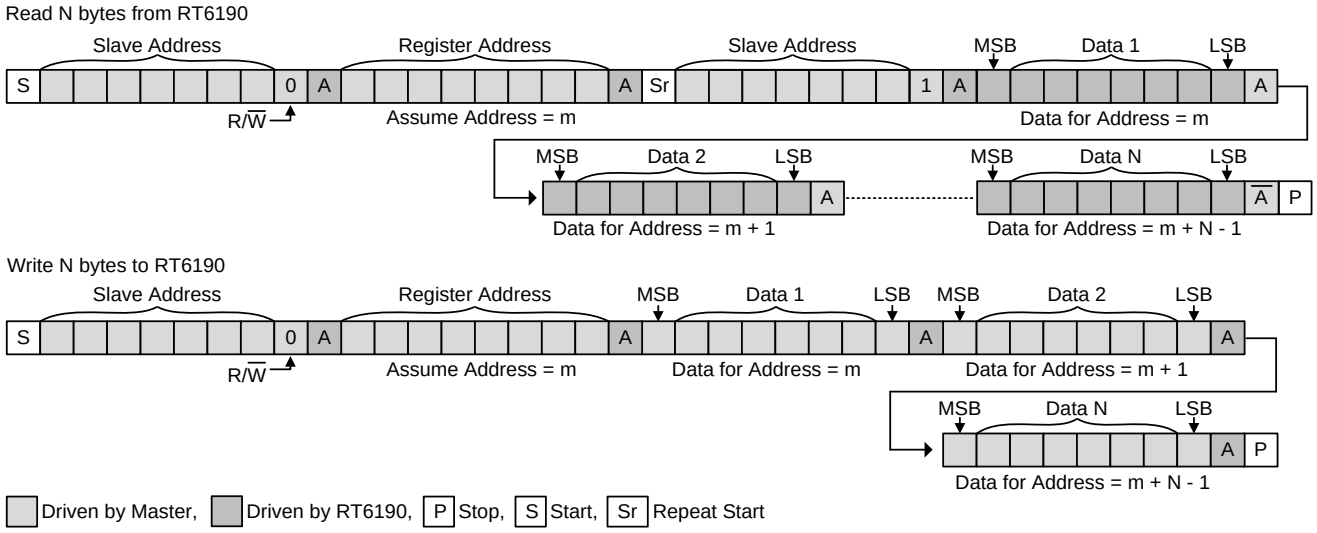


Figure 8. PCB Layout in Bottom Layer

I²C Interface

The RT6190 I²C slave address can be determined by ADDRESS pin. Connect ADDRESS pin to VDD selects 0x2D, and connect ADDRESS pin to AGND selects 0x2C. The RT6190 supports fast mode (bit rate up to 400kb/s), and the read or write bit stream (N ≥ 1) is shown as Figure 9.



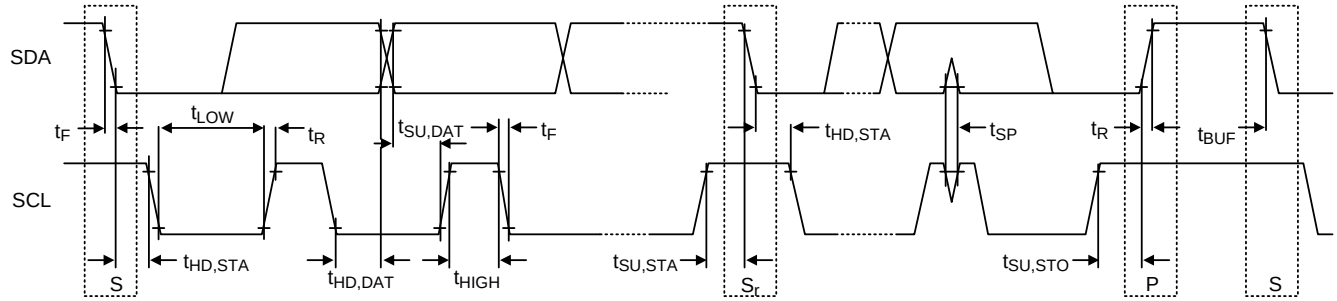


Figure 9. I²C Read/Write Bit Stream and Timing Diagram

Table 2. I²C Register Summary

Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x00	Manufacturer_ID	MANUFACTURER_ID								0x82
0x01	Output_CV	OUT_CV[7:0]								0x90
0x02		Reserved					OUT_CV[10:8]			0x01
0x03	Output_CC	OUT_CC[7:0]								0x59
0x04		Reserved							OUT_CC[8]	0x01
0x05	Input_CV	Reserved		IN_CV						0x00
0x06	Input_CC	IN_CC[7:0]								0xFF
0x07		Reserved							IN_CC[8]	0x01
0x08	Vref_SC	Reserved		VREF_SC						0x12
0x09	Vref_PSM	GAIN_VCOMP		VREF_PSM						0x6E
0x0A	Vref_POCP	Reserved		VREF_POCP						0x24
0x0B	OVP	Reserved		OVP_DELAY_INT_SET		OVP_DELAY_EXT_SET		OVP_LEVEL		0x12
0x0C	UVP	EN_IN_OVP	POWER_ROLE	UVP_DELAY_INT_SET		UVP_DELAY_EXT_SET		UVP_LEVEL		0x12
0x0D	Setting1	F_CCM	SLEWRATE_R		SLEWRATE_F		FSW			0x78
0x0E	Setting2	EN_PWM	DIS_INCV	DIS_INCC	EN_DISCHARGE	Reserved	IR_COMPR			0x10
0x0F	Setting3	DT_SEL		GM_EA		GAIN_ICS		GAIN_OCS		0x10
0x10	Setting4	ADC_AVG_SEL		I2C_SPEED	OCP4_TIME_X10	Reserved		EN_ADC	DRIVER_CHARGE	0x82
0x11	RATIO	SSP_EN	VIN_RATIO	VOUT_RATIO	Reserved	CHIP_VERSION				--
0x12	Output_Voltage	OUT_VOLTAGE[7:0]								0x00
0x13		Reserved					OUT_VOLTAGE[10:8]			0x00
0x14	Output_Current	OUT_CURRENT[7:0]								0x00
0x15		Reserved					OUT_CURRENT[10:8]			0x00
0x16	Input_Voltage	IN_VOLTAGE[7:0]								0x00
0x17		Reserved					IN_VOLTAGE[10:8]			0x00
0x18	Input_Current	IN_CURRENT[7:0]								0x00
0x19		Reserved					IN_CURRENT[10:8]			0x00

Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x1A	Temperature	TEMPERATURE[7:0]								0x00
0x1B		Reserved					TEMPERATURE[10:8]			0x00
0x1C	Status1	IN_OVP	OTP	INT_UVP	INT_OVP	EXT_UVP_C	EXT_OVP_C	EXT_UVP_A	EXT_OVP_A	0x00
0x1D	Status2	Reserved	PG	Reserved	CV_CC	OCP4	OCP3	OCP2	OCP1	0x10
0x1E	Alert1	ALERT_IN_OVP	ALERT_OTP	ALERT_INT_UVP	ALERT_INT_OVP	ALERT_EXT_UVP_C	ALERT_EXT_OVP_C	ALERT_EXT_UVP_A	ALERT_EXT_OVP_A	0x00
0x1F	Alert2	ALERT_OTP_R	ALERT_RAMP_PG	ALERT_TM1	ALERT_WDT	ALERT_OCP4	ALERT_OCP3	ALERT_OCP2	ALERT_OCP1	0x00
0x20	Mask1	M_ALERT_IN_OVP	M_ALERT_OTP	M_ALERT_INT_UVP	M_ALERT_INT_OVP	M_ALERT_EXT_UVP_C	M_ALERT_EXT_OVP_C	M_ALERT_EXT_UVP_A	M_ALERT_EXT_OVP_A	0xFF
0x21	Mask2	M_ALERT_OTP_R	M_ALERT_RAMP_PG	M_ALERT_TM1	M_ALERT_WDT	M_ALERT_OCP4	M_ALERT_OCP3	M_ALERT_OCP2	M_ALERT_OCP1	0xFF
0x22	OCP1_Setting	OCP1_SETTING								0x51
0x23	OCP2_Setting	OCP2_SETTING								0x64
0x24	OCP3_Setting	OCP3_SETTING								0xFF
0x25	OCP4_Setting	OCP4_SETTING								0xFF
0x26	OCP1 Delay Time	OCP1_TIME_LSB	OCP1_TIMING							0x0D
0x27	OCP2 Delay Time	OCP2_TIME_LSB	OCP2_TIMING							0x00
0x28	OCP Enable	OCP4_EN	OCP3_EN	OCP2_EN	OCP1_EN	OCP4_TIMING		OCP3_TIMING		0x30
0x29	Setting5	PROTECT_PATH_C	PROTECT_PATH_A	PROTECT_PATH_1	PATH_FLOATING	PATH_C_TYPE	PATH_A_TYPE	POWER_PATH_GC	POWER_PATH_GA	0x00
0x2A	Power Path OVP/UVP	Reserved				DIS_EXT_UVP_C	DIS_EXT_OVP_C	DIS_EXT_UVP_A	DIS_EXT_OVP_A	0x0F
0x2B	PPS	DIS_ALARM_LO	DIS_ALARM_HI	UVP_PPS	OVP_PPS	Reserved				0xC0
0x2C	VBUSC Alarm High Threshold	ALARM_HI[7:0]								0xFF
0x2D		Reserved					ALARM_HI[10:8]			0x07
0x2E	VBUSC Alarm Low Threshold	ALARM_LO[7:0]								0x00
0x2F		Reserved					ALARM_LO[10:8]			0x00

Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x30	Watchdog	Reserved	TIMER1_SEL			Reserved	WATCHDOG_SEL			0x00
0x32	VBUSC_ Voltage ADC	Reserved						VBUSC ADC	Reserved	0x00
0x33	VBUSC_ Voltage	VBUSC_VOLTAGE[7:0]								0x00
0x34		Reserved					VBUSC_VOLTAGE[10:8]			0x00
0x35	UVP_ Reference	UVP_REF								0x21
0x36	OVP_ Reference	OVP_REF								0xDC
0x37	Status3	Reserved			ALARM_ LO	ALARM_ HI	TO_ 275MS	IN_UVLO		0x00
0x38	Alert3	Reserved			ALERT_ ALARM_ LO	ALERT_ ALARM_ HI	ALERT_ TO_ 275MS	ALERT_ IN_UVL O_F	ALERT_ IN_UVL O_R	0x00
0x39	Mask3	Reserved			M_ALER T_ALAR M_LO	M_ALER T_ALAR M_HI	M_ALER T_TO_ 275MS	M_ALER T_IN_UV LO_F	M_ALER T_IN_UV LO_R	0x00

Table 3. I²C Register Map

Register Address	0x00		Register Name	Manufacturer_ID				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	0	0	1	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	MANUFACTURE_ID		MANUFACTURE_ID					

Register Address	0x01		Register Name	Output_CV				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	1	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OUT_CV[7:0]		Lower 8 bits of 11-bit OUT_CV[10:0] for output constant voltage (CV) setting. VOUT_CV = OUT_CV[10:0](Decimal) x ΔV (1) When 0x11[5] = 0, VOUT ratio = 0.08V/V： Range = 3V (0x0F0) to 21V (0x690) with ΔV = 12.5mV/step. (2) When 0x11[5] = 1, VOUT ratio = 0.05V/V： Range = 3V (0x096) to 32V (0x640) with ΔV = 20mV/step. (3) Default value = 0x190 with VOUT ratio = 0.08V/V for default VOUT = 5V.					

Register Address	0x02		Register Name	Output_CV				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	OUT_CV[10:8]		Upper 3 bits of 11-bit OUT_CV[10:0] for output constant voltage (CV) setting. Refer to 0x01 register for detail description.					

Register Address	0x03		Register Name	Output_CC				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	0	1	1	0	0	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OUT_CC[7:0]		Lower 8 bits of 9-bit OUT_CC[8:0] for output constant current (CC) setting. With output sense resistor = 10mΩ (R30 for Forward operation, and R29 for Reverse operation), the output CC can be set as: IOUT_CC = -0.15A + {OUT_CC[8:0](Decimal) x ΔI} (1) When 0x0F[1:0] = 00 (GAIN_OCS = 10x)： Range = 0.306A (0x013) to 12.114A (0x1FF) with ΔI = 24mA/step. (2) When 0x0F[1:0] = 01 (GAIN_OCS = 20x)： Range = 0.306A (0x026) to 5.982A (0x1FF) with ΔI = 12mA/step. (3) When 0x0F[1:0] = 10 (GAIN_OCS = 30x)： Range = 0.306A (0x039) to 3.938A (0x1FF) with ΔI = 8mA/step. (4) When 0x0F[1:0] = 11 (GAIN_OCS = 40x)： Range = 0.306A (0x04C) to 2.916A (0x1FF) with ΔI = 6mA/step. (5) Default value = 0x159 with 0x0F[1:0] = 00 (GAIN_OCS = 10x) for default output CC = 8.13A.						

Register Address	0x04		Register Name	Output_CC				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 1	Reserved		Reserved bits					
Bit 0	OUT_CC[8]		Upper 1 bit of 9-bit OUT_CC[8:0] for output constant current (CC) setting. Refer to 0x03 register for detail description.					

Register Address	0x05		Register Name	Input_CV				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6	Reserved		Reserved bits					
Bit 5 to Bit 0	IN_CV		Minimum input constant voltage (CV) setting. VIN_CV = IN_CV[5:0](Decimal) x ΔV (1) When 0x11[6] = 0, VIN ratio = 0.08V/V： Range = 0V (0x00) to 22.05V (0x3F) with ΔV = 350mV/step. (2) When 0x11[6] = 1, VIN ratio = 0.05V/V： Range = 0V (0x00) to 35.28V (0x3F) with ΔV = 560mV/step. (3) Default value = 0x00 with VIN ratio = 0.08V/V for default input CV = 0V.					

Register Address	0x06		Register Name	Input_CC				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	1	1	1	1	1	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IN_CC[7:0]		Lower 8 bits of 9-bit IN_CC[8:0] for input constant current (CC) setting. With input sense resistor = 10mΩ (R29 for Forward operation, and R30 for Reverse operation), the input CC can be set as: IIN_CC = -0.45A + {IN_CC[8:0](Decimal) x ΔI} (1) When 0x0F[3:2] = 00 (GAIN_ICS = 10x)： Range = 0.318A (0x020) to 11.814A (0x1FF) with ΔI = 24mA/step (2) When 0x0F[3:2] = 01 (GAIN_ICS = 20x)： Range = 0.318A (0x040) to 5.682A (0x1FF) with ΔI = 12mA/step. (3) When 0x0F[3:2] = 10 (GAIN_ICS = 30x)： Range = 0.318A (0x060) to 3.638A (0x1FF) with ΔI = 8mA/step. (4) When 0x0F[3:2] = 11 (GAIN_ICS = 40x)： Range = 0.318A (0x080) to 2.616A (0x1FF) with ΔI = 6mA/step. (5) Default value = 0x1FF with 0x0F[3:2] = 00 (GAIN_ICS = 10x) for default input CC = 11.814A.					

Register Address	0x07		Register Name	Input_CC				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	R	R	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 1	Reserved		Reserved bits					
Bit 0	IN_CC[8]		Upper 1 bit of 9-bit IN_CC[8:0] for input constant current (CC) setting. Refer to 0x06 register for detail description.					

Register Address	0x08		Register Name	Vref_SC				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	0	1	0
Read/Write	R	R	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6	Reserved		Reserved bits					
Bit 5 to Bit 0	VREF_SC		Slope compensation ramp setting for internal use.					

Register Address	0x09		Register Name	Vref_PSM				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	1	0	1	1	1	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6	GAIN_VCOMP		Vcomp gain setting for internal use.					
Bit 5 to Bit 0	VREF_PSM		Minimum peak current setting of TON in PSM for internal use.					

Register Address	0x0A		Register Name	Vref_POCP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	1	0	0	1	0	0
Read/Write	R	R	RW	RW	RW	RW	RW	RW

Bits	Name	Description
Bit 7 to Bit 6	Reserved	Reserved bits
Bit 5 to Bit 0	VREF_POCP	Input peak current limit setting. With input sense resistor = 10mΩ (R29 for Forward operation, and R30 for Reverse operation), the input peak current limit can be set as : I_{POCP} = [0x0A[5:0](Decimal) x 0.4A] - 1.169A. (1) Range = 5.231A (0x10) to 24.031A (0x3F). (2) Default value = 0x24 for default I_{POCP} =13.231A.

Register Address	0x0B		Register Name	OVP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	0	1	0
Read/Write	R	R	RW	RW	RW	RW	RW	RW

Bits	Name	Description
Bit 7 to Bit 6	Reserved	Reserved bits
Bit 5 to Bit 4	OVP_DELAY_INT_SET	OVP delay time setting for output voltage. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 00：96μs　　10：288μs 01：192μs (Default)　　11：386μs
Bit 3 to Bit 2	OVP_DELAY_EXT_SET	OVP delay time setting for VBUSC and VBUSA pins. 00：8μs (Default)　　10：32μs 01：16μs　　11：64μs
Bit 1 to Bit 0	OVP_LEVEL	OVP threshold setting. 00：Reserved　　10：120% (Default) 01：115%　　11：125%

Register Address	0x0C		Register Name	UVP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	0	1	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
Bit 7	EN_IN_OVP	Enable or disable input OVP function. (Trip level = 27V): 0：Disable 1：Enable
Bit 6	POWER_ROLE	Forward or Reverse operation selection. 0：Forward operation 1：Reverse operation Note: This register "Only" can be set when 0x0E[7] = 0.
Bit 5 to Bit 4	UVP_DELAY_INT_SET	UVP delay time setting for output voltage. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 00：256μs 10：768μs 01：512μs (Default) 11：1024μs
Bit 3 to Bit 2	UVP_DELAY_EXT_SET	UVP delay time setting for VBUSC and VBUSA pins. 00：32μs (Default) 10：128μs 01：64μs 11：256μs
Bit 1 to Bit 0	UVP_LEVEL	UVP threshold setting. 00：50% 10：70% (Default) 01：60% 11：80%

Register Address	0x0D		Register Name	Setting1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	1	1	1	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
Bit 7	F_CCM	Operation mode setting. 0：Light load PSM 1：Force CCM
Bit 6 to Bit 5	SLEWRATE_R	Rising slew rate setting for DVS up. (1) For 0x11[5] = 0, VOUT ratio = 0.08V/V, ΔVOUT = 12.5mV/step. (2) For 0x11[5] = 1, VOUT ratio = 0.05V/V, ΔVOUT = 20mV/step. 00：Slew rate = ΔVOUT/4μs 10：Slew rate = ΔVOUT/16μs 01：Slew rate = ΔVOUT/8μs 11：Slew rate = ΔVOUT/32μs (Default)
Bit 4 to Bit 3	SLEWRATE_F	Falling slew rate setting for DVS down. (1) For 0x11[5] = 0, VOUT ratio = 0.08V/V, ΔVOUT = 12.5mV/step. (2) For 0x11[5] = 1, VOUT ratio = 0.05V/V, ΔVOUT = 20mV/step. 00：Slew rate = ΔVOUT/4μs 10：Slew rate = ΔVOUT/16μs 01：Slew rate = ΔVOUT/8μs 11：Slew rate = ΔVOUT/32μs (Default)
Bit 2 to Bit 0	FSW	Switching frequency setting. 000：250kHz (Default) 100：615kHz 001：325kHz 101：730kHz 010：400kHz 110：845kHz 011：500kHz 111：960kHz

Register Address	0x0E		Register Name	Setting2				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	0	0	0
Read/Write	RW	RW	RW	RW	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	EN_PWM		Enable or disable RT6190. 0：Disable 1：Enable					
Bit 6	DIS_INCV		Enable or disable input CV loop to ignore IN_CV setting. 0：Enable 1：Disable					
Bit 5	DIS_INCC		Enable or disable input CC loop to ignore IN_CC setting. 0：Enable 1：Disable					
Bit 4	EN_DISCHARGE		Enable or disable the output discharge resistor when turn off by I2C or in DVS down operation. 0：Disable 1：Enable					
Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	IR_COMPR		Cable voltage drop compensation setting: 000：Disable (Default) 100：80mΩ 001：10mΩ 101：120mΩ 010：20mΩ 110：160mΩ 011：40mΩ 111：200mΩ					

Register Address	0x0F		Register Name	Setting3				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6	DT_SEL		Dead time setting. 00：30ns (Default) 10：70ns 01：50ns 11：90ns					
Bit 5 to Bit 4	GM_EA		Error amplifier gain setting. 00：275μA/V 10：825μA/V 01：550μA/V (Default) 11：1100μA/V					
Bit 3 to Bit 2	GAIN_ICS		Input average current sense gain setting. 00：10x (Default) 10：30x 01：20x 11：40x					
Bit 1 to Bit 0	GAIN_OCS		Output average current sense gain setting. 00：10x (Default) 10：30x 01：20x 11：40x					

Register Address	0x10		Register Name	Setting4				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	0	0	0	0	0	1	0
Read/Write	RW	RW	RW	RW	R	R	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 6	ADC_AVG_SEL		Average times of ADC function. 00：2 times 10：8 times (Default) 01：4 times 11：16 times					
Bit 5	I2C_SPEED		I2C speed selection. 0：Bit rate = 300kHz. 1：Bit rate = 1MHz/3.4MHz.					
Bit 4	OCP4_TIME_X10		OCP4 delay time ratio. 0: x 1 1: x 10					
Bit 3 to Bit 2	Reserved		Reserved bits					
Bit 1	EN_ADC		Enable or disable ADC function for 0x12 to 0x1B registers. 0：Disable 1：Enable					
Bit 0	DRIVER_CHARGE		Enable or disable driver charge function. 0：Disable 1：Enable					

Register Address	0x11		Register Name	RATIO				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	--	--	--	--
Read/Write	RW	RW	RW	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7	SSP_EN		Enable or disable spread spectrum function. 0：Disable 1：Enable					
Bit 6	VIN_RATIO		VIN ratio selection for input voltage setting range. 0：0.08V/V 1：0.05V/V Note: This register "Only" can be set when 0x0E[7] = 0.					
Bit 5	VOUT_RATIO		VOUT ratio selection for output voltage setting range. 0：0.08V/V 1：0.05V/V Note: This register "Only" can be set when 0x0E[7] = 0.					
Bit 4	Reserved		Reserved bits					
Bit 3 to Bit 0	CHIP_VERSION		CHIP_VERSION					

Register Address	0x12		Register Name	Output_Voltage				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OUT_VOLTAGE[7:0]		Lower 8 bits of 11-bit OUT_VOLTAGE[10:0] for output voltage reporting. VOUT Reporting = OUT_VOLTAGE[10:0](Decimal) x ΔV (1) When 0x11[5] = 0, VOUT ratio = 0.08V/V： Range = 3V (0x0F0) to 25.5875V (0x7FF) with ΔV = 12.5mV/step. (2) When 0x11[5] = 1, VOUT ratio = 0.05V/V： Range = 3V (0x096) to 36V (0x708) with ΔV = 20mV/step.					

Register Address	0x13		Register Name	Output_Voltage				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	OUT_VOLTAGE[10:8]		Upper 3 bits of 11-bit OUT_VOLTAGE[10:0] for output voltage reporting. Refer to 0x12 register for detail description.					

Register Address	0x14		Register Name	Output_Current				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OUT_CURRENT[7:0]		Lower 8 bits of 11-bit OUT_CURRENT[10:0] for output average current reporting. With output sense resistor = 10mΩ (R30 for Forward operation, and R29 for Reverse operation), the output average current can be read as below: IOUT Reporting = -0.15A + {OUT_CURRENT[10:0](Decimal) x ΔI} (1) When 0x0F[1:0] = 00 (GAIN_OCS = 10x): Range = 0.0036A (0x00F) to 20.811A (0x7FF) with ΔI = 10.24mA/step (2) When 0x0F[1:0] = 01 (GAIN_OCS = 20x): Range = 0.0036A (0x01E) to 10.33A (0x7FF) with ΔI = 5.12mA/step (3) When 0x0F[1:0] = 10 (GAIN_OCS = 30x): Range = 0.0036A (0x02D) to 6.837A (0x7FF) with ΔI = 3.413mA/step (4) When 0x0F[1:0] = 11 (GAIN_OCS = 40x): Range = 0.0036A (0x03C) to 5.09A (0x7FF) with ΔI = 2.56mA/step					

Register Address	0x15		Register Name	Output_Current				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	OUT_CURRENT[10:8]		Upper 3 bits of 11-bit OUT_CURRENT[10:0] for output average current reporting. Refer to 0x14 register for detail description.					

Register Address	0x16		Register Name	Input_Voltage				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IN_VOLTAGE[7:0]		Lower 8 bits of 11-bit IN_VOLTAGE[10:0] for input voltage reporting. VIN Reporting = IN_VOLTAGE[10:0](Decimal) x ΔV (1) When 0x11[6] = 0, VIN ratio = 0.08V/V： Range = 3V (0x0F0) to 25.5875V (0x7FF) with ΔV = 12.5mV/step. (2) When 0x11[6] = 1, VIN ratio = 0.05V/V： Range = 3V (0x096) to 36V (0x708) with ΔV = 20mV/step.					

Register Address	0x17		Register Name	Input_Voltage				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	IN_VOLTAGE[10:8]		Upper 3 bits of 11-bit IN_VOLTAGE[10:0] for input voltage reporting. Refer to 0x16 register for detail description.					

Register Address	0x18		Register Name	Input_Current				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	IN_CURRENT[7:0]		Lower 8 bits of 11-bit IN_CURRENT[10:0] for input average current reporting. With input sense resistor = 10mΩ (R29 for forward operation, and R30 for reverse operation), the input average current can be read as below: IIN Reporting = -0.45A + {IN_CURRENT[10:0](Decimal) x ΔI} (1) When 0x0F[3:2] = 00 (GAIN_ICS = 10x): Range = 0.0108A (0x02D) to 20.511A (0x7FF) with ΔI = 10.24mA/step (2) When 0x0F[3:2] = 01 (GAIN_ICS = 20x): Range = 0.0108A (0x05A) to 10.03A (0x7FF) with ΔI = 5.12mA/step (3) When 0x0F[3:2] = 10 (GAIN_ICS = 30x): Range = 0.0108A (0x087) to 6.537A (0x7FF) with ΔI = 3.413mA/step (4) When 0x0F[3:2] = 11 (GAIN_ICS = 40x): Range = 0.0108A (0x0B4) to 4.79A (0x7FF) with ΔI = 2.56mA/step						

Register Address	0x19		Register Name	Input_Current				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	IN_CURRENT[10:8]		Upper 3 bits of 11-bit IN_CURRENT[10:0] for input average current reporting. Refer to 0x18 register for detail description.					

Register Address	0x1A		Register Name	Temperature				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	TEMPERATURE[7:0]		Lower 8 bits of 11-bit TEMPERATURE[10:0] for temperature reporting. The 11-bit TEMPERATURE[10:0] is used for external thermal sense by recording TSEN pin voltage. The temperature reporting range is from 0V to 2V with 1mV/step.					

Register Address	0x1B		Register Name	Temperature				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	TEMPERATURE[7:0]		Upper 3 bits of 11-bit TEMPERATURE[10:0] for temperature reporting. Refer to 0x1A register for detail description.					

Register Address	0x1C		Register Name	Status1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7	IN_OVP		OVP indicator for input voltage. (Input voltage : VIN pin for Forward, VOUT pin for Reverse) 0：No fault 1：Fault					
Bit 6	OTP		OTP indicator. 0：No fault 1：Fault					
Bit 5	INT_UVP		UVP indicator for output voltage. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：No fault 1：Fault					
Bit 4	INT_OVP		OVP indicator for output voltage. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：No fault 1：Fault					
Bit 3	EXT_UVP_C		UVP indicator for VBUSC pin. 0：No fault 1：Fault					
Bit 2	EXT_OVP_C		OVP indicator for VBUSC pin. 0：No fault 1：Fault					
Bit 1	EXT_UVP_A		UVP indicator for VBUSA pin. 0：No fault 1：Fault					
Bit 0	EXT_OVP_A		OVP indicator for VBUSA pin. 0：No fault 1：Fault					

Register Address	0x1D		Register Name	Status2				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	1	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7, Bit 5	Reserved		Reserved bits					
Bit 6	PG		Power good status indicator. 0：Output Voltage < 85% of setting or ≥ OVP trip threshold. 1：OVP trip threshold > Output Voltage ≥ 90% of setting. (Output voltage : VOUT pin for Forward, VIN pin for Reverse)					
Bit 4	CV_CC		Indicator for constant voltage (CV) and constant current (CC). 0：CV mode. 1：CC mode. Note: This bit will be active when 0x0E[7] = 1.					
Bit 3	OCP4		OCP4 indicator. 0：No fault 1：Fault This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) {IN_CURRENT[10:3] (Register 0x18/0x19) - OUT_CURRENT[10:3] (Register 0x14/0x15)} > OCP4_SETTING[7:0] (Register 0x25) with OCP4 Delay Time (Register 0x28[3:2]).					
Bit 2	OCP3		OCP3 indicator. 0：No fault 1：Fault This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) OUT_CURRENT[10:3] (Register 0x14/0x15) > OCP3_SETTING[7:0] (Register 0x24) with OCP3 Delay Time (Register 0x28[1:0]).					
Bit 1	OCP2		OCP2 indicator. 0：No fault 1：Fault This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) OUT_CURRENT[10:3] (Register 0x14/0x15) > OCP2_SETTING[7:0] (Register 0x23) with OCP2 Delay Time (Register 0x27).					
Bit 0	OCP1		OCP1 indicator. 0：No fault 1：Fault This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) OUT_CURRENT[10:3] (Register 0x14/0x15) > OCP1_SETTING[7:0] (Register 0x22) with OCP1 Delay Time (Register 0x26).					

Register Address	0x1E		Register Name	Alert1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
Bit 7	ALERT_IN_OVP	Internal flag to detect input voltage OVP. (Input voltage : VIN pin for Forward, VOUT pin for Reverse) 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: When input OVP fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 6	ALERT_OTP	Internal flag to detect OTP. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: After OTP fault condition is detected, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 5	ALERT_INT_UVP	Internal flag to detect output voltage UVP. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: When output UVP fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 4	ALERT_INT_OVP	Internal flag to detect output voltage OVP. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: When output OVP fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 3	ALERT_EXT_UVP_C	Internal flag to detect VBUSC UVP. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: When VBUSC UVP fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 2	ALERT_EXT_OVP_C	Internal flag to detect VBUSC OVP. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: When VBUSC OVP fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 1	ALERT_EXT_UVP_A	Internal flag to detect VBUSA UVP. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: When VBUSA UVP fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 0	ALERT_EXT_OVP_A	Internal flag to detect VBUSA OVP. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. Note: When VBUSA OVP fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.

Register Address	0x1F		Register Name	Alert2				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	ALERT_OTP_R		Internal flag to detect OTP recovery after OTP happened. 0：OTP not recovery. ALERT pin keeps low level. 1：OTP recovery. ALERT pin goes to high level. Note: After OTP recovery condition is detected, this bit can be changed to default setting "0" by writing this bit to "1" only.					
Bit 6	ALERT_RAMP_PG		Internal flag to detect output voltage status. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：ALERT pin keeps high level. (1) Power off: Output Voltage < 85% of setting. (2) Normal: OVP trip threshold > Output Voltage ≥ 90% of setting. (3) DVS: Output Voltage not reach to target level. 1：ALERT pin becomes low level. (1) Power on: After 0x0E[7] from 0 to 1, Output Voltage ≥ 90% of setting. (2) Normal: Output Voltage < 85% of setting or ≥ OVP trip threshold. (3) DVS: Output Voltage reach to target level. Note: After this bit = 1, this bit can be changed to default setting "0" by writing this bit to "1" only.					
Bit 5	ALERT_TM1		Internal flag to detect Timer1 status. 0：Timer1 is disabled and ALERT pin keeps high level. Timer1 will begin to count if 0x30[6:4] ≠ 000, and ALERT pin keeps high level if Timer1 is still counting. 1：Timer1 timeout completed. ALERT pin goes to low level. Note: After Timer1 finished counting, this bit can be changed to default setting "0" by writing this bit to "1" only.					
Bit 4	ALERT_WDT		Internal flag to detect watchdog timer status. 0：Watchdog is disabled and ALERT pin keeps high level. Watchdog will begin to count if 0x30[2:0] ≠ 000, and ALERT pin goes to low level. 1：Watchdog timeout completed. ALERT will keep low level and RT6190 will be reset to default setting including all I2C registers except 0x1F[4] and 0x30. Note: After watchdog timer finished counting, this bit can be changed to default setting "0" by writing this bit to "1" only.					
Bit 3	ALERT_OCP4		Internal flag to detect OCP4. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) {IN_CURRENT[10:3] (Register 0x18/0x19) - OUT_CURRENT[10:3] (Register 0x14/0x15)} > OCP4_SETTING[7:0] (Register 0x25) with OCP4 Delay Time (Register 0x28[3:2]). Note: When OCP4 fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.					

Bits	Name	Description
Bit 2	ALERT_OCP3	Internal flag to detect OCP3. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) OUT_CURRENT[10:3] (Register 0x14/0x15) > OCP3_SETTING[7:0] (Register 0x24) with OCP3 Delay Time (Register 0x28[1:0]). Note: When OCP3 fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 1	ALERT_OCP2	Internal flag to detect OCP2. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) OUT_CURRENT[10:3] (Register 0x14/0x15) > OCP2_SETTING[7:0] (Register 0x23) with OCP2 Delay Time (Register 0x27). Note: When OCP2 fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.
Bit 0	ALERT_OCP1	Internal flag to detect OCP1. 0：No fault. ALERT pin keeps high level. 1：Fault. ALERT pin goes to low level. This bit will be changed to 1 only when: (1) ADC function is enabled (0x10[1] = 1). (2) OUT_CURRENT[10:3] (Register 0x14/0x15) > OCP1_SETTING[7:0] (Register 0x22) with OCP1 Delay Time (Register 0x26). Note: When OCP1 fault condition is removed, this bit can be changed to default setting "0" by writing this bit to "1" only.

Register Address	0x20		Register Name	Mask1				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	1	1	1	1	1	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	M_ALERT_IN_OVP		Mask internal flag output of input voltage OVP to ALERT pin. (Input voltage : VIN pin for Forward, VOUT pin for Reverse) 0：Mask 1：Not mask					
Bit 6	M_ALERT_OTP		Mask internal flag output of OTP to ALERT pin. 0：Mask 1：Not mask					
Bit 5	M_ALERT_INT_UVP		Mask internal flag output of output voltage UVP to ALERT pin. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：Mask 1：Not mask					
Bit 4	M_ALERT_INT_OVP		Mask internal flag output of output voltage OVP to ALERT pin. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：Mask 1：Not mask					
Bit 3	M_ALERT_EXT_ UVP_C		Mask internal flag output of VBUSC UVP to ALERT pin. 0：Mask 1：Not mask					
Bit 2	M_ALERT_EXT_ OVP_C		Mask internal flag output of VBUSC OVP to ALERT pin. 0：Mask 1：Not mask					
Bit 1	M_ALERT_EXT_ UVP_A		Mask internal flag output of VBUSA UVP to ALERT pin. 0：Mask 1：Not mask					
Bit 0	M_ALERT_EXT_ OVP_A		Mask internal flag output of VBUSA OVP to ALERT pin. 0：Mask 1：Not mask					

Register Address	0x21		Register Name	Mask2				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	1	1	1	1	1	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	M_ALERT_OTP_R		Mask internal flag output of OTP recovery to ALERT pin. 0：Mask 1：Not mask					
Bit 6	M_ALERT_RAMP_PG		Mask internal flag output of output voltage status to ALERT pin. (Output voltage : VOUT pin for Forward, VIN pin for Reverse) 0：Mask 1：Not mask					
Bit 5	M_ALERT_TM1		Mask internal flag output of Timer1 to ALERT pin. 0：Mask 1：Not mask					
Bit 4	M_ALERT_WDT		Mask internal flag output of watchdog timer to ALERT pin. 0：Mask 1：Not mask					
Bit 3	M_ALERT_OCP4		Mask internal flag output of OCP4 to ALERT pin. 0：Mask 1：Not mask					
Bit 2	M_ALERT_OCP3		Mask internal flag output of OCP3 to ALERT pin. 0：Mask 1：Not mask					
Bit 1	M_ALERT_OCP2		Mask internal flag output of OCP2 to ALERT pin. 0：Mask 1：Not mask					
Bit 0	M_ALERT_OCP1		Mask internal flag output of OCP1 to ALERT pin. 0：Mask 1：Not mask					

Register Address	0x22		Register Name	OCP1_Setting				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	0	1	0	0	0	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OCP1_SETTING		With output sense resistor = 10mΩ (R30 for forward operation, and R29 for reverse operation), the OCP1 can be set as below: OCP1 = -0.15A + OCP1_SETTING[7:0](Decimal) x ΔI (1) When 0x0F[1:0] = 00 (GAIN_OCS = 10x): Range = 0.3415A (0x06) to 20.7396A (0xFF) with ΔI = 81.92mA/step. (2) When 0x0F[1:0] = 01 (GAIN_OCS = 20x): Range = 0.3415A (0x0C) to 10.2948A (0xFF) with ΔI = 40.96mA/step. (3) When 0x0F[1:0] = 10 (GAIN_OCS = 30x): Range = 0.3415A (0x12) to 6.8132A (0xFF) with ΔI = 27.307mA/step. (4) When 0x0F[1:0] = 11 (GAIN_OCS = 40x): Range = 0.3415A (0x18) to 5.0724A (0xFF) with ΔI = 20.48mA/step. (5) Default value = 0x51 with 0x0F[1:0] = 00 (GAIN_OCS = 10x) for default OCP1 = 6.4855A.					

Register Address	0x23		Register Name	OCP2_Setting				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	1	1	0	0	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OCP2_SETTING		With output sense resistor = 10mΩ (R30 for forward operation, and R29 for reverse operation), the OCP2 can be set as below: OCP2 = -0.15A + OCP2_SETTING[7:0](Decimal) x ΔI (1) When 0x0F[1:0] = 00 (GAIN_OCS = 10x): Range = 0.3415A (0x06) to 20.7396A (0xFF) with ΔI = 81.92mA/step. (2) When 0x0F[1:0] = 01 (GAIN_OCS = 20x): Range = 0.3415A (0x0C) to 10.2948A (0xFF) with ΔI = 40.96mA/step. (3) When 0x0F[1:0] = 10 (GAIN_OCS = 30x): Range = 0.3415A (0x12) to 6.8132A (0xFF) with ΔI = 27.307mA/step. (4) When 0x0F[1:0] = 11 (GAIN_OCS = 40x): Range = 0.3415A (0x18) to 5.0724A (0xFF) with ΔI = 20.48mA/step. (5) Default value = 0x64 with 0x0F[1:0] = 00 (GAIN_OCS = 10x) for default OCP2 = 8.042A.					

Register Address	0x24		Register Name	OCP3_Setting				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	1	1	1	1	1	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OCP3_SETTING		With output sense resistor = 10mΩ (R30 for forward operation, and R29 for reverse operation), the OCP3 can be set as below: OCP3 = -0.15A + OCP3_SETTING[7:0](Decimal) x ΔI (1) When 0x0F[1:0] = 00 (GAIN_OCS = 10x): Range = 0.3415A (0x06) to 20.7396A (0xFF) with ΔI = 81.92mA/step. (2) When 0x0F[1:0] = 01 (GAIN_OCS = 20x): Range = 0.3415A (0x0C) to 10.2948A (0xFF) with ΔI = 40.96mA/step. (3) When 0x0F[1:0] = 10 (GAIN_OCS = 30x): Range = 0.3415A (0x12) to 6.8132A (0xFF) with ΔI = 27.307mA/step. (4) When 0x0F[1:0] = 11 (GAIN_OCS = 40x): Range = 0.3415A (0x18) to 5.0724A (0xFF) with ΔI = 20.48mA/step. (5) Default value = 0xFF with 0x0F[1:0] = 00 (GAIN_OCS = 10x) for default OCP3 = 20.7396A.					

Register Address	0x25		Register Name	OCP4_Setting				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	1	1	1	1	1	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OCP4_SETTING		Short output sense resistor and with input sense resistor = 10mΩ (R29 for forward operation, and R30 for reverse operation), the OCP4 can be set as below: OCP4 = -0.3A + {OCP4_SETTING[7:0](Decimal) + 1} x ΔI (1) When 0x0F[3:2] = 00 (GAIN_ICS = 10x): Range = 0.3554A (0x07) to 20.6715A (0xFF) with ΔI = 81.92mA/step. (2) When 0x0F[3:2] = 01 (GAIN_ICS = 20x): Range = 0.3554A (0x0F) to 10.1858A (0xFF) with ΔI = 40.96mA/step. (3) When 0x0F[3:2] = 10 (GAIN_ICS = 30x): Range = 0.3554A (0x17) to 6.6905A (0xFF) with ΔI = 27.307mA/step. (4) When 0x0F[3:2] = 11 (GAIN_ICS = 40x): Range = 0.3554A (0x1F) to 4.9429A (0xFF) with ΔI = 20.48mA/step. (5) Default value = 0xFF with 0x0F[3:2] = 00 (GAIN_ICS = 10x) fordefault OCP4 = 20.6715A.					

Register Address	0x26		Register Name	OCP1 Delay Time				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	1	1	0	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	OCP1_TIME_LSB		Time step selection for OCP1 delay time: 0：8ms 1：32ms					
Bit 6 to Bit 0	OCP1_TIMING		With 0x26[7], OCP1 delay time can be set as below: OCP1 Delay Time = OCP1_TIMING[6:0](Decimal) x Δt (1) When 0x26[7] = 0： Range = 0ms (0x00) to 1.016s (0x7F) with Δt = 8ms/step. (2) When 0x26[7] = 1： Range = 0ms (0x80) to 4.064s (0xFF) with Δt = 32ms/step. (3) Default value = 0x0D for default OCP1 delay time = 104ms.					

Register Address	0x27		Register Name	OCP2 Delay Time				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	OCP2_TIME_LSB		Time step selection for OCP2 delay time: 0：8ms 1：32ms					
Bit 6 to Bit 0	OCP2_TIMING		With 0x27[7], OCP2 delay time can be set as below: OCP2 Delay Time = OCP2_TIMING[6:0](Decimal) x Δt (1) When 0x27[7] = 0： Range = 0ms (0x00) to 1.016s (0x7F) with Δt = 8ms/step. (2) When 0x27[7] = 1： Range = 0ms (0x80) to 4.064s (0xFF) with Δt = 32ms/step. (3) Default value = 0x00 for default OCP2 delay time = 0ms.					

Register Address	0x28		Register Name	OCP Enable				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	1	1	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	OCP4_EN		Enable or disable OCP4. 0：Disable 1：Enable					
Bit 6	OCP3_EN		Enable or disable OCP3. 0：Disable 1：Enable					
Bit 5	OCP2_EN		Enable or disable OCP2. 0：Disable 1：Enable					
Bit 4	OCP1_EN		Enable or disable OCP1. 0：Disable 1：Enable					
Bit 3 to Bit 2	OCP4_TIMING		OCP4 delay time setting: 00：50ms 01：100ms 10：200ms 11：400ms					
Bit 1 to Bit 0	OCP3_TIMING		OCP3 delay time setting: 00：0ms 01：5ms 10：10ms 11：20ms					

Register Address	0x29		Register Name	Setting5				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7	PROTECT_PATH_C		Power path C status when fault happens on power path A. 0：Turn off power path C by GPC. 1：Remain original status of power path C.					
Bit 6	PROTECT_PATH_A		Power path A status when fault happens on power path C. 0：Turn off power path A by GPA. 1：Remain original status of power path A.					
Bit 5	PROTECT_PATH_1		All power path status when fault happens. 0：Turn off each power path by GPC and GPA. 1：Remain original status of each power path.					
Bit 4	PATH_FLOATING		All power path status. 0：Keep original status. 1：Floating all power path by making GPC and GPA to tri-state.					
Bit 3	PATH_C_TYPE		External MOS type for power path C. 0：N-MOS 1：P-MOS					
Bit 2	PATH_A_TYPE		External MOS type for power path A. 0：N-MOS 1：P-MOS					
Bit 1	POWER_PATH_GC		Enable or disable GPC pin. 0：Disable 1：Enable					
Bit 0	POWER_PATH_GA		Enable or disable GPA pin. 0：Disable 1：Enable					

Register Address	0x2A		Register Name	Power Path OVP/UVP				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	1	1	1	1
Read/Write	R	R	R	R	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 4	Reserved		Reserved bits					
Bit 3	DIS_EXT_UVP_C		Disable VBUSC UVP. 0：Enable 1：Disable					
Bit 2	DIS_EXT_OVP_C		Disable VBUSC OVP. 0：Enable 1：Disable					
Bit 1	DIS_EXT_UVP_A		Disable VBUSA UVP. 0：Enable 1：Disable					
Bit 0	DIS_EXT_OVP_A		Disable VBUSA OVP. 0：Enable 1：Disable					

Register Address	0x2B		Register Name	PPS				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	R	R	R	R
Bits	**Name**		**Description**					
Bit 7	DIS_ALARM_LO		Disable VBUSC alarm low detection. 0：Enable 1：Disable					
Bit 6	DIS_ALARM_HI		Disable VBUSC alarm high detection. 0：Enable 1：Disable					
Bit 5	UVP_PPS		UVP threshold control bit. 0：Keep UVP_LEVEL (0x0C[1:0]) setting. 1：Follow UVP_REF (0x35[7:0]) setting.					
Bit 4	OVP_PPS		OVP threshold control bit. 0：Keep OVP_LEVEL (0x0B[1:0]) setting. 1：Follow OVP_REF (0x36[7:0]) setting.					
Bit 3 to Bit 0	Reserved		Reserved bits					

Register Address	0x2C		Register Name	VBUSC Alarm High Threshold				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	1	1	1	1	1	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	ALARM_HI[7:0]		Lower 8 bits of 11-bit ALARM_HI[10:0] for VBUSC Alarm High threshold setting. VBUSC Alarm Hi = ALARM_HI[10:0](Decimal) x ΔV (1) When 0x11[5] = 0, VOUT ratio = 0.08V/V： Range = 3V (0x0F0) to 25.5875V (0x7FF) with ΔV = 12.5mV/step. (2) When 0x11[5] = 1, VOUT ratio = 0.05V/V： Range = 3V (0x096) to 36V (0x708) with ΔV = 20mV/step. (3) Default value = 0x7FF with VOUT ratio = 0.08V/V for default VBUSC Alarm High threshold = 25.5875V.					

Register Address	0x2D		Register Name	VBUSC Alarm High Threshold				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	ALARM_HI[10:8]		Upper 3 bits of 11-bit ALARM_HI[10:0] for VBUSC Alarm High threshold setting. Refer to 0x2C register for detail description.					

Register Address	0x2E		Register Name	VBUSC Alarm Low Threshold				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	ALARM_LO[7:0]		Lower 8 bits of 11-bit ALARM_LO[10:0] for VBUSC Alarm Low threshold setting. VBUSC Alarm Lo = ALARM_LO[10:0](Decimal) x ΔV (1) When 0x11[5] = 0, VOUT ratio = 0.08V/V： Range = 3V (0x0F0) to 25.5875V (0x7FF) with ΔV = 12.5mV/step. (2) When 0x11[5] = 1, VOUT ratio = 0.05V/V： Range = 3V (0x096) to 36V (0x708) with ΔV = 20mV/step. (3) Default value = 0x000 with VOUT ratio = 0.08V/V for default VBUSC Alarm Low threshold = 0V.					

Register Address	0x2F		Register Name	VBUSC Alarm Low Threshold				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	ALARM_LO[10:8]		Upper 3 bits of 11-bit ALARM_LO[10:0] for VBUSC Alarm Low threshold setting. Refer to 0x2E register for detail description.					

Register Address	0x30		Register Name	Watchdog				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	RW	RW	RW	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7, Bit 3	Reserved		Reserved bits					
Bit 6 to Bit 4	TIMER1_SEL		Timer1 timeout setting. The ALERT pin will go low when Timer1 finished counting. 000：Disable (Default) 100：3s 001：0.5s 101：4s 010：1s 110：6s 011：2s 111：8s					
Bit 2 to Bit 0	WATCHDOG_SEL		Watchdog timeout setting. Watchdog timer will start counting if ALERT pin goes low, and it will be reset by I2C access. 000：Disable (Default) 100：3s 001：0.5s 101：4s 010：1s 110：6s 011：2s 111：8s					

Register Address	0x32		Register Name	VBUSC_Voltage ADC				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	RW	R
Bits	**Name**		**Description**					
Bit 7 to Bit 2 Bit 0	Reserved		Reserved bits					
Bit 1	VBUSC ADC		Enable ADC function for VBUSC Voltage. 0 : Disable 1 : Enable					

Register Address	0x33		Register Name	VBUSC_Voltage				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 0	VBUSC_VOLTAGE[7:0]		Lower 8 bits of 11-bit VBUSC_VOLTAGE[10:0] for VBUSC voltage reporting. VBUSC Reporting = VBUSC_VOLTAGE[10:0](Decimal) x ΔV (1) When 0x11[5] = 0, VOUT ratio = 0.08V/V： Range = 3V (0x0F0) to 25.5875V (0x7FF) with ΔV = 12.5mV/step. (2) When 0x11[5] = 1, VOUT ratio = 0.05V/V： Range = 3V (0x096) to 36V (0x708) with ΔV = 20mV/step.					

Register Address	0x34		Register Name	VBUSC_Voltage				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	1
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 3	Reserved		Reserved bits					
Bit 2 to Bit 0	VBUSC_VOLTAGE [10:8]		Upper 3 bits of 11-bit VBUSC_VOLTAGE[10:0] for VBUSC voltage reporting. Refer to 0x33 register for detail description.					

Register Address	0x35		Register Name	UVP_Reference				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	1	0	0	0	0	1
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	UVP_REF		When 0x2B[5] = 1, UVP threshold can be adjusted independent as below: UVP = UVP_REF[7:0](Decimal) x ΔV (1) When 0x11[5] = 0, VOUT ratio = 0.08V/V： Range = 0V (0x00) to 25.5V (0xFF) with ΔV = 0.1V/step. (2) When 0x11[5] = 1, VOUT ratio = 0.05V/V： Range = 0V (0x00) to 36V (0xE1) with ΔV = 0.16V/step. (3) Default value = 0x21 with VOUT ratio = 0.08V/V for UVP_REF = 3.3V.					

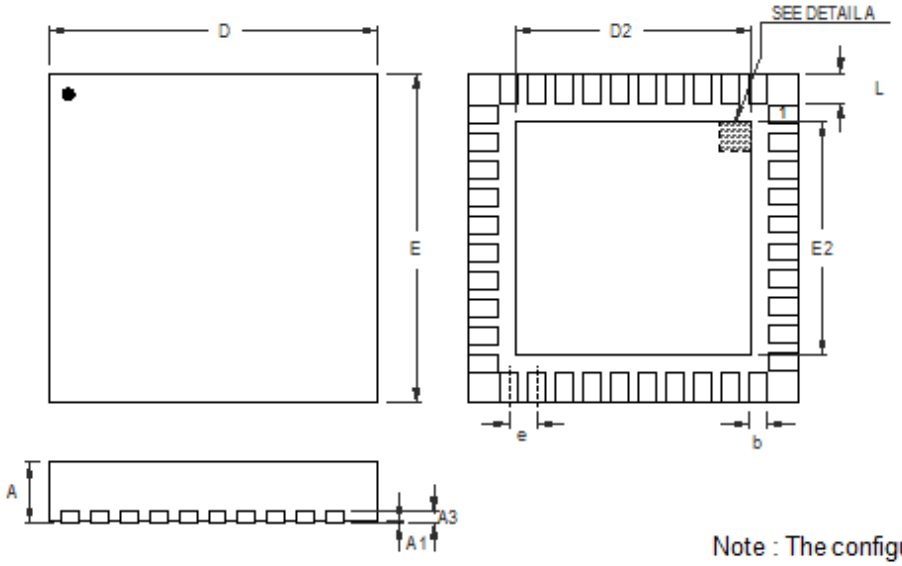
Register Address	0x36		Register Name	OVP_Reference				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	1	1	0	1	1	1	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 0	OVP_REF		When 0x2B[4] = 1, OVP threshold can be adjusted independent as below: OVP = OVP_REF[7:0](Decimal) x ΔV (1) When 0x11[5] = 0, VOUT ratio = 0.08V/V： Range = 0V (0x00) to 25.5V (0xFF) with ΔV = 0.1V/step. (2) When 0x11[5] = 1, VOUT ratio = 0.05V/V： Range = 0V (0x00) to 36V (0xE1) with ΔV = 0.16V/step. (3) Default value = 0xDC with VOUT ratio = 0.08V/V for OVP_REF = 22V.					

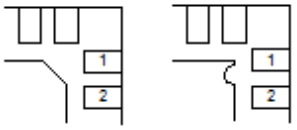
Register Address	0x37		Register Name	Status3				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
Bit 7 to Bit 5	Reserved		Reserved bits					
Bit 4	ALARM_LO		VBUSC alarm low indicator when VBUSC alarm low detection is enabled (0x2B[7] = 0). 0：VBUSC_VOLTAGE[10:0] > ALARM_LO[10:0] 1：VBUSC_VOLTAGE[10:0] < ALARM_LO[10:0]					
Bit 3	ALARM_HI		VBUSC alarm high indicator when VBUSC alarm high detection is enabled (0x2B[6] = 0). 0：VBUSC_VOLTAGE[10:0] < ALARM_HI[10:0] 1：VBUSC_VOLTAGE[10:0] > ALARM_HI[10:0]					
Bit 2	TO_275MS		275ms timeout indicator for DVS operation. 0：275ms timer is counting after OUT_CV[10:0] is changed for DVS operation. 1：Timeout completed when ALERT not go low after 275ms.					
Bit 1	IN_UVLO		Input UVLO indicator. (1) 0x0C[6] = 0, input = VIN for Forward operation. (2) 0x0C[6] = 1, input = VOUT for Reverse operation. 00：Input < 2.7V (typ.) 01/10：Reserved 11：Input > 3V (typ.)					
Bit 0								

Register Address	0x38		Register Name	Alert3				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 5	Reserved		Reserved bits					
Bit 4	ALERT_ALARM_LO		Internal flag to detect VBUSC status when VBUSC alarm low detection is enabled (0x2B[7] = 0). 0：VBUSC_VOLTAGE[10:0] > ALARM_LO[10:0] 1：VBUSC_VOLTAGE[10:0] < ALARM_LO[10:0] Note: After VBUSC_VOLTAGE[10:0] < ALARM_LO[10:0], this bit can be changed to "0" by writing this bit to "1" only.					
Bit 3	ALERT_ALARM_HI		Internal flag to detect VBUSC status when VBUSC alarm high detection is enabled (0x2B[6] = 0). 0：VBUSC_VOLTAGE[10:0] < ALARM_HI[10:0] 1：VBUSC_VOLTAGE[10:0] > ALARM_HI[10:0] Note: After VBUSC_VOLTAGE[10:0] > ALARM_HI[10:0], this bit can be changed to "0" by writing this bit to "1" only.					
Bit 2	ALERT_TO_275MS		Internal flag to detect 275ms timeout for DVS operation. 0：275ms timer is counting after OUT_CV[10:0] is changed for DVS operation. 1：Timeout completed when ALERT not go low after 275ms. Note: When 275ms timeout condition is removed, this bit can be changed to "0" by writing this bit to "1" only.					
Bit 1	ALERT_IN_UVLO_F		Internal flag to detect input UVLO falling. (1) 0x0C[6] = 0, input = VIN for Forward operation. (2) 0x0C[6] = 1, input = VOUT for Reverse operation. 0：Input > 2.7V (typ.) 1：Input < 2.7V (typ.) Note: After input < 2.7V, this bit can be changed to "0" by writing this bit to "1" only.					
Bit 0	ALERT_IN_UVLO_R		Internal flag to detect input UVLO rising. (1) 0x0C[6] = 0, input = VIN for Forward operation. (2) 0x0C[6] = 1, input = VOUT for Reverse operation. 0：Input < 3V (typ.) 1：Input > 3V (typ.) Note: After input > 3V, this bit can be changed to "0" by writing this bit to "1" only.					

Register Address	0x39		Register Name	Mask3				
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	RW	RW	RW	RW	RW
Bits	**Name**		**Description**					
Bit 7 to Bit 5	Reserved		Reserved bits					
Bit 4	M_ALERT_ALARM_LO		Mask internal flag output of VBUSC status when VBUSC alarm low detection is enabled (0x2B[7] = 0) to ALERT pin. 0：Mask 1：Not mask					
Bit 3	M_ALERT_ALARM_HI		Mask internal flag output of VBUSC status when VBUSC alarm high detection is enabled (0x2B[6] = 0) to ALERT pin. 0：Mask 1：Not mask					
Bit 2	M_ALERT_TO_275MS		Mask internal flag output of 275ms timeout for DVS operation to ALERT pin. 0：Mask 1：Not mask					
Bit 1	M_ALERT_IN_UVLO_F		Mask internal flag output of input UVLO falling to ALERT pin. (1) 0x0C[6] = 0, input = VIN for Forward operation. (2) 0x0C[6] = 1, input = VOUT for Reverse operation. 0：Mask 1：Not mask					
Bit 0	M_ALERT_IN_UVLO_R		Mask internal flag output of input UVLO rising to ALERT pin. (1) 0x0C[6] = 0, input = VIN for Forward operation. (2) 0x0C[6] = 1, input = VOUT for Reverse operation. 0：Mask 1：Not mask					

Outline Dimension





DETAIL A

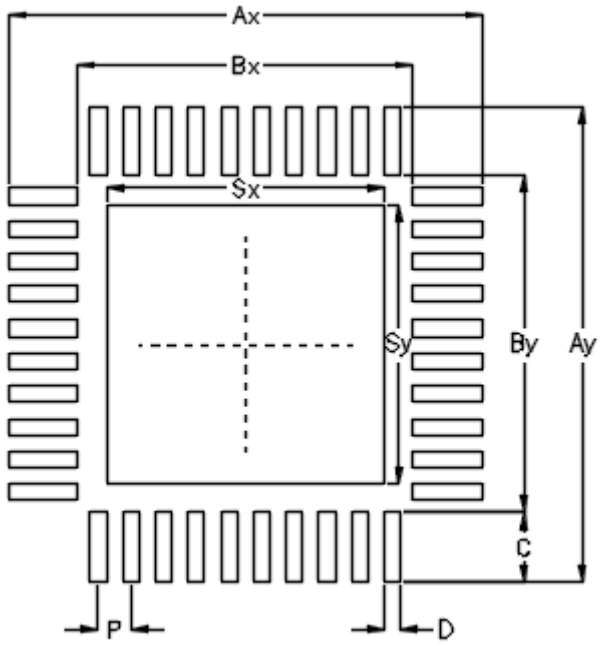
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-40	40	0.40	5.80	5.80	4.10	4.10	0.85	0.20	3.40	3.40	±0.05

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Datasheet Revision History

Version	Date	Description	Item
03	2022/12/01	Modify	General Description on P1 Features on P1 Operation on P6 Recommended BOM on P23 Application Information on P33, P34, P36, P37, P40 I^2C Register Summary on P42, 52