RICHTEK®

RTQ2522A/B

2A Ultra-Low Dropout Voltage LDO Regulators with Soft-Start

1 General Description

The RTQ2522A/B is a very low dropout linear regulator which operates from input voltage as low as 0.8V. The device is capable of supplying 2A of output current with a typical dropout voltage of only 90mV. A VBIAS supply is required to run the internal reference and LDO circuitry while output current comes directly from the VIN supply for high efficiency regulation. User-programmable soft-start limits the input inrush current and minimizes stress on the input power. The enable input and power good output allow easy sequencing with external regulators. This complete flexibility provides an easy-to-use robust power management solution for a wide variety of applications.

The RTQ2522A/B is stable with output capacitor greater than or equal to 2.2μF. A precise reference and error amplifier deliver 1% accuracy over load, line and temperature. Overcurrent limit and over-temperature protection are also included. The RTQ2522A/B is available in the WDFN-10L 3x3 and WQFN-20L 5x5 packages. The recommended ambient temperature range is −40°C to 105°C and junction temperature range is −40°C to 125°C.

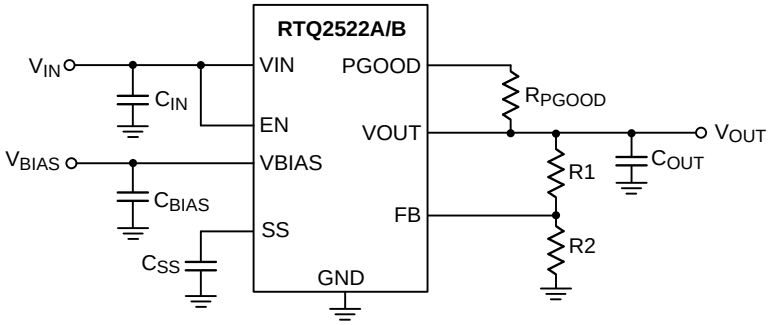
2 Features

- **Ultra low V_{IN} Range: 0.8V to 5.5V**
- **VBIAS Voltage Range: 2.7V to 5.5V**
- **VOUT Voltage Range: 0.8V to 3.6V**
- **Low Dropout: 90mV Typical at 2A, V_{BIAS} = 5V**
- **1% Accuracy Over Line/Load/Temperature**
- **PGOOD Indicator for Easy Sequence Control**
- **Programmable Soft-Start Provides Linear Voltage Startup**
- **Stable with Any Output Capacitor ≥ 2.2μF**
- **Overcurrent and Over-Temperature Protection**

3 Applications

- PCs, Servers, Modems, and Set-Top-Boxes
- FPGA Applications
- DSP Core and I/O Voltages
- Instrumentation
- Post-Regulation Applications
- Applications With Sequencing Requirements

4 Simplified Application Circuit



5 Ordering Information

RTQ2522A/B □□□

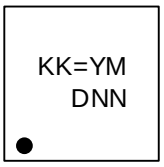
- Pin 1 Orientation
  (2) : Quadrant 2, Follow EIA-481
  (Empty means Pin1 orientation is Quadrant 1)
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
  QW : WQFN-20L 5x5 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant
- A : WDFN-10L 3x3
  B : WQFN-20L 5x5

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

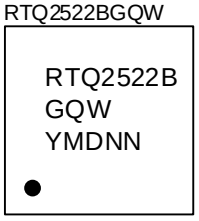
6 Marking Information

RTQ2522AGQW



KK= : Product Code
YMDNN : Date Code

RTQ2522BGQW



RTQ2522BGQW : Product Number
YMDNN : Date Code

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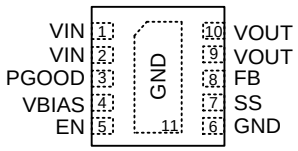
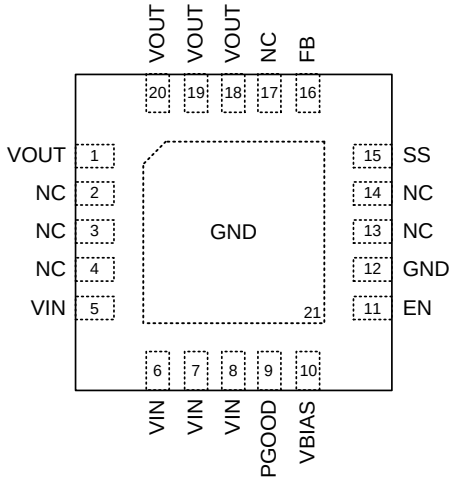
7 Pin Configuration

(TOP VIEW)



WDFN-10L 3x3



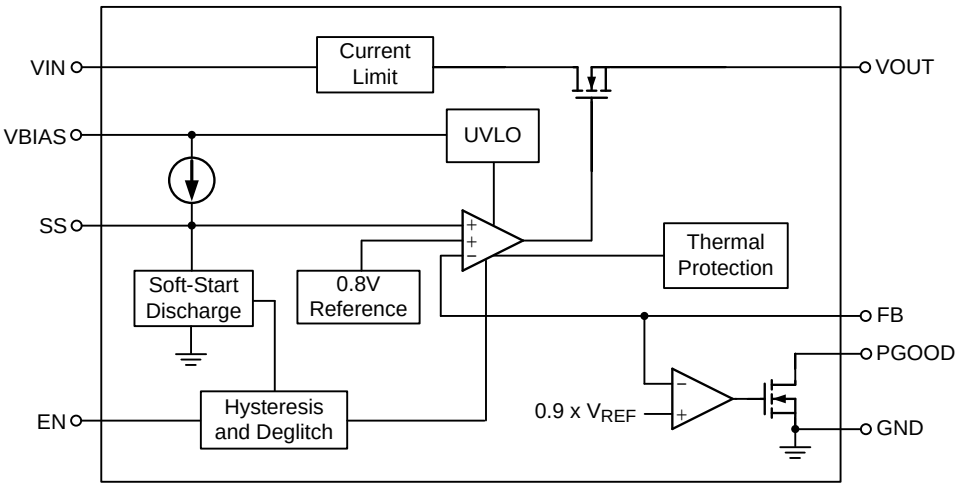
WQFN-20L 5x5

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN-10L 3x3	WQFN-20L 5x5		
1, 2	5, 6, 7, 8	VIN	Power input of the device.
9, 10	1, 18, 19, 20	VOUT	Regulated output voltage. A minimum of 2.2μF capacitor should be placed directly at this pin.
3	9	PGOOD	Power good indicator. An open-drain, active-high output that indicates the status of VOUT. A pull-up resistor from 10kΩ to 1MΩ should be connected from this pin to a supply of up to 5.5V.
4	10	VBIAS	Bias input pin. Providing input voltage for internal control circuitry.
5	11	EN	Chip enable (Active-High). Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. Connect to VIN if not being used.
6 11 (Exposed Pad)	12 21 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	15	SS	Connect a capacitor between this pin and the ground to set the soft-start ramp time of the output voltage.
8	16	FB	Feedback pin. Connect this pin to an external voltage divider to set the output voltage.

Pin No.		Pin Name	Pin Function
WDFN-10L 3x3	WQFN-20L 5x5		
--	2, 3, 4, 13, 14, 17	NC	No internal connection. This pin can be left floating or connected to GND.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Output Voltage, VOUT ---------- –0.3V to (V_{IN} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 3.27W
  - WQFN-20L 5x5 ---------- 3.54W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 30.5°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
  - WQFN-20L 5x5, θ_{JA} ---------- 28.2°C/W
  - WQFN-20L 5x5, θ_{JC} ---------- 7.1°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
- HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 0.8V to 5.5V
- Ambient Temperature Range ---------- –40°C to 105°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

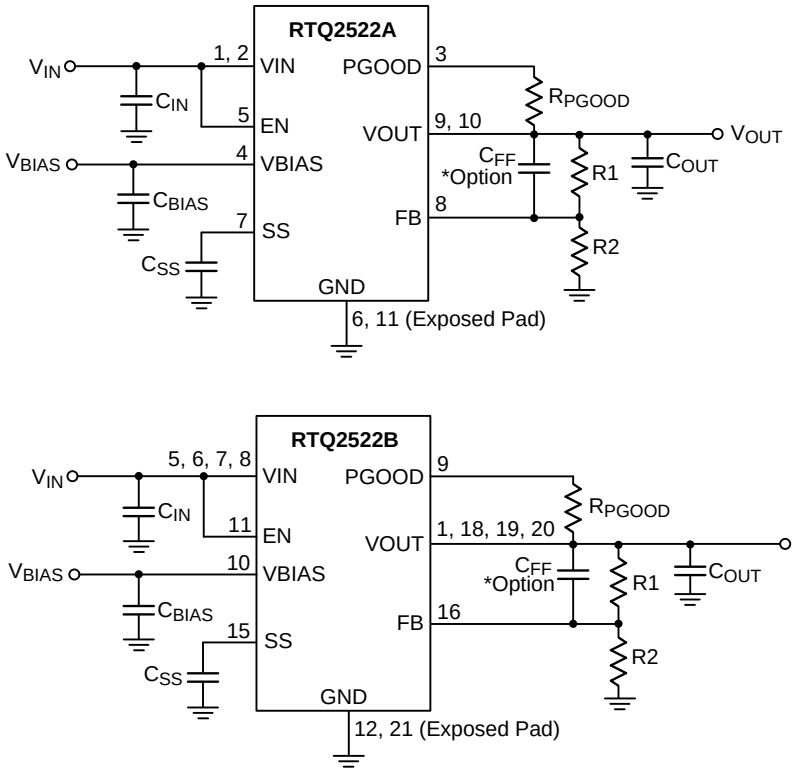
(V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 5V, C_{BIAS} = 0.1µF, C_{IN} = C_{OUT} = 10µF, C_{SS} = 1nF, I_{OUT} = 50mA, T_A = –40°C to 105°C, unless otherwise specified. Typical values are at T_A = 25°C)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		V_{OUT} + V_{DROP}	--	5.5	V
VBIAS Pin Voltage		V_{BIAS}		2.7	--	5.5	V
Internal Reference		V_{REF}	T_A = 25°C	0.796	0.8	0.804	V
Output Voltage Range		V_{OUT}	V_{IN} = 5V, I_{OUT} = 2A	V_{REF}	--	3.6	V
Accuracy			2.97V ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 2A	–1	±0.5	1	%
Line Regulation		ΔV_{LINE}	V_{OUT} (Normal) + 0.3 ≤ V_{IN} ≤ 5.5V	--	0.03	--	%/V
Load Regulation		ΔV_{LOAD}	50mA ≤ I_{OUT} = 2A	--	0.09		%/A
VIN Dropout Voltage		V_{DROP_VIN}	I_{OUT} = 2A, V_{BIAS} – V_{OUT} (Normal) ≥ 3.25V	--	90	140	mV
VBIAS Dropout Voltage		V_{DROP_VBIAS}	I_{OUT} = 2.0A, V_{IN} = V_{BIAS}	--	--	1.3	V
			I_{OUT} = 1.0A, V_{IN} = V_{BIAS}	--	--	1.2	
			I_{OUT} = 0.5A, V_{IN} = V_{BIAS}	--	--	1.1	
Current Limit		I_{LIM}	V_{OUT} = 80% × V_{OUT} (Normal)	2.5	--	5.5	A
Bias Pin Current		I_{BIAS}		--	1	2	mA
Shutdown Supply Current (I_{GND})		I_{SHDN}	V_{EN} = 0.4V	--	1	50	µA
Feedback Pin Current		I_{FB}		–1	0.15	1	µA
Power-Supply Rejection (VIN to VOUT)		PSRR (Note 5)	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	60	--	dB
			300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	30	--	
Power-Supply Rejection (VBIAS to VOUT)			1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	50	--	dB
			300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	30	--	
Output Noise Voltage		Noise (Note 5)	100Hz to 100kHz, I_{OUT} = 1.5A, C_{SS} = 0.001µF	--	25 x V_{OUT}	--	μV_{RMS}
Minimum Startup Time		t_{STR} (Note 5)	R_{LOAD} for I_{OUT} = 1A, C_{SS} = open	--	200	--	µs
Soft-Start Charging Current		I_{SS}	V_{SS} = 0.4V	--	440	--	nA
Enable Input Voltage	Logic_High	V_{IH}		1.1	--	5.5	V
	Logic_Low	V_{IL}		0	--	0.4	
Enable Pin Hysteresis		V_{EN_HYS}		--	50	--	mV
Enable Pin Deglitch Time		V_{EN_DG}		--	20	--	µs
Enable Pin Current		I_{EN}	V_{EN} = 5V	--	0.1	1	µA
PGOOD Trip Threshold		V_{IT}	V_{OUT} decreasing	85	90	94	%V_{OUT}
PGOOD Trip Hysteresis		V_{HYS}		--	3	--	%V_{OUT}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD Output Low Voltage	V_{PGOOD_L}	I_{PGOOD} = 1mA (sinking), $V_{OUT} < V_{IT}$	--	--	0.3	V
PGOOD Leakage Current	I_{PGOOD_LK}	V_{PGOOD} = 5.25 V, $V_{OUT} > V_{IT}$	--	0.1	1	μA
Thermal Shutdown Temperature	T_{SD}	Shutdown, temperature increasing	--	165	--	°C
		Reset, temperature decreasing	--	140	--	

Note 5. Guaranteed by design.

14 Typical Application Circuit

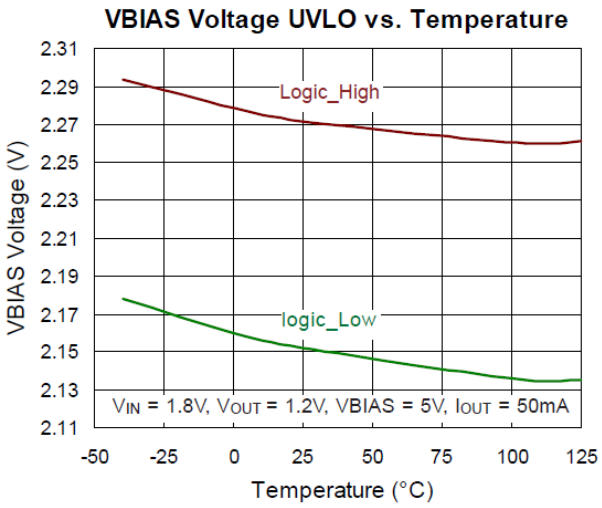


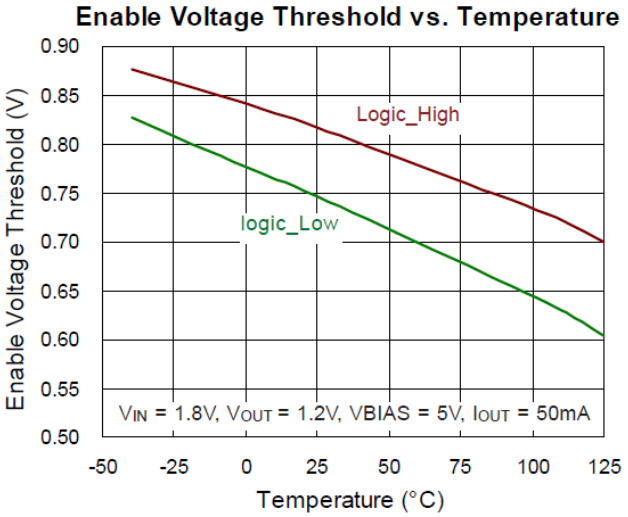
*: The feedforward capacitor is optional for the transient response and circuit stability improvement.

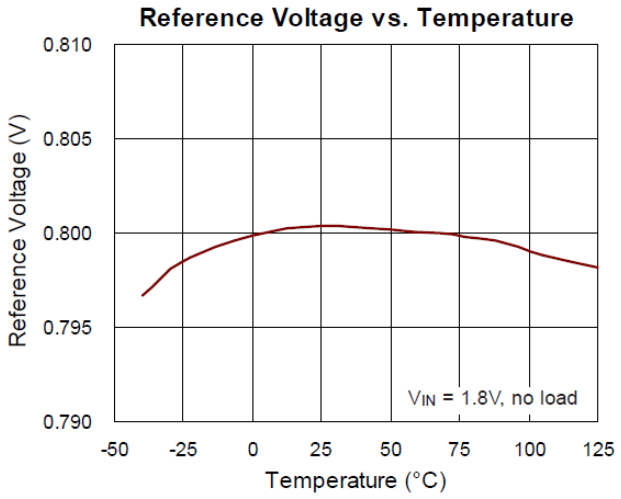
Table 1. Suggested Component Value

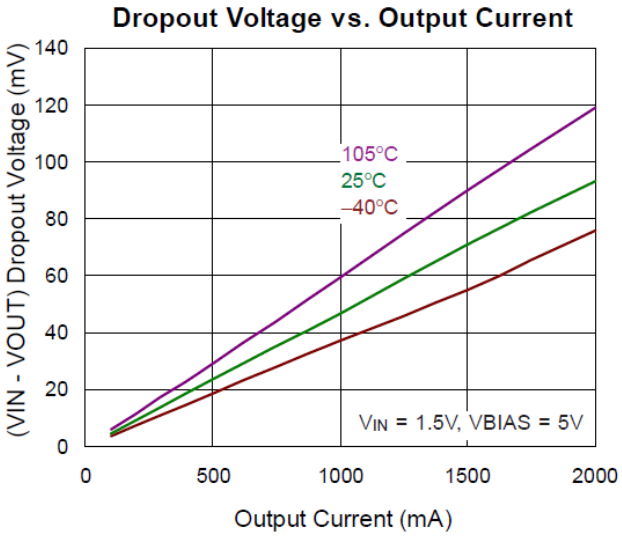
VOUT (V)	R1 (kΩ)	R2 (kΩ)
0.8	Short	Open
0.9	0.619	4.99
1.0	1.13	4.53
1.05	1.37	4.42
1.1	1.87	4.99
1.2	2.49	4.99
1.5	4.12	4.75
1.8	3.57	2.87
2.5	3.57	1.69
3.3	3.57	1.15

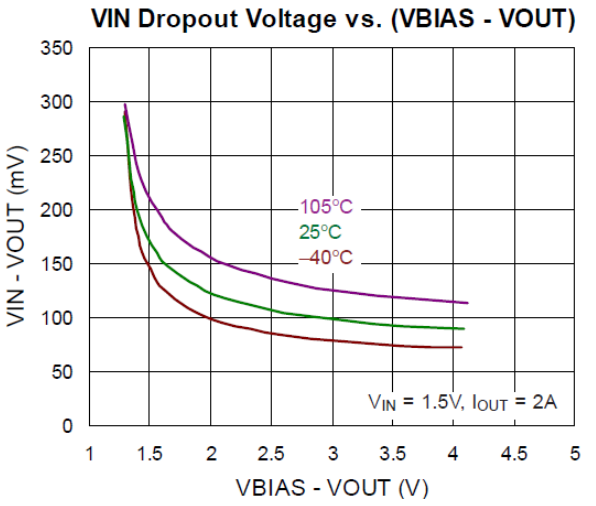
15 Typical Operating Characteristics

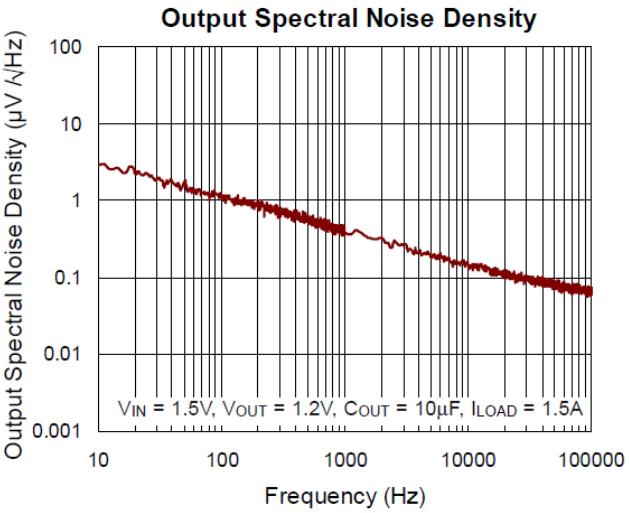


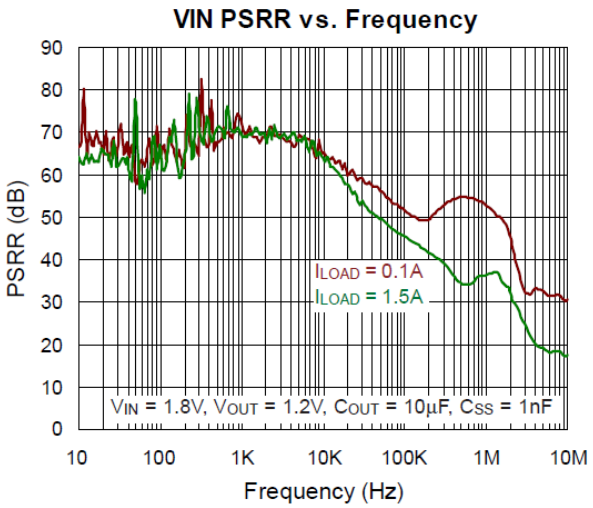


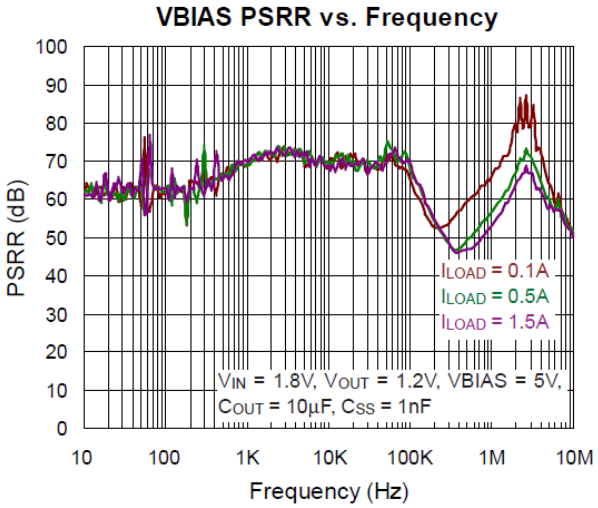


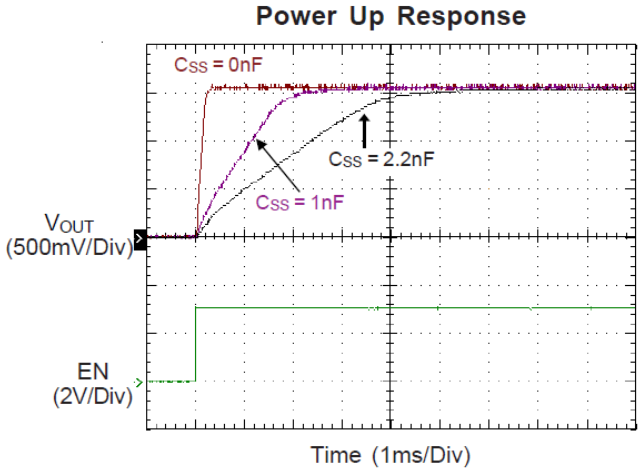


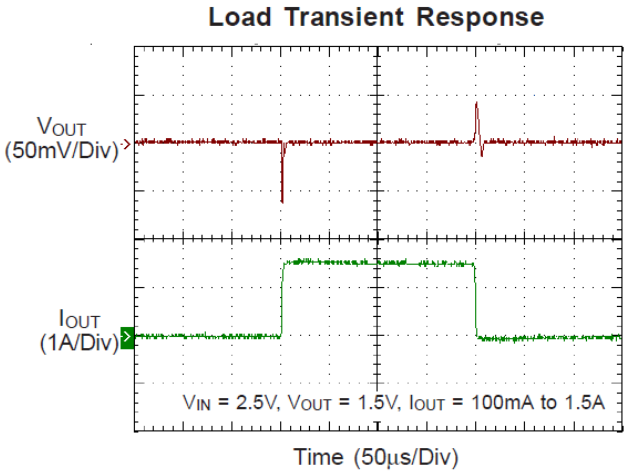












16 Operation

The RTQ2522A/B is a very low dropout linear regulator which operates from input voltage as low as 0.8V. It provides a highly accurate output that is capable of supplying 2A of output current with a typical dropout voltage of only 90mV. Output voltage range is from 0.8V to 3.6V.

16.1 VIN and VBIAS Supply

The VBIAS input supplies the internal reference and LDO circuitry while all output current comes directly from the VIN input for high efficiency regulation. With external VBIAS 3.25V above VOUT, offers the RTQ2522A/B very low dropout performance (140mV Max. at 2A) which allows the device to be used in place of a DC-DC converter and still achieve good efficiency. This provides designers to achieve the smallest, simplest, and lowest cost solution.

For applications where an auxiliary bias voltage is not available or low dropout is not required. In these applications, VBIAS is suggested be 1.3V above VOUT and attention on power rating and thermal is needed.

16.2 Enable and Shutdown

The EN pin is active high. Apply a voltage above 1.1V ensures the LDO regulator turns on, while the regulator turns off if the V_{EN} belows 0.4V. The enable circuitry has typical 50mV hysteresis and deglitching for use with relatively slowly ramping analog signals. That helps avoid on-off cycling as a result of small glitches in the V_{EN} signal. A fast rise-time signal must be used to enable the RTQ2522A/B if precise turn-on timing is required. If not used, EN can be connected to either VIN or VBIAS. If EN is connected to VIN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

16.3 Soft-Start

The RTQ2522A/B includes a soft-start feature to prevent excessive current flow during start-up. When the LDO is enabled, an internal soft-start current (I_{SS}) charges the external soft-start capacitor (C_{SS}) to build a ramp-up voltage internally. The RTQ2522A/B achieve a linear and monotonic soft-start by tracking the voltage ramp until the voltage exceeds the internal reference. The soft-start ramp time can be calculated using Equation 1:

$$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A} \quad (1)$$

16.4 Power GOOD

When the output voltage is greater than V_{IT} + V_{HYS}, the output voltage is considered good and the open-drain PGOOD pin goes high impedance and is typically pulled high with external resistor. If VOUT drops below V_{IT} or if VBIAS drops below 1.9 V, the open-drain output turns on and pulls the PGOOD output low. The PGOOD pin also asserts when the device is disabled, OCP or OTP triggered.

16.5 Overcurrent Protection

The RTQ2522A/B has built-in overcurrent protection. When overcurrent (typ. 3A) is detected, the RTQ2522A/B foldback and limit the current at typical 2.25A. It allows the device to supply surges of up to 3A and prevent the device over-heating if short circuit happened.

16.6 Thermal Shutdown and Over-temperature Protection

At higher temperatures, or in cases where internal power dissipation causes excessive self heating on chip, the thermal shutdown circuitry will shut down the LDO when the junction temperature exceeds approximately 160°C. It will re enable the LDO once the junction temperature drops back to approximately 140°C. The RTQ2522A/B will cycle in and out of thermal shutdown without latch-up or damage until the overstress condition is removed. Long term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and

therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

17 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RTQ2522A/B is a low dropout regulator that features soft-start capability. It provides EN and PGOOD for easily system sequence control, and built-in overcurrent & thermal protection for safe operation.

17.1 Dropout Voltage

Because of two power supply inputs VIN and VBIAS and one VOUT regulator output, there are two Dropout voltages specified. The first is the VIN Dropout voltage is the voltage difference ($V_{IN} - V_{OUT}$) when VOUT starts to decrease by percent specified in the Electrical Characteristics table.

The second, VBIAS dropout voltage is the voltage difference ($V_{BIAS} - V_{OUT}$) when VIN and VBIAS pins are joined together and V_{OUT} starts to decrease. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. In these applications, V_{BIAS} is suggested be 1.3V above V_{OUT} and attention on power rating and thermal is needed.

17.2 Input, Output, and Bias Capacitor Selection

The device is designed to be stable for all available types and values of output capacitors $\geq 2.2\mu F$. The device is also stable with multiple capacitors in parallel, which can be of any type or value. The capacitance required on the VIN and VBIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is $1\mu F$ and minimum recommended capacitor for V_{BIAS} is $0.1\mu F$. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is $4.7\mu F$. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.

17.3 Adjusting the Output Voltage

The output voltage of the RTQ2522A/B is adjustable from 0.8V to 3.6V by external voltage divider resisters as shown in Typical Application Circuit. R1 and R2 can be calculated the output voltage. In order to achieve the maximum accuracy specifications, R2 should be $\leq 4.99k\Omega$.

17.4 Power Up Sequence Requirement

The RTQ2522A/B supports power on the input VIN, VBIAS, and EN pins in any order without damage the device. Generally, connecting the EN and VIN for most application is acceptable, as long as VIN and V_{EN} is greater than the EN threshold (typ. = 1.1V) and the input ramp rate of VIN and VBIAS is faster than the output settled soft-start ramp rate. If the VIN/BIAS input source ramp rate is slower than the output settled soft-start time, the output will track the input supply ramp up level and minus the dropout voltage until it reaches the settled output voltage level. For the other case, If EN is connected with VBIAS, and the provided VIN is present before VBIAS, the output soft-start will as programmed. While VBIAS and V_{EN} are present before VIN is applied also the settled soft-start time has expired, then VOUT tracks VIN ramp up. If the soft-start time has not expired, output tracks VIN ramp up until output reaches the value set by the charging soft- start capacitor.

17.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the

difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WQFN-20L 5x5 package, the thermal resistance, θ_{JA}, is 28.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 3.27W for a WDFN-10L 3x3 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (28.2°C/W) = 3.54W for a WQFN-20L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

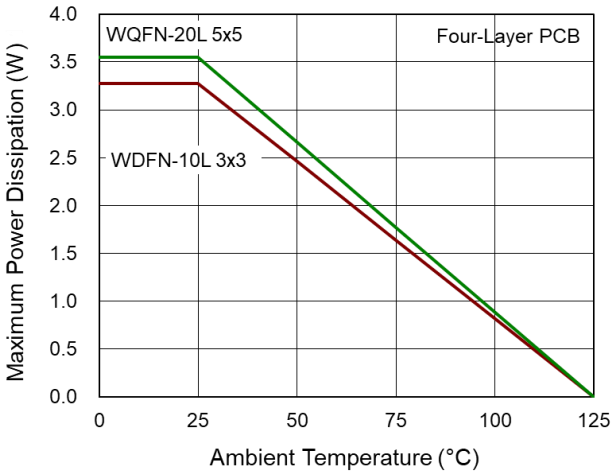


Figure 1. Derating Curve of Maximum Power Dissipation

17.6 Layout Considerations

For best performance of the RTQ2522A/B, the PCB layout suggestions below are highly recommended:

- Input capacitor must be placed as close as possible to IC to minimize the power loop area.
- Minimize the power trace length and avoid using vias for the input and output capacitors connection.

Figure 2 and Figure 3 shows the examples for the layout reference which helps the inductive parasitic components minimization, load transient reduction and good circuit stability.

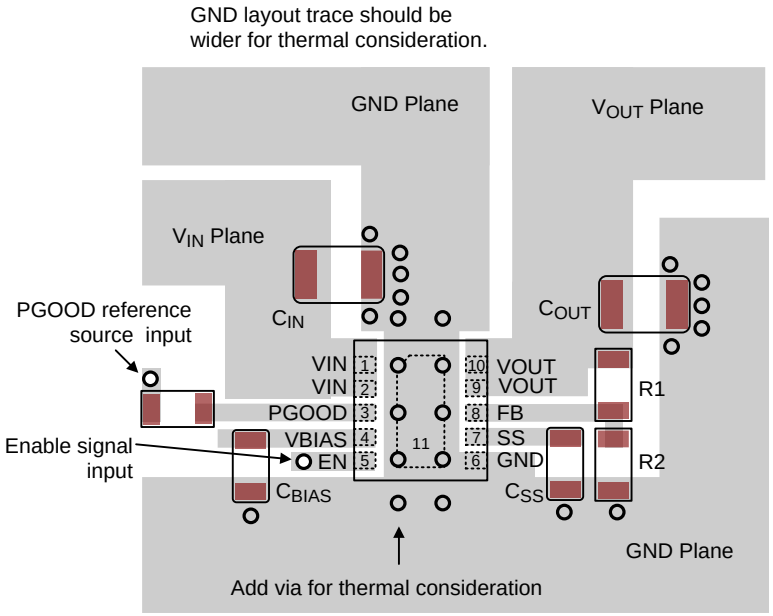


Figure 2. RTQ2522A PCB Layout Guide

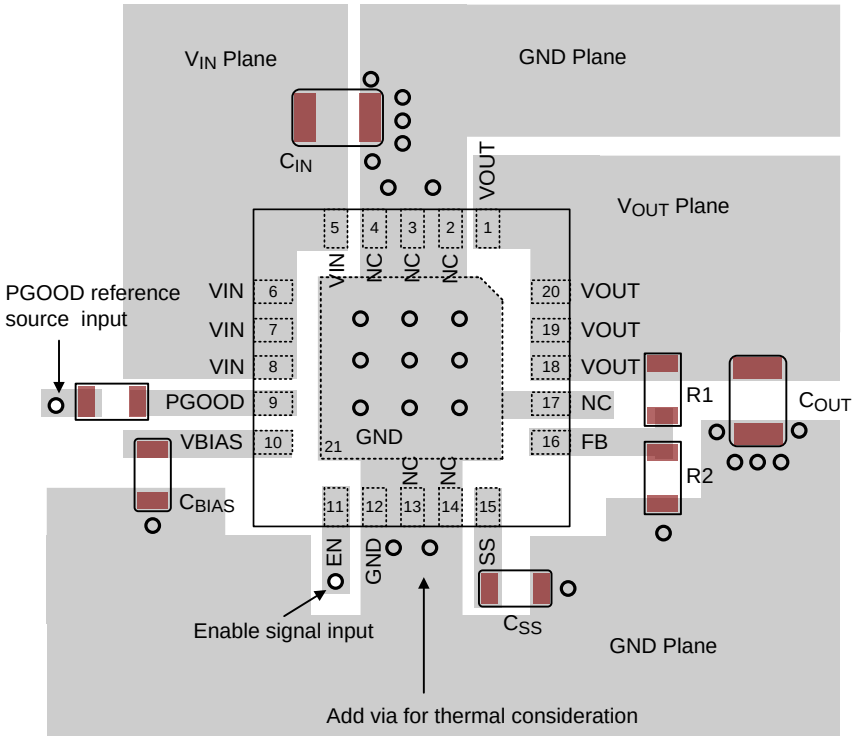
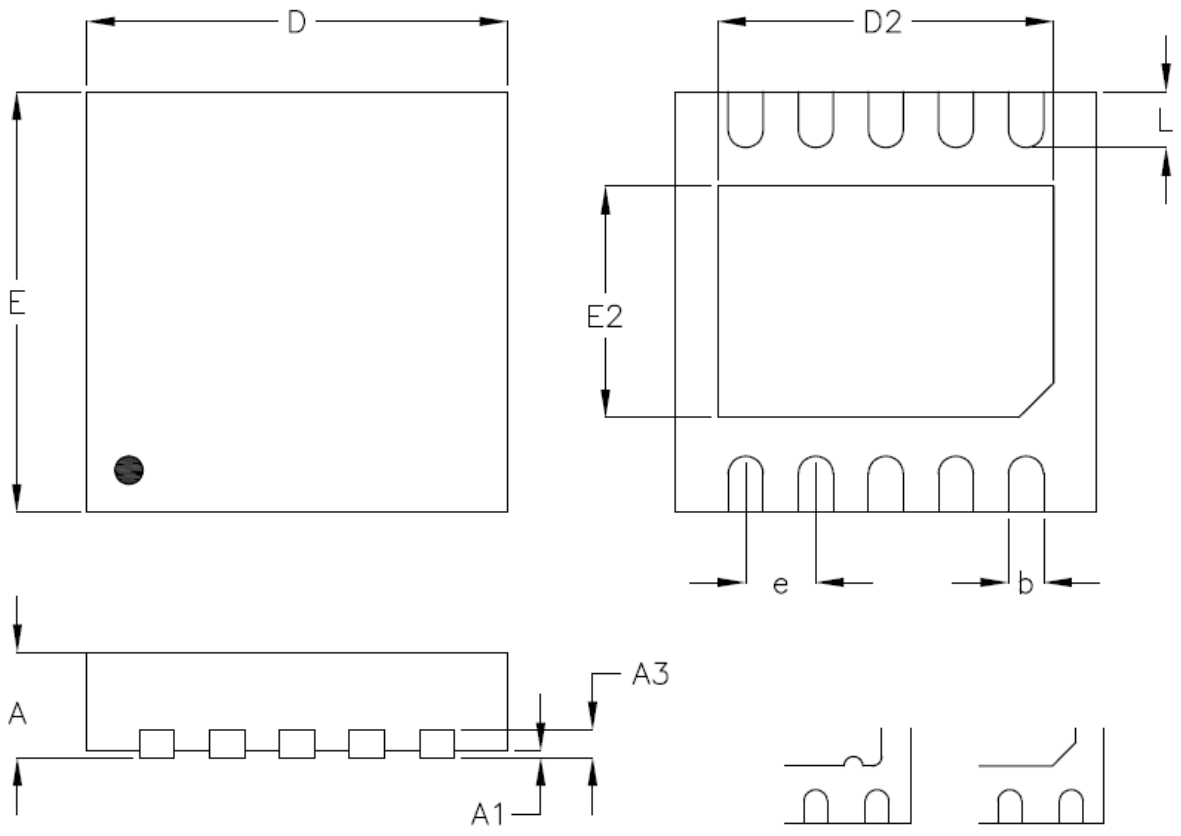


Figure 3. RTQ2522B PCB Layout Guide

18 Outline Dimension

18.1 WDFN-10L 3x3 Package

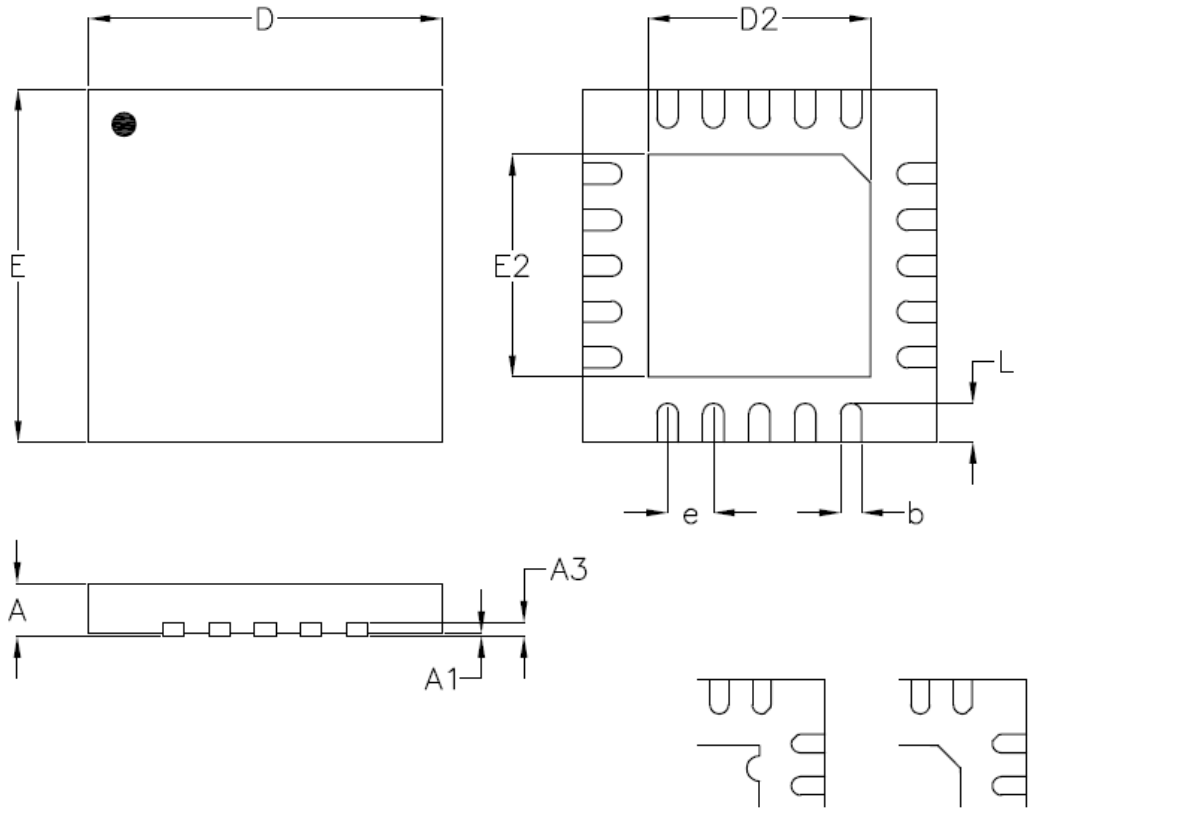


Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

18.2 WQFN-20L 5x5 package



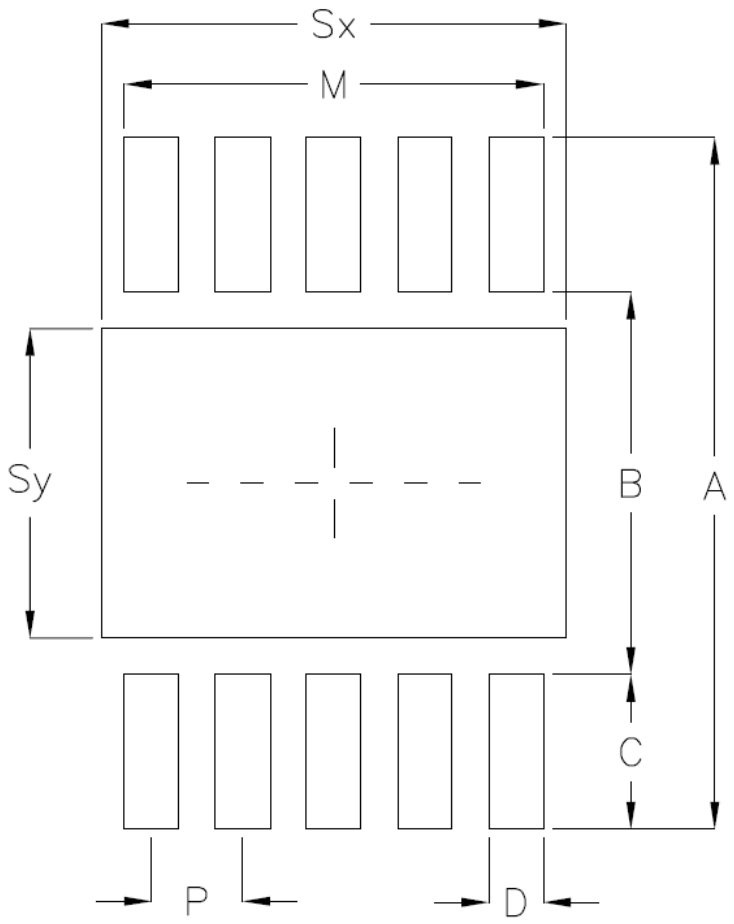
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.350	0.010	0.014
D	4.900	5.100	0.193	0.201
D2	3.100	3.200	0.122	0.126
E	4.900	5.100	0.193	0.201
E2	3.100	3.200	0.122	0.126
e	0.650		0.026	
L	0.500	0.600	0.020	0.024

W-Type 20L QFN 5x5 Package

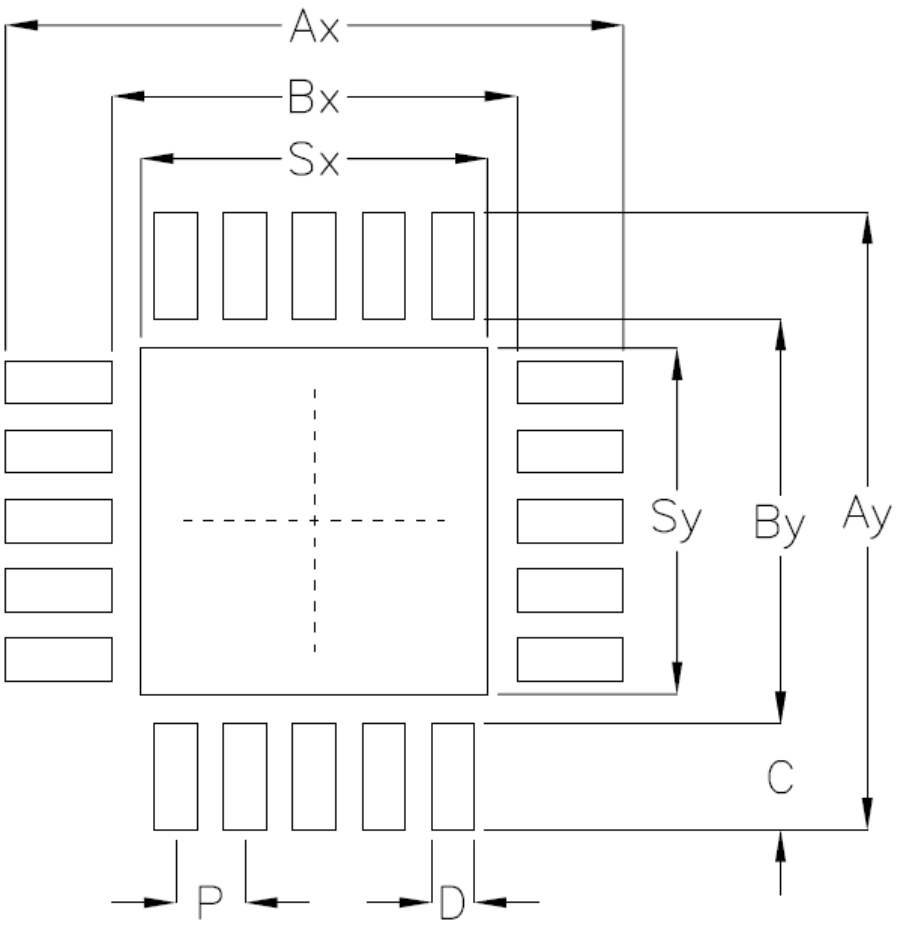
19 Footprint Information

19.1 WDFN-10L 3x3 Package



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

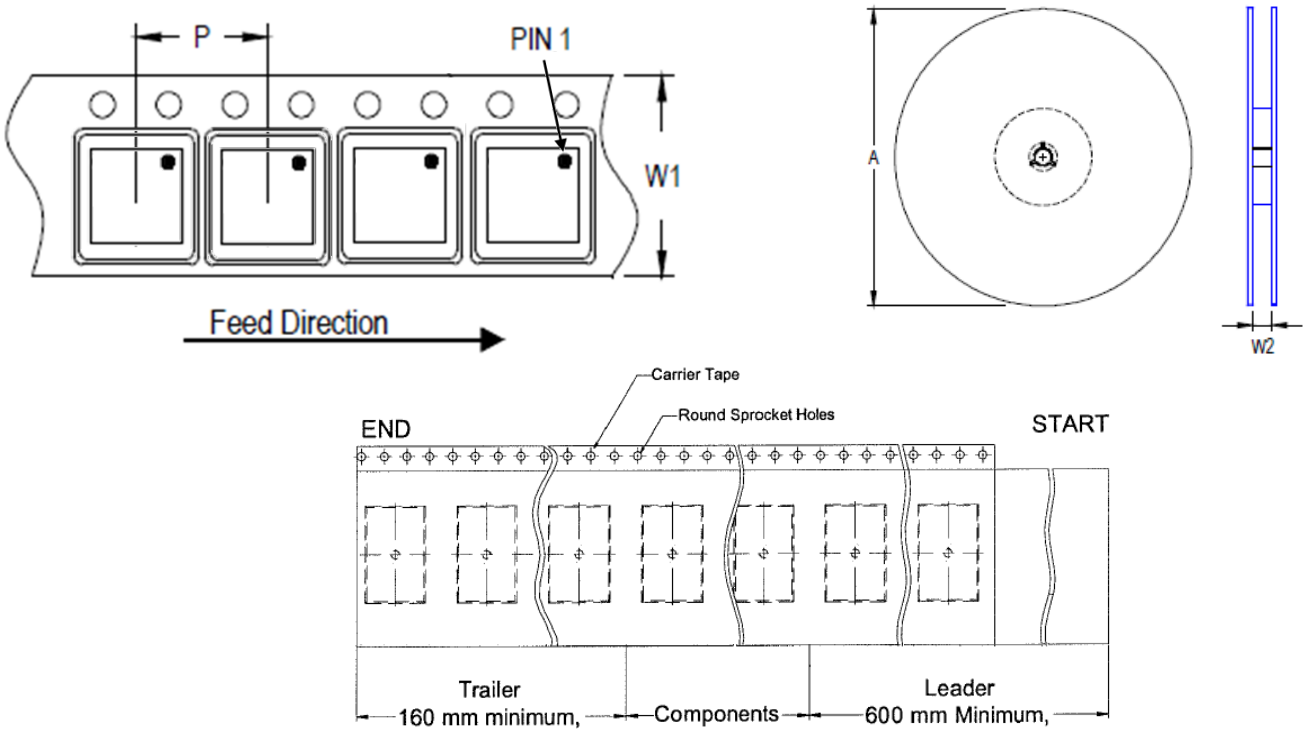
19.2 WQFN-20L 5x5 package



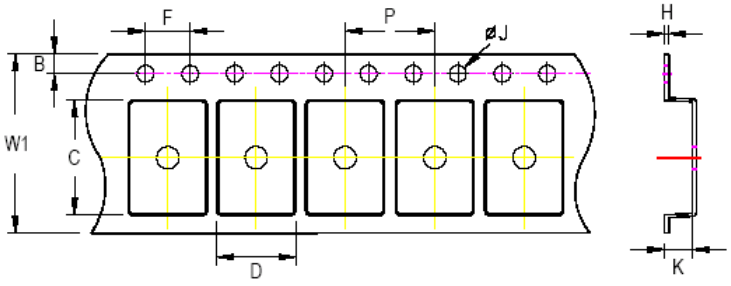
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-20	20	0.65	5.80	5.80	3.80	3.80	1.00	0.40	3.25	3.25	±0.05

20 Packing Information

20.1 WDFN-10L 3x3 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leade r(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

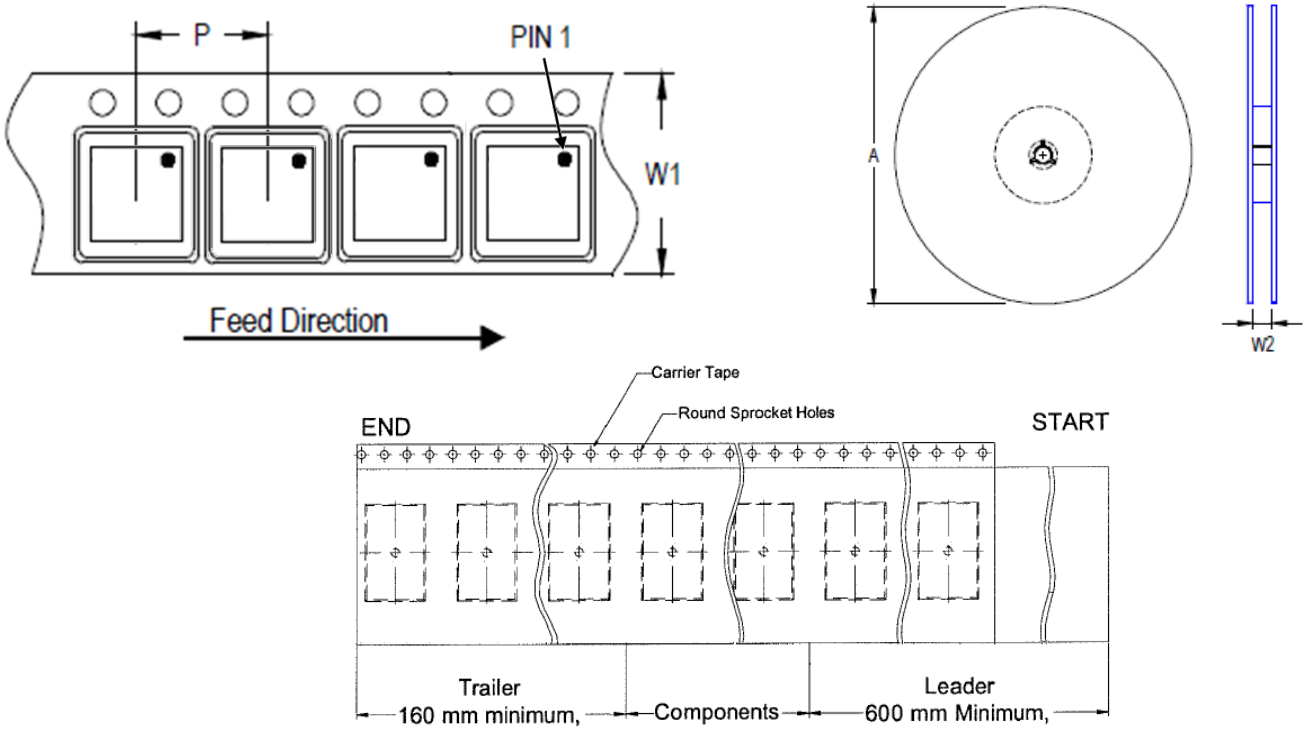
Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 Tape and Reel Packing

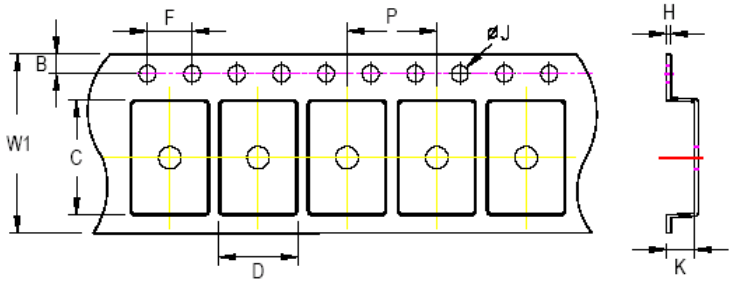
Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*40.0	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

20.3 WQFN-20L 5x5 package Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.4 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 5x5	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*40.0	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Partial Reel.			

20.5 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
04	2023/8/7	Modify	General Description on P1 Features on P1 Ordering Information on P1 Operation on P3 Electrical Characteristics on P5 Application Information on P10
05	2024/3/25	Modify	Features on P1 General Description on P1 Ordering Information on P2 Recommended Operating Conditions on P6 Electrical Characteristics On p7 Operation on P12, 13 Application Information on P14 Packing Information on P21, 22, 23, 24, 25